



Special Interest Group on Design Automation ACM/SIGDA E-NEWSLETTER, Vol. 56, No. 9

SIGDA - The Resource for EDA Professionals

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Online archive: <https://www.sigda.org/newsletters/>

SIGDA News

1. Chips Act 2.0, Part 1: Europe's Second Semiconductor Push **Chips Act 2.0, Part 2: From Brussels to the Bench: What Chips Act 2.0 Means for Engineers**

The EU's first Chips Act was sold with a simple ambition: strengthen Europe's semiconductor industry and raise its share of the global chip value chain to 20% by 2030. Three years after the legislation entered into force, that target looks increasingly remote.

2. NVIDIA Secures 8 GW Ohio AI Campus for OpenAI

Samsung Electronics has outlined a new generation of 3D memory products aimed at improving the performance and energy efficiency of AI infrastructure. The company previewed the technologies at Future of Memory and Storage (FMS) 2026 in Santa Clara, California, alongside a portfolio spanning DRAM, NAND and enterprise storage.

3. AWS and NVIDIA Plan 2 Million-GPU AI Expansion

Amazon Web Services (AWS) and NVIDIA are expanding their long-running AI infrastructure partnership with plans to deploy 2 million additional NVIDIA GPUs across AWS data centers in 2027 and 2028.

4. Micron Launches \$10BN AI Memory Research Hub

Micron Technology is setting up a long-term U.S. research hub with a planned \$10 billion investment over the next decade, targeting new memory, computing and semiconductor manufacturing technologies for the AI era.

5. Quanta Computer and Quantinuum Team Up to Scale Computing

Quanta Computer and Quantinuum have signed a collaborative development agreement aimed at building the industrial infrastructure needed for large-scale quantum computers. The partnership brings together Quantinuum's quantum computing technology with Quanta's experience in manufacturing and scaling advanced computing platforms.

6. IBM and OpenAI Partner on Secure Enterprise AI

IBM and OpenAI have formed a strategic partnership aimed at helping large organizations deploy AI across core business operations, legacy applications and cybersecurity environments.

Message from the EiC

Dear SIGDA members,

In this edition, we bring you the latest news and activities in our community, paper deadlines, upcoming conferences, an insightful article on What is Quantum Systems Engineering, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

7. [SK Hynix Sets First HBF Standard for AI Memory](#)

SK hynix and Sandisk have unveiled the first standard specification for High Bandwidth Flash (HBF), positioning the technology as a new memory tier for AI infrastructure.

8. [Nvidia Serves 2.4T-Parameter Qwen3.8 Model on GB300 NVL72](#)

Nvidia has published Day-0 inference results for Alibaba's open-weight Qwen3.8-2.4T-A95B, showing the 2.4-trillion-parameter Qwen3.8 model running across its GB300 NVL72 rack-scale system.

SIGDA Awards

1. 2026 ISLPED Best Paper Awards and Candidates @ ISLPED 2026

<https://www.islped.org/2026/final-program/>

- **A Current Mode Wireless Power Transfer with Deficit Energy Quantifier for Implanted Medical Devices**
Minsik Cho, Minhyeok Jeong, Hyunjun Choi, Mingyu Kim, Shin Han, and Yoonmyung Lee
- **[Best Paper Award] L²Mersit: A Scaling-Free Sub-8-bit Data Format for On-Device Reliable Large Language Model Serving**
Myeongjin Kim, Hyeonseong Kim, Ik Joon Chang, and Seungkyu Choi
- **[Best Paper Award] GCU-Net: A Hybrid CNN-Transformer Architecture for Fast and Accurate Dynamic Voltage Drop Prediction**
Freddy Gabbay and Mohammad Omri
- **CMAx-CAMEL: A Coarse-to-Fine Adaptive, Memory-Efficient, and Low-Power Edge Processor for Contrast Maximization**
Kyeongpil Min, Jongin Choi, Kyeongwon Lee, and Woojoo Lee
- **PowerFlow-DNN: Compiler-Directed Fine-Grained Power Orchestration for End-to-End Edge AI Inference**
Paul Yi-Chia Chen, Claire Jeongeun Kim, Wenbo Zhu, Yuanhan Li, Shun Yao Huang, Chenjie Weng, and Christopher Torng
- **Area-Efficient FHE Acceleration via Ciphertext-Level Parallelism and Shared-Key Reuse**
Youngtae Ahn, Jaehyung Kim, and Hyungmin Cho
- **[Best Paper Award] MITRA: Reconfigurable, Low-Latency, and Power-Efficient In-Memory Stochastic Architecture for Transcendental Functions**
Farzad Razi, Mehran Moghadam, M. Hassan Najafi, Serkan Aygun, and Marc D. Riedel
- **SA-Kura: An Energy-Efficient Systolic Array Accelerator for Locally-Coupled Kuramoto Drift in Diffusion Sampling**
Jeongmin Jin, Kyeongwon Lee, Mundo Jeong, Jongin Choi, and Woojoo Lee

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What is Quantum Systems Engineering?

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Quantum Computing (QC) is rapidly transitioning from a physics-only endeavor to an engineering challenge, for the benefit of scientific computing [1]. This scenario ushers in a new paradigm, Quantum High-Performance Computing (QHPC) [2], and with it a new research field, Quantum Systems Engineering [3]. It is of the utmost importance that we engineer these emerging hybrid systems by obeying dependability principles since their inception, striving to make them as reliable, scalable and usable as possible [4].

Unlike classical digital systems built with CMOS transistors, nowadays-available quantum devices are hampered by the early stage of technological development and the high sensitivity to environmental noise [5]. Different quantum technologies also boast very different characteristics, in terms of number of qubits (10s to 1000s), their connectivity (fixed, all-to-all), their coherence time (10s of microseconds to minutes), and the speed at which they can perform computations (nanoseconds to milliseconds). These issues push us to re-think the entire computing stack in order to plug these devices into HPC infrastructures.

QSE addresses these challenges by co-designing across multiple layers:

- Scientific Workload layer, where the HPC application and quantum algorithms live
- System Management layer, managing the distribution of tasks and managing resources
- Hardware layer, both in the classical and in the quantum domain, managing compilation, verification and execution.

These layers must work in concert with each other seamlessly, from the very high level definition of the user application, down to the sequence of pulses executed on the quantum device.

As in classical systems, systems engineering in quantum systems must fulfill the three pillars of dependability:

- reproducibility, running an experiment on different devices or the same device across time has to consistently provide the same results
- resiliency, maintaining correct system behavior in the presence of faults, errors, and environmental disturbances
- security and privacy, the ability to keep the system safe from attacks and maintaining the privacy of the data it handles.

The three pillars are deeply intertwined. For instance, environmental noise affects reproducibility, complicating fault detection that pertains resiliency. On

Paper Deadlines

ISSCC'27 – IEEE Int'l Solid-State Circuits Conference

San Francisco, CA, USA

Deadline: Sept. 9, 2026

Feb. 14-18, 2027

<http://isscc.org>

ISQED'27 - Int'l Symposium on Quality Electronic Design

San Francisco, CA, USA

Deadline: Sept. 17, 2026

Apr. 14-16, 2027

<http://www.isqed.org>

ISPD'27 – ACM Int'l Symposium on Physical Design

Taiwan

Abstracts due: Sept. 21, 2026

Deadline: Sept. 28, 2026

Mar 31- Apr. 2, 2027

<http://www.ispd.cc/>

DATE'27 - Design Automation and Test in Europe

Dresden, Germany

Abstracts due: Sept 13, 2026

Deadline: Sept. 20, 2026

March 22-24, 2027

<http://www.date-conference.com>

HOST'27 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust

Washington DC, USA

(winter submissions)

Abstracts due: Nov. 1, 2025

Deadline: Nov. 8, 2028

May 3-6, 2027

<http://www.hostsymposium.org>

the other hand, plugging quantum devices in cloud/HPC environments exposes them to new security risks that must be prevented at the system level.

Another fundamental goal of QSE is enabling scalable integration of hybrid systems. Nowadays, Quantum Processing Units (QPUs) are seen as coprocessors, akin to GPUs. To achieve an integration depth comparable to that of GPUs, however, requires overcoming challenges in hybrid programmability, workload orchestration, and fault management. On the user side, there is the need to develop new programming abstractions to ease the development of hybrid workloads [6], while on the hardware side there is the need to systematically analyse how faults manifest in a system in order to counteract or prevent them [7]. These research directions all aim towards one final goal: the creation of a quantum-classical operating system.

In the future, QSE is poised to become a foundational discipline that bridges together different domains: physics, computer architectures, and systems engineering. The achievement of quantum advantage for scientific computing applications for the benefit of humanity will happen when, not if, we get QSE right.

References:

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SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES)

features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor increased to

Upcoming Conferences

MLCAD'26 - ACM/IEEE Workshop on Machine Learning for CAD

Jeju Island, Korea
Sep. 7-9, 2026
<https://mlcad.org/symposium/>

VLSI-SoC'26 - IFIP/IEEE Int'l Conference on Very Large Scale Integration

Limassol, Cyprus
Oct. 11-14, 2026
<http://www.vlsi-soc.com>

MICRO'26 - IEEE/ACM Int'l Symposium on Microarchitecture

Athens, Greece
Oct. 31 - Nov. 4, 2026
<http://www.microarch.org/micro59>

ICCAD'26 - IEEE/ACM Int'l Conference on Computer-Aided Design

San Jose, CA, USA
Nov 8-12, 2026
<https://iccad.com/>

ICCD'26 - IEEE Int'l Conference on Computer Design

Hong Kong, China
Nov. 16-18, 2026
<http://www.iccd-conf.com>

FPT'26 - Int'l Conference on Field-Programmable Technology

Honolulu, Hawaii, USA
Dec. 7-10, 2026
<http://icfpt.org>

iSES'26 - IEEE Int'l Symposium on Smart Electronic Systems

Goa, India
Dec. 15-17, 2026
<http://www.ieee-ises.org>

2.2 in 2023, more than doubling its value from 2020. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through the [best paper](#) and [rookie of the year](#) awards. Authors can send their paper submissions to the [manuscript portal](#).

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Prabhat Mishra, Senior Associate Editor, at prabhat@ufl.edu

ASP-DAC'27 - Asia and South Pacific Design Automation Conference

Tokyo, Japan

Jan. 25-28, 2027

<http://www.aspdac.com>

Call for [Special Issue on Open, Reliable, and Generalizable Datasets for AI in EDA](#)

Submission Deadline: August 31, 2026

For questions and further information, please contact the guest editors:

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SIGDA Vision 2030

ACM SIGDA is launching SIGDA Vision 2030, a community-driven initiative to identify key challenges and define strategic priorities for the Design Automation field.

You can contribute by completing a short survey (5-10 minutes): <https://bit.ly/SIGDA-Vision-2030-Survey>

The input collected will be discussed in upcoming interactive sessions at major conferences (including DATE, DAC, and ICCAD) and will contribute to a strategic report outlining priorities and concrete actions for the coming years. Your input is extremely valuable in shaping the future of the community.

Technical Activities

1. [Insect-Inspired Neuromorphic Sensor Targets Physical AI](#)

Machine vision is undergoing a structural transition. For decades, digital video has relied primarily on frame-based cameras that capture full images at fixed intervals, creating large amounts of redundant data. Research teams are now exploring neuromorphic engineering, modeled on biological nervous systems, to address the latency and power limitations of conventional cameras...

2. [Chiplets Offer a Scalable Compute Strategy for Software-defined Vehicles](#)

As automotive compute demands accelerate, chiplet architectures offer scalable performance without sacrificing cost, software reuse, or reliability...

3. Energy Storage Moves from Backup to Critical Grid Infrastructure

As renewable energy moves deeper into the global electricity mix, energy storage is taking on a role that goes well beyond backup power. Batteries and other storage technologies are increasingly becoming part of the infrastructure needed to make power grids more flexible, reliable, and capable of handling variable generation...

4. AMD Bets on Heterogeneous SoCs to Break GPU Dominance in Robotics

AMD targets robotics with heterogeneous compute, unified memory, deterministic latency and open ecosystems to challenge GPU-centric architectures...

Job Positions

VinUniversity, Vietnam

Job Title: Faculty members of Computer Science

Description: The College of Engineering and Computer Science (CECS) at VinUniversity provides a rigorous academic foundation and extensive opportunities for interdisciplinary, application-oriented research and learning. The faculty members will be responsible for three primary responsibilities: Research: Lead high-impact research with strong translational outcomes and publications in top-tier journals and secure competitive external funding. Foster interdisciplinary collaboration within and beyond the College through active engagement in academic events. Contribute to innovation, entrepreneurship, and technology transfer, including commercialization efforts; Teaching: Develop, plan, and deliver high-quality, accredited curricula for undergraduate and/or graduate programs. Prepare course materials, deliver lectures and tutorials, assess student performance, provide feedback, and supervise academic projects. Supervise research students and projects, and mentor junior faculty to support their professional; Service: Contribute to university service through committee work, faculty recruitment, accreditation, and program development. Support initiatives aligned with VinUni's Vision 2030 and carry out duties assigned by the Dean. For more information, please refer to https://vinuni.talent.vn/careers/job/10779?utm_source=referral&utm_campaign=trangpnt&utm_medium=npoOJo231kjsyD6snjR-NA.

University of Massachusetts Lowell, US

Job Title: Open Rank Tenure-Track Faculty in Core AI

Description: The Miner School of Computer & Information Sciences at the University of Massachusetts Lowell invites applications for a tenure-track, open-rank faculty position in the field of core Artificial Intelligence (AI), including but not limited to Generative AI, Foundation Models, Large Language Models (LLMs), Vision-Language Models (VLMs), World Models, AI Agents, Multimodal Learning, Machine Learning, and Trustworthy AI. Starting in September 2027, this role is expected to help build our programs in Applied Artificial Intelligence and to contribute to the development of our recently established Center for Artificial

Intelligence Research Computing. Outstanding candidates with expertise in core areas of AI, including but not limited to Generative AI, Foundation Models, Large Language Models (LLMs), Vision-Language Models (VLMs), World Models, AI Agents, Multimodal Learning, Machine Learning, and Trustworthy AI, are encouraged to apply. For more information, please refer to <https://careers.pageuppeople.com/822/lowell/en-us/job/530087/open-rank-tenuretrack-faculty-in-core-ai-miner-school-of-computer-information-sciences>.

Technical University of Munich, Germany

Job Title: Scientific Researcher in Chip Design

Description: The Professorship for Computer Architecture and Operating Systems at TUM Campus Heilbronn covers a broad range of research focus areas in computer architecture, parallel processing and hardware-oriented applications and optimisations as well as operating systems. The main task associated with the position comprises helping in the development organisation of existing and upcoming lab courses and lectures in computer architecture and hardware design in Heilbronn. The lab courses are held in the first and second semester of the master programme, respectively. The research focus can be freely chosen upon agreement with the supervisor, e.g. in educational research. As part of the doctorate, several scientific papers are to be prepared and published. Further tasks include the organisation of related courses as well as the supervision of theses. Please send your complete applications (curriculum vitae, copies of certificates, expert reviews if available) until 15.09.2026 at the latest. For more information, please refer to <https://facultyvacancies.com/scientific-researcher-in-chip-design.i46540.html>.

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