Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 56, No. 8

SIGDA - The Resource for EDA Professionals
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Online archive: https://www.sigda.org/newsletters/

SIGDA News

1. **SEMI Reports 7.4% Rise in Silicon Wafer Shipments**
Global silicon wafer shipments continued their recovery in the second quarter of 2026, with demand from AI applications helping to offset weaker consumer electronics markets.

2. **SK Hynix Posts Record Q2 as AI Memory Demand Drives HBM Growth**
SK hynix has reported its strongest quarterly financial performance to date, with record revenue and profits driven by surging demand for high-performance memory used in AI infrastructure.

3. **Samsung and Broadcom Deepen AI Semiconductor Partnership with $200B Collaboration**
Samsung Electronics and Broadcom have expanded their long-standing relationship with a new strategic agreement covering memory, foundry and advanced packaging technologies aimed at next-generation AI infrastructure.

4. **SK Group and NVIDIA Expand AI Factory and HBM Partnership**
SK Group and NVIDIA have unveiled a strategic partnership worth more than $500 billion aimed at expanding AI infrastructure and next-generation memory technologies.

5. **NVIDIA Expands Agent Toolkit for AI-Driven Chip Engineering**
NVIDIA has expanded its NVIDIA Agent Toolkit with new AI physics and accelerated computing capabilities, aiming to accelerate the adoption of autonomous AI engineers for chip and system design.

6. **NVIDIA Expands Jetson Thor Lineup with T3000 and T2000 Edge AI Modules**
General-purpose robots and autonomous machines are increasingly moving into commercial deployment, driving demand for compact computing platforms that can run advanced AI models locally. NVIDIA has responded by expanding its Jetson Thor family with two new modules aimed at robotics and edge AI applications.

Message from the EiC

Dear SIGDA members,

In this edition, we bring you the latest news and activities in our community, paper deadlines, upcoming conferences, an insightful article on What is Neuromorphic Hardware, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

7. **AMD Unveils Rack-Scale AI Platform and Embedded AI Processors**
AMD has expanded its AI hardware portfolio with a sweeping set of launches aimed at data centres, enterprise systems and robotics, introducing its first rack-scale AI platform alongside new CPUs, GPUs and embedded processors.

8. **NVIDIA and Japan Launch National AI Infrastructure for Robotics**
Japan is moving to build what NVIDIA describes as the world's first national AI infrastructure dedicated to physical AI, combining government support with major industrial and technology partners. The initiative will see Noetra Corp. deploy a large-scale AI factory based on NVIDIA's next-generation Vera Rubin architecture to support AI development across manufacturing, logistics, healthcare, telecommunications and other sectors.

9. **3M and Microsoft Partner on AI Data Center Optics and Enterprise AI**
3M and Microsoft have announced a strategic partnership that combines AI infrastructure with enterprise digital transformation, with Microsoft becoming the first announced hyperscale cloud provider to deploy 3M's Expanded Beam Optical (EBO) technology in Azure data centers.

SIGDA Awards

1. 2026 DAC Under-40 Innovators Award @ DAC 2026
https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

- **Rangharajan Venkatesan,** *Nvidia Corporation, USA*
- **Yibo Lin,** *Peking University, China*
- **Pietro Mercati,** *Intel Corporation, USA*
- **Aydin Aysu,** *North Carolina State University, USA*

2. Marie R. Pistilli Women in Engineering Achievement Award @ DAC 2026
https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

Helen Li
Duke University, USA

3. 2026 Most Influential Paper Award @ DAC 2026
https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

First-order incremental block-based statistical timing analysis

Chandu Visweswariah[1], Kaushik Ravindran[2], Kerim Kalafala[3], Steve G Walker[3], Sambasivan Narayan[4]
[1]CURE100 | [2]Stealth AI Startup | [3]International Business Machines Corporation | [4]Apple Inc., USA

4. SIGDA Pioneering Achievement Award @ DAC 2026
https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

Sachin Sapatnekar
University of Minnesota, USA

SIGDA E-News Editorial Board

5. SIGDA Distinguished Service Award @ DAC 2026
https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

- **Yiran Chen,** *Duke University, USA*
- **Donatella Sciuto,** *Politecnico di Milano, Italy*

6. SIGDA Meritorious Service Award @ DAC 2026
https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

- **Ambar Sarkar,** *NVIDIA Corporation, USA*
- **Andy Pimentel,** *University of Amsterdam, Netherlands*
- **Hussam Amrouch,** *Technical University of Munich, Germany*
- **Ramesh Karri,** *New York University, USA*

7. ACM TODAES Best Paper Award @ DAC 2026
https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

MFIT: Multi-fidelity thermal modeling for 2.5 D and 3D multi-chiplet architectures

Lukas Pfromm[1], Alish Kanani[1], Harsh Sharma[2,4], Parth Solanki[1], Eric Tervo[1], Jaehyun Park[3], • Janardhan Doppa[4], Partha Pratim Pande[4], Umit Ogras[5,1]
[1]University of Wisconsin, Madison, USA | [2]AMD, USA | [3]University of Ulsan, Korea | [4]Washington State University, USA | [5]Samsung Austin Research Center, USA

8. ACM TODAES Rookie Author of the Year (RAY) Award @ DAC 2026
https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

Yequan Zhao
University of California, Santa Barbara, USA

9. ACM TODAES Test of Time Paper Award @ DAC 2026
https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

A detailed power model for field-programmable gate arrays

Kara Poon[1], Steve Wilton[1], Andy Yan[2]
[1]University of British Columbia, Canada| [2]Microsoft, USA

10. ACM SIGDA Outstanding New Faculty Award @ DAC 2026
https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

Zhiyao Xie
The Hong Kong University of Science and Technology, Hong Kong, China

11. ACM SIGDA Outstanding PhD Dissertation Award @ DAC 2026
https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

Tailored Computing: Cross-Layer System, Architecture, and Silicon Co-Design for Physical Intelligence

Zishen Wan,
Georgia Institute of Technology, USA

Paper Deadlines

VLSID'27 – International Conference on VLSI Design & International Conference on Embedded Systems
Bengaluru, India
Deadline: Aug 7, 2026
Jan 2-6, 2027
https://vlsid.org/

ISSCC'27 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA, USA
Deadline: Sept. 9, 2026
Feb. 14-18, 2027
http://isscc.org

ISQED'27 - Int'l Symposium on Quality Electronic Design
San Francisco, CA, USA
Deadline: Sept. 17, 2026
Apr. 14-16, 2027
http://www.isqed.org

ISPD'27 – ACM Int'l Symposium on Physical Design
Taiwan
Abstracts due: Sept. 21, 2026
Deadline: Sept. 28, 2026
Mar 31- Apr. 2, 2027
http://www.ispd.cc/

DATE'27 - Design Automation and Test in Europe
Dresden, Germany
Abstracts due: Sept 13, 2026
Deadline: Sept. 20, 2026
March 22-24, 2027
http://www.date-conference.com

HOST'27 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
Washington DC, USA
(winter submissions)
Abstracts due: Nov. 1, 2025
Deadline: Nov. 8, 2028
May 3-6, 2027
http://www.hostsymposium.org

12. 2026 DAC Best Paper Candidates @ DAC 2026

https://confcats-siteplex.s3.amazonaws.com/dac/images/dac-2026_program_july-22.pdf

- **Adana: Accelerating Large Language Models via Adaptive Nonuniform Asymmetric Quantization**
  Xinkuang Geng, Siting Liu, Hui Wang, Leibo Liu, Jie Han, Honglan Jiang
- **Amoeba: Runtime Tensor Parallel Transformation for LLM Inference Services**
  Haoyu Chen, Xue Li, Kun Qian, Yu Guan, Jin Zhao, Xin Wang
- **ChipModeler: LLM-Aided Reference Model Design for Agile Hardware Verification**
  Jianmin Ye, Yifan Zhang, Tianyang Liu, Qi Tian, Shengchu Su, Lik Tung Fu, Nan Guan, Zhe Jiang, Xi Wang
- **CLUE-ECC: Low-Cost LPDDR6 Reliability Enhancement by Integrating System ECC with On-Die ECC**
  Youngbae Kong, Jae-Youn Hong, Jongwoo Jeon, Junki Lee, Young Jung Kang, Joon-Sung Yang
- **DCTS: Differentiable Clock Tree Synthesis Based on Probabilistic Graphical Model**
  Han Zhang, Junming Jiao, Zhi Li, Qixun Tian, Peng Cao
- **Disentangled Differentiable Timing-Power Co-Optimization with Quad-Gradient Gate Sizing**
  Zixuan Pan, Zizheng Guo, Yufan Du, Runsheng Wang, Yibo Lin
- **DyPamear: Efficient and Scalable Dynamic Graph Pattern Mining on Practical Processing-in-Memory Architecture**
  Yi Zhang, Yu Huang, Deting Chen, Chaoqiang Liu, Haifeng Liu, Xueqi Li, Xiaofei Liao, Hai Jin
- **FLASH3D: A Fast Layered Analytical Solver for High-Accuracy Steady-State Thermal Simulation of 3D ICs**
  Hao Ai, Liang Chen, Jianhua Zhang, Wenxing Zhu
- **LightningFNO: Ultra-Fast Modeling and Inverse Design for Photonic Matrix-Vector Multiplication Computing Units**
  Mingyuan Li, Qisheng Yang, Yichi Zhang, Xiaoxuan Wu, Guochang Lin, Tian-ling Ren
- **Making Sense of Job Preemption for Distributed Deep Learning Acceleration**
  Younghun Go, Changyong Shin, Minchul Kang, Jaehyun Hwang, Chuck Yoo, Gyeongsik Yang
- **Miter-Aware LUT Mapping: Aligning Structure and Solvability for Efficient Logic Equivalence Checking**
  Jiaying Zhu, Zhengyuan Shi, Mengxia Tao, Kezhi Li, Min Li, Qiang Xu
- **Nothing Left to Learn: Isomorphic Graph Transformations for Hardware IP Protection**
  Shaza Elsharief, Lilas Alrahis, Johann Knechtel, Ozgur Sinanoglu
- **Shared Logic Unleashed: Multiple-Node Boolean Optimization for Next-Gen Synthesis**
  Alessandro Tempia Calvino, Anubhaw Xess, Anika Prasad, Jacob Minz, Eleonora Testa, Walter Lau Neto, Alan Mishchenko, Giovanni De Micheli, Patrick Vuillod, Luca Amaru

Upcoming Conferences

ISLPED'26 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
Chicago, IL, USA
Aug. 5-7, 2026
http://www.islped.org

MLCAD'26 - ACM/IEEE Workshop on Machine Learning for CAD
Jeju Island, Korea
Sep. 7-9, 2026
https://mlcad.org/symposium/

VLSI-SoC'26 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Limassol, Cyprus
Oct. 11-14, 2026
http://www.vlsi-soc.com

MICRO'26 – IEEE/ACM Int'l Symposium on Microarchitecture
Athens, Greece
Oct. 31 - Nov. 4, 2026
http://www.microarch.org/micro59

ICCAD'26 – IEEE/ACM Int'l Conference on Computer-Aided Design
San Jose, CA, USA
Nov 8-12, 2026
https://iccad.com/

ICCD'26 – IEEE Int'l Conference on Computer Design
Hong Kong, China
Nov. 16-18, 2026
http://www.iccd-conf.com

FPT'26 - Int'l Conference on Field-Programmable Technology
Honolulu, Hawaii, USA
Dec. 7-10, 2026
http://icfpt.org

13. Best Paper Awards @ GLSVLSI'26
https://glsvlsi.org/awards.html

- **MIBID: Model Based Fault Diagnosis on Ising Machines**
  Nafisa Sadaf Prova, Ahmet Efe, Abhimanyu Kumar, Chris Kim, Sachin S. Sapatnekar, and Ulya R. Karpuzcu (University of Minnesota)
- **MPiCO: Memory-Pool-Based XPU-PIM Cluster over Optical I/O with Load-Imbalance-Aware Assignment and Execution-Site-Matching Mapping Strategies for MoE Inference**
  Zixu Li, Yinyin Lin, Chengchen Wang, Yong Wang, Haidong Tian and Xiankui Xiong (Fudan University and ZTE Cooperation)
- **PiCASO: A Real-time Pi-Integrated Conversational AI System with Optimized LLMs**
  Mahsa Ardakani, Jinendra Malekar and Ramtin Zand (University of South Carolina)

14. Best Poster Awards @ GLSVLSI'26
https://glsvlsi.org/awards.html

- **Adaptive Post-Decoder Memory for Low-Power 360° Video**
  Md Humaun Kabir, Ricardo Mulino, Ali Haidous, Soumya Swaraj Mondal, Dakota Hudson, Md Sajjad Hossain, Na Gong and Hritom Das
- **Multi-Range Communication for Chiplet-Based Systems**
  Arvin Delavari, Amirtha Chandrasekaran and Boris Vaisband

15. Best Paper Awards @ IGSC'26
https://glsvlsi.org/awards.html

- **Advancing Environmental Sustainability in Data Centers via Carbon Depreciation Models**
  Shixin Ji, Zhuoping Yang, Xingzhen Chen, Alex Jones, and Peipei Zhou
- **Revisiting "Cooler is Better": ITD-Aware Per-CPU Thermal Optimization for Sustainable Data Center Operation**
  Jason Crop, Hayden Moore, and Sudeep Pasricha

iSES'26 – IEEE Int'l Symposium on Smart Electronic Systems
Goa, India
Dec. 15-17, 2026
http://www.ieee-ises.org

ASP-DAC'27 - Asia and South Pacific Design Automation Conference
Tokyo, Japan
Jan. 25-28, 2027
http://www.aspdac.com

What is Neuromorphic Hardware?

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The concept of neuromorphic electronic circuits was introduced by Carver Mead in the late 1980s in his seminal book [1]. Since then, neuromorphic computing has evolved into a computing paradigm that seeks to emulate not only the architecture but also the operating principles of biological neural systems. Unlike

conventional deep learning systems, which typically rely on dense synchronous computations, neuromorphic systems process information using sparse asynchronous spike events. Energy efficiency arises from two key factors: the sparse activation of neurons, which reduces unnecessary computation, and spike-driven synaptic integration, where incoming spikes trigger the accumulation of weighted contributions into the neuron state rather than the continuous execution of dense multiply-accumulate operations. The low inference latency property comes from the fact that useful decisions can often be inferred from the first emitted spikes.

The field is advancing quickly in two directions: neuromorphic algorithms and neuromorphic hardware. Neuromorphic algorithms encompass both computational models, such as spiking neural networks (SNNs), and learning algorithms, such as surrogate-gradient-based adaptations of backpropagation [2]. Neuromorphic hardware provides the computing platforms where these computational models are mapped and executed, with the possibility of supporting in-situ and continuous learning. However, to fully exploit the potential energy and latency advantages of neuromorphic computing, specialized hardware architectures are essential.

A first challenge is reducing the data movement inherent to conventional von Neumann architectures, commonly known as the memory wall problem. A key design principle is therefore memory-compute co-location, where synaptic weights and neuron states are stored close to the computational units. A second aspect is avoiding dedicated physical interconnects between every pair of communicating neurons. This is achieved through the Address Event Representation (AER), where a spike event is encoded into a packet containing the neuron address and timing information. These packets are then routed to destination neurons according to the network connectivity, requiring efficient Network-on-Chip architectures.

Today, several design philosophies coexist. Purely analog approaches [1] offer compelling advantages in energy efficiency and latency by exploiting the intrinsic dynamics of electronic circuits, but they also face significant challenges in programmability, precision, and scalability. Mixed-signal implementations are perhaps the most faithful realization of Carver Mead's original vision, with well-known examples including Neurogrid [3], BrainScaleS [4], and DYNAP-SE [5]. These systems use analog circuits for neuron computation and digital circuits for spike communication, programmability, and control. Digital implementations, however, have become the dominant approach for large-scale neuromorphic processors, as they offer excellent scalability, robustness to process, voltage, and temperature variations, compatibility with standard CMOS design flows and EDA tools, and easier verification and reproducibility. Representative examples include large-scale platforms such as SpiNNaker [6], IBM’s TrueNorth [7], and Intel’s Loihi [8]. FPGAs also play an important role in rapid prototyping and hardware/software co-design, providing an attractive balance between flexibility, performance, energy efficiency, and development cost. Examples include Spiker+ [9] and SNN2Bitstream [10]. Emerging architectures exploit memristive and spintronic devices [2], [11]. Naturally, testing and reliability of these specialized neuromorphic chips become primary concerns [12].

Moving forward, several challenges remain: the development of neuromorphic architectures that go beyond today's abstractions and move closer to the original vision of emulating biological computation, hardware-aware training algorithms,

programming software frameworks, mapping and compilation of models onto hardware, benchmarking and evaluation methodologies, design automation, and hardware/algorithm co-design. As neuromorphic hardware, algorithms, and design automation continue to mature together, neuromorphic computing is becoming an increasingly compelling platform for energy-efficient edge intelligence and real-time artificial intelligence.

References:

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[12] S. Raptis and H.-G. Stratigopoulos, "Training Test Inputs for Spiking Neural Network Hardware: A Case Study on the Loihi 2 Neuromorphic Processor," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2026

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES) features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor increased to

2.2 in 2023, more than doubling its value from 2020. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through the best paper and rookie of the year awards. Authors can send their paper submissions to the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Prabhat Mishra, Senior Associate Editor, at prabhat@ufl.edu

Call for Special Issue on Open, Reliable, and Generalizable Datasets for AI in EDA

Submission Deadline: August 31, 2026

For questions and further information, please contact the guest editors:

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SIGDA Vision 2030

ACM SIGDA is launching SIGDA Vision 2030, a community-driven initiative to identify key challenges and define strategic priorities for the Design Automation field.

You can contribute by completing a short survey (5-10 minutes): https://bit.ly/SIGDA-Vision-2030-Survey

The input collected will be discussed in upcoming interactive sessions at major conferences (including DATE, DAC, and ICCAD) and will contribute to a strategic report outlining priorities and concrete actions for the coming years. Your input is extremely valuable in shaping the future of the community.

Technical Activities

1. **As AI Moves from Training to Inference, Optics Moves Closer to the Chip**

Imec researchers argue that co-packaged optics will not be enough for future AI systems, pushing the industry toward 2.5D and eventually 3D optical I/O…

2. **Micro-transfer Printing Advances Heterogeneous Integration for Next-gen Silicon Photonics**

IEEE study highlights micro-transfer printing as a scalable route to enhance silicon photonics for AI and high-speed communications…

3. **Field-Upgradable Hardware Architectures Reshape EV Charger Design**

As EV charging infrastructure expands across India, charger manufacturers face a problem that software updates alone cannot always solve. Charging stations are expected to operate for years despite widely varying grid conditions, differences

in electrical infrastructure and evolving charging standards. Replacing installed hardware every time requirements change can increase both costs and downtime…

4. **Hands-Free Transit Ticketing: The Emerging Role of Wireless Technologies**

Hands-free wireless positioning technologies are transforming transit fare collection by enabling seamless, secure passenger identification without manual validation…

Job Positions

University of Toronto, Canada

Job Title: Assistant Professor of Computer Engineering

Description: The Edward S. Rogers Sr. Department of Electrical and Computer Engineering (ECE) at the University of Toronto invites applications for a full-time tenure stream Assistant Professor position. The successful candidate will conduct transformational research aligned with one or more of the following Canadian strategic priority areas: Advanced digital technologies (Artificial Intelligence, Quantum Technologies, Cybersecurity); Environment, Climate Resilience, and the Arctic. The nominee's research must clearly align with one or more of these strategic priority areas. The appointment is expected to begin on 1 July 2027. For more information, please refer to https://facultyvacancies.com/assistant-professor-of-computer-engineering,i46319.html.

Uppsala University, Sweden

Job Title: Lecturer in Information Technology

Description: Uppsala University is a broad research university with a strong international position. The ultimate goal is to conduct education and research of the highest quality and relevance to make a difference in society. Our most important asset is all of our 7,600 employees and 53,000 students who, with curiosity and commitment, make Uppsala University one of Sweden's most exciting workplaces. The subject area of employment is in Human-Machine Interaction, which is an interdisciplinary subject and focuses on the development and evaluation of methods and tools for constructing computer-based artifacts that support people, organizations and society to achieve their goals. Understanding and formulation of theories on the basic conditions of the interaction process are necessary for the design of successful IT systems. Artificial Intelligence and interaction with advanced technology demand new knowledge and emphasize the need for integrating ethical aspects in the development of computerized artifacts. For more information, please refer to https://facultyvacancies.com/lecturer-in-information-technology,i46359.html.

University of Antwerp, Belgium

Job Title: Postdoctoral Scholarship in Computer Science

Description: The University of Antwerp is a dynamic, forward-thinking, European university. We offer an innovative academic education to more than 20,000 students, conduct pioneering scientific research and play an important service-providing role in society. We are one of the largest, most international and most innovative employers in the region. With more than 6,000 employees from 100 different countries, we are helping to build tomorrow's world every day. Through top scientific research, we push back boundaries and set a course for the future – a future that you can help to shape. You will actively work on the preparation and defence of a PhD thesis in the field of Electronics-ICT: Artificial Intelligence. This PhD project focuses on the development of intelligent control algorithms for inland waterway vessels, using machine learning, with the aim of controlling the vessel in an optimal and efficient manner. In this context, control is formulated as a trade-off between different objectives, such as minimising energy consumption, ensuring smooth vessel operation (without abrupt manoeuvres), complying with regulations, and reaching the destination on time. In addition, the optimal use of hybrid propulsion systems (such as engines and batteries) and other energy consumers on board, such as cargo climate control and hotel loads, is taken into account. The system learns from data and adapts to changing conditions, enabling it to make balanced and sustainable decisions in real time. You will publish scientific articles related to the research project. In addition to project-based research, you will also be responsible for a limited range of support tasks related to teaching and/or research management within the Department of Electronics and Information and Communication Technology. For more information, please refer to https://facultyvacancies.com/postdoctoral-scholarship-in-computer-science,i46326.html.

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