Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 56, No. 5

SIGDA - The Resource for EDA Professionals
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Online archive: https://www.sigda.org/newsletters/

SIGDA News

1. **NVIDIA and Google Cloud Target Physical AI Factories**
NVIDIA and Google Cloud have expanded their long-running partnership with a set of announcements at Google Cloud Next 2026 that tie new GPU infrastructure, confidential computing, and Google's reworked enterprise agent stack into a broader push towards physical AI factories.

2. **Siemens and TSMC Expand AI-Driven Chip Design Collaboration**
Siemens and TSMC are deepening their collaboration to push AI-powered automation across semiconductor design workflows. The move builds on an existing partnership and focuses on accelerating advanced node development and improving design efficiency using AI.

3. **Musk Teams with Intel for Terafab Plans**
Elon Musk has ambitious plans for the semiconductor industry. To secure the supply chain for AI chips for his companies, Tesla, SpaceX, and xAI, he is proposing a series of fabs, the Terafab, that will provide a terawatt of processing performance a year in the next decade.

4. **TSMC SoIC Roadmap Targets 2029 Chip Stacking**
TSMC is pushing its 3D chip-stacking roadmap towards finer interconnect pitches and tighter integration as advanced packaging becomes a larger part of performance scaling for AI and high-performance computing designs.

5. **SK Hynix Begins Mass Production of 192GB AI Server Memory**
SK hynix has started mass production of a 192GB SOCAMM2 memory module, targeting next-generation AI servers and setting the stage for higher-performance, lower-power infrastructure.

6. **Omdia Raises 2026 Semiconductor Forecast to 62.7%**
The global semiconductor market is heading for a blockbuster 2026, with Omdia sharply raising its revenue growth forecast to 62.7%. The revision reflects surging demand for memory chips, particularly DRAM and NAND, as AI workloads continue to reshape infrastructure needs.

Message from the EiC

Dear SIGDA members,

In this edition, we bring you the latest news and activities in our community, paper deadlines, upcoming conferences, an insightful article on What is a Native Differential Privacy Accelerator, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

7. SiFive Funding Backs Datacentre CPU Push

SiFive has raised $400 million in an oversubscribed Series G round as it steps up its push into datacenter CPU IP, with Atreides Management leading the round and Nvidia among the investors. The financing values the Santa Clara company at $3.65 billion and, according to Reuters, CEO Patrick Little sees it as potentially the company's last private round before an IPO.

8. MATCH Act Targets Chip Tool Exports to China

A bipartisan US bill aimed at tightening semiconductor export controls on China is moving through the House Foreign Affairs Committee, with lawmakers seeking to give the restrictions more force in statute rather than leaving so much discretion with the Commerce Department's Bureau of Industry and Security.

SIGDA Awards

1. *ISPD Best Paper Award @ ISPD 2026*

https://ispd.cc/ispd2026/index.php?page=program

Gradient-Guided RC Weighting for Timing-Driven Global Routing[1]

Liang Xiao, Qinkai Duan, Leilei Jin, Jinwei Liu, Tsung-Yi Ho, Evangeline F.Y. Young and Martin Wong
The Chinese University of Hong Kong

2. *EDAA Achievement Award 2026 @ DATE 2026*

https://www.date-conference.com/awards

Krishnendu Chakrabarty

Arizona State University, US

3. *IEEE CEDA Outstanding Service Recognition Award 2026 @ DATE 2026*

https://www.date-conference.com/awards

Aida Todri-Sanial
Eindhoven University of Technology, NL

4. *IEEE CEDA Distinguished Service Award 2026 @ DATE 2026*

https://www.date-conference.com/awards

David Atienza,
EPFL, CH

5. *IEEE CS TTTC Outstanding Contribution Award 2026 @ DATE 2026*

https://www.date-conference.com/awards

Valeria Bertacco, *University of Michigan, US*
Wolfgang Müller, *Paderborn University, DE*

SIGDA E-News Editorial Board

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[1] We deeply regret the error in ISPD Best Paper Award @ ISPD 2026 published in the previous issue. The paper mentioned here is the Best Paper Award Winner. The same has been corrected in the April edition of the eNewsletter published on the website.

6. *SIGDA Outstanding New Faculty Award 2026 @ DATE 2026*

https://www.date-conference.com/awards

Meng Li
Assistant Professor,
Peking University, CN

7. *DATE Best Paper Award @ DATE 2026*

https://www.date-conference.com/awards

1. D_low Track - Design Methods and Tools:

   FSDB: A Folded-Store Dynamic-Broaden Hybrid Compute-In-Rom/Sram Architecture For Deploying Large-Scale DNNs On-Chip

   Tianyi Yu, Teng Yi, Huazhong Yang, Xueqing Li
   Department of Electronic Engineering, LFET/BNRist/SKLSNC, Tsinghua University

2. D_high track - Design Methods and Tools:

   TORRENT: A Distributed DMA For Efficient And Flexible Point-To-Multipoint Data Movement

   Yunhao Deng, Fanchen Kong, Xiaoling Yi, Ryan Antonio, Marian Verhelst
   MICAS-ESAT, KU Leuven

3. A Track - Application Design

   INSPIRE: In-Sensor Compressed Weight Retrieval For Enhancing Vit Efficiency At Edge

   Sabbir Ahmed[1], Deniz Najafi[2], Mohaiminul Al Nahian[1], Navid Khoshavi[3], Abdullah Al Arafat[4], Mamshad Nayeem Rizve[5], Mahdi Nikdast[6], Adnan Siraj Rakin[7] and Shaahin Angizi[2]
   1Binghamton University (SUNY), US; [2]New Jersey Institute of Technology, US; [3]AMD, US; [4]Florida International University, US; [5]Adobe, US; [6]Colorado State University, US; [7]Binghamton University, US

4. T Track - Test and Dependability

   RIFT: A Scalable Methodology for LLM Accelerator Fault Assessment using Reinforcement Learning

   Khurram Khalil, Muhammad Mahad Khaliq and Khaza Anuarul Hoque,
   University of Missouri, US

5. T Track - Test and Dependability

   KirbyMM: Outer-Product Based Matrix Multiplication on ARMv9 Processor

   LanshuHuang, Han Huang, ZhiguangChen and Yutong Lu Sun
   Yat-sen University, CN

Paper Deadlines

ICCD'26 – IEEE Int'l Conference on Computer Design
Hong Kong, China
Abstracts due: May 15, 2026
Deadline: May 22, 2026
Nov. 16-18, 2026
http://www.iccd-conf.com

MLCAD'26 - ACM/IEEE International Symposium on Machine Learning for CAD
Jeju Island, Korea
Abstracts due: May 16, 2026
Deadline: May 23, 2026
Sep. 7-9, 2026
https://mlcad.org/symposium

iSES'26 – IEEE Int'l Symposium on Smart Electronic Systems
Goa, India
Deadline: June 6, 2026
Dec. 15-17, 2026
http://www.ieee-ises.org

ASP-DAC'27 - Asia and South Pacific Design Automation Conference
Tokyo, Japan
Abstracts due: July 3, 2026
Deadline: July 10, 2026
Jan. 25-28, 2027
http://www.aspdac.com

8. *PhD Forum Best Poster Award @ DATE 2026*

https://www.date-conference.com/awards

Side-Channel Awareness in Neural Network FPGA Accelerators: Security Threats and Opportunities for Functional Safety

Vincent Meyers,
Karlsruhe Institute of Technology, DE

Generative AI in the Hardware Design Flow: from High-Level Synthesis to Security

Luca Collini,
New York University, US

9. *EDAA Outstanding Dissertation Awards @ DATE 2026*

https://www.date-conference.com/awards

1. Topic 1 - New directions in systems design methods and tools, simulation and validation, embedded software design and optimization for embedded, cyber-physical, secure and learning systems

Learning-Based Methods for Enabling On-Edge, Accurate, Sustainable, and Human Centered Intelligent Manufacturing

Luigi Capogrosso, *Politecnico Di Torino, IT*
Advisors: Marco Cristani, Franco Fummi

2. Topic 2 - New directions in SoC platforms co-design, novel architectures for future computing in design flows, and power management

AI-driven Design and Optimization of Heterogeneous ChipletSystems for Server-Scale AI Workloads

Harsh Sharma*, Washington State University, US*
Advisors: Partha Pande, Jana Doppa

3. Topic 3 New directions in logic, physical design and CAD for analog/mixed-signal,nano-scale and emerging technologies

Equality Saturation for Circuit Synthesis and Verification

Samuel Coward*, Imperial College London, UK*
Advisor: George Constantinides

4. Topic 4 New directions in safety, reliability and security-aware hardware design, validation and test

Hardware-Firmware Security Co-Verification

Aruna Jayasena*, University of Florida, US*
Advisor: Prabhat Mishra

10. *SIGDA PhD Dissertation Award 2026 @ DATE 2026*

https://www.date-conference.com/awards

Upcoming Conferences

FCCM' 26 - IEEE International Symposium On Field-Programmable Custom Computing Machines
Atlanta, GA, USA
May 13-16, 2026
https://www.fccm.org

MDTS'26 – IEEE Microelectronics Design & Test Symposium
Albany, NY, USA
May 18-20, 2026
http://natw.ieee.org

RTAS'26 - IEEE Real-Time and Embedded Technology and Applications Symposium
Saint Malo, France
May 12-14, 2026
http://2026.rtas.org

ISCAS'26 – IEEE Int'l Symposium on Circuits and Systems
Shanghai, China
May 24-27, 2026
https://2026.ieee-iscas.org

IWLS'26 - International Workshop on Logic & Synthesis
Hong Kong, China
May 29-31, 2026
https://www.iwls.org

GLSVLSI'26 - ACM Great Lakes Symposium on VLSI
Finger Lakes, NY, USA
June 22-24, 2026
http://www.glsvlsi.org

ICECET'26 - IEEE International Conference on Electrical, Computer and Energy Technologies
Rome, Italy
July 6-9, 2026
www.icecet.com

Technology Mapping and Optimization Algorithms for Logic Synthesis of Advanced Technologies

Alessandro Tempia Calvino, *École Polytechnique Fédérale de Lausanne, CH*
Advisor: Giovanni De Micheli

11. Outstanding Reviewer Awards @ DATE 2026

https://www.date-conference.com/awards

1. D Track
   - **Lorenzo Ferretti**, *Micron Technology, US*
   - **Siting Liu**, *ShanghaiTech University, CN*
   - **Yukai Chen**, *IMEC, BE*
   - **Nicoleta Cucu Laurenciu**, *Radboud University, NL*

2. A Track
   - **Bahar Farahani**, *Shahid Beheshti University, IR*
   - **Jo Vliegen**, *KU Leuven, BE*

3. T Track
   - **Mohammad Hasan Ahmadilivani**, *Tallinn University of Technology, EE*
   - **Johann Knechtel**, *New York University Abu Dhabi, AE*

4. E Track
   - **BaekGyu Kim**, *Daegu Gyeongbuk Institute of Science & Technology, KR*
   - **Yasmina Abdeddaim**, *University Gustave Eiffel, CNRS, LIGM, FR*

What is a Native Differential Privacy Accelerator?

Contributing authors: Muhammad Hamis Haider <hamis.haider@usask.ca> and Seokbum Ko <seokbum.ko@usask.ca>, Department of Electrical and Computer Engineering, University of Saskatchewan, Canada
AE: Alberto Marchisio <alberto.marchisio@nyu.edu>

A native differential privacy accelerator is specialized hardware that is designed to support differential privacy as a built-in part of the system, rather than adding privacy later through software. Differential privacy (DP) is a mathematical framework that limits how much information about any single individual can be learned from the output of a computation [1].

In machine learning, DP is most applied using differentially private stochastic gradient descent (DP SGD). DP SGD works by limiting the influence of each training example through gradient clipping and then adding carefully calibrated noise before updating the model [2], [3]. This approach allows machine learning models to be trained with formal privacy guarantees by ensuring that individual training samples do not significantly affect the final result.

The need for native hardware support comes from practical challenges. Compared with standard training, DP SGD introduces additional steps, including

ISVLSI'26 – IEEE Computer Society Annual Symposium on VLSI
Kolkata, India
July 7-10, 2026
http://www.ieee-isvlsi.org

DAC'26 – Design Automation Conference
Long Beach, CA, USA
July 26-29, 2026
http://www.dac.com

ICLAD'26 - IEEE International Conference on LLM-Aided Design
Standford, CA, USA
July 30-31, 2026
https://iclad.ai

ISLPED'26 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
Chicago, IL, USA
Aug. 5-7, 2026
http://www.islped.org

MICRO'26 – IEEE/ACM Int'l Symposium on Microarchitecture
Athens, Greece
Abstracts due: Mar. 31, 2026
Deadline: Apr. 7, 2026
Oct. 31 - Nov. 4, 2026
http://www.microarch.org/micro59

VLSI-SoC'26 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Limassol, Cyprus
Abstracts due: Apr. 20, 2026
Deadline: Apr. 27, 2026
Oct. 11-14, 2026
http://www.vlsi-soc.com

ICCAD'26 – IEEE/ACM Int'l Conference on Computer-Aided Design
San Jose, CA, USA
Abstracts due: Apr. 7, 2026
Deadline: Apr 14, 2026
Nov 8-12, 2026
https://iccad.com

for example gradient computation, clipping, noise generation, and privacy accounting. These operations increase memory movement and reduce the efficiency of conventional accelerators, which are typically optimized for standard mini batch training [3], [4]. NIST has also pointed out that private training is difficult to map efficiently onto existing hardware because for example processing limits common matrix based optimizations [5].

A native differential privacy accelerator addresses these challenges by integrating key privacy related operations directly into the hardware's data path or control logic. Current research includes accelerators specifically designed for DP SGD, such as DiVa, which focuses on addressing the memory and utilization bottlenecks seen in private training [4]. Other work proposes hardware mechanisms that help enforce privacy requirements, such as DPWatch, which monitors whether gradients have been properly noised before they are allowed to leave the device [6]. In this context, “native” means that privacy is treated as a core architectural requirement rather than just an optional algorithm implemented in software.

This area of research is still developing, and the term “native differential privacy accelerator” is not yet widely standardized in the literature. However, the trend is clear. As differential privacy moves from theoretical work toward deployment in real machine learning systems, hardware support is becoming increasingly important for reducing overhead, improving energy efficiency, and increasing confidence that privacy critical steps are executed correctly [3]–[6].

References:

[1] C. Dwork and A. Roth, The Algorithmic Foundations of Differential Privacy. Hanover, MA, USA: Now Publishers, 2014.
[2] M. Abadi, A. Chu, I. Goodfellow, H. B. McMahan, I. Mironov, K. Talwar, and L. Zhang, “Deep learning with differential privacy,” in Proc. ACM SIGSAC Conf. Comput. Commun. Secur. (CCS), Vienna, Austria, 2016, pp. 308-318.
[3] M. H. Haider, N. -j. Kim, H. Zhang, J. Arias-Garcia, H. -J. Lee and S. -b. Ko, "Memory-Efficient Differential Privacy Accelerator," 2025 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Busan, Korea, Republic of, 2025, pp. 1-5, doi: 10.1109/APCCAS67402.2025.11378315.
[4] B. Park, R. Hwang, D. Yoon, Y. Choi, and M. Rhu, “DiVa: An accelerator for differentially private machine learning,” in Proc. 55th IEEE/ACM Int. Symp. Microarchitecture (MICRO), Chicago, IL, USA, 2022.
[5] N. Papernot and A. G. Thakurta, “How to deploy machine learning with differential privacy,” NIST, Dec. 21, 2021.
[6] P. K. Sanjaya et al., “DPWatch: A framework for hardware-based differential privacy guarantees,” IEEE Comput. Archit. Lett., vol. 24, no. 1, pp. 89-92, 2025.

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES) features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor increased to

2.2 in 2023, more than doubling its value from 2020. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through the best paper and rookie of the year awards. Authors can send their paper submissions to the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Prabhat Mishra, Senior Associate Editor, at prabhat@ufl.edu

Call for Special Issue on Advances in Physical Design Automation
Submission Deadline: July 7, 2026
For questions and further information, please contact the guest editors at:
- Rickard Ewetz, rewetz@ufl.edu
- Tung-Chieh Chen, donchen@synopsys.com
- Stephan Held, held@dm.uni-bonn.de
- Gracieli Posser, gposser@cadence.com

Call for Special Issue on Open, Reliable, and Generalizable Datasets for AI in EDA
Submission Deadline: August 31, 2026
For questions and further information, please contact the guest editors:
- Qi Sun, Zhejiang University, qisunchn@zju.edu.cn
- Tsung-Yi Ho, The Chinese University of Hong Kong, tyho@cse.cuhk.edu.hk
- Grace Li Zhang, TU Darmstadt, grace.zhang@tu-darmstadt.de
- Haoyu Yang, NVIDIA, haoyuy@nvidia.com

SIGDA Vision 2030

ACM SIGDA is launching SIGDA Vision 2030, a community-driven initiative to identify key challenges and define strategic priorities for the Design Automation field.

You can contribute by completing a short survey (5-10 minutes): https://bit.ly/SIGDA-Vision-2030-Survey

The input collected will be discussed in upcoming interactive sessions at major conferences (including DATE, DAC, and ICCAD) and will contribute to a strategic report outlining priorities and concrete actions for the coming years. Your input is extremely valuable in shaping the future of the community.

Technical Activities

1. Humanoid Robots Hit the Factory Floor

Backed by big tech and billion-dollar venture funds, humanoid robots have reached manufacturing lines. Success now hinges on power, production-level reliability, and real-world data streams…

2. **Game, Set, Bot: Sony AI’s ‘Ace’ Serves Up a Defeat to Table Tennis Pros**

Codenamed “Ace,” Sony AI claims the system represents the first instance of a robot reaching human, expert-level performance in a competitive physical sport…

3. **Intel and Vietnam’s FPT Partner to Deliver AI-driven Digital Manufacturing Platform for Autonomous Factory Optimization**

Intel Corp. and Vietnam’s FPT Corp. have formed a strategic collaboration to deliver an end-to-end AI-driven factory optimization solution. The initiative integrates AI, simulation, and digital manufacturing technologies to reduce bottlenecks, accelerate decision-making, and improve downtime recovery, supporting the transition toward autonomous factory operations…

4. **Cisco’s Universal Quantum Switch Ushers in Quantum Networking**

Cisco has unveiled the working prototype of a switch designed to transmit and relay quantum information between systems from different vendors, enabling interoperability…

Job Positions

The Ramaiah Institute of Science and Management, India

Job Title: Faculty Positions in Engineering, Sciences and Technology

Description: We seek passionate educators and accomplished researchers who aspire to: Deliver transformative education and design innovative curricula; Build globally visible research programs, secure competitive funding; Publish in leading journals and engage with international academic communities; Mentor the next generation of engineers, scientists, and innovators; Collaborate with world-class universities and industry partners. For more information, please refer to https://facultyvacancies.com/faculty-posiitons-in-engineering-sciences-and-technology,i44759.html.

Lund University, Sweden

Job Title: Postdoctoral Students in Electrical Engineering

Description: As a doctoral student, you are both admitted as a student and employed at Lund University. You will be trained in a scientific approach, including critical thinking, independent problem-solving, and research ethics awareness. You will also develop leadership and pedagogical skills under supervision. Doctoral studies end with a thesis and a doctoral degree. The primary duties of the doctoral student position are to perform research and teaching within the computer security area. The research focuses on security for dynamic resource allocation in next-generation mobile networks. Key topics include: Verification of target resources in dynamic execution environments; New principles and protocols for execution target verification; Protected execution environments such as Intel TDX and AMD SEV; Side-channel risks in confidential computing environments; Side-channel attacks on dynamically allocated tasks;

Security of resource allocation functions and related attacks/defences. The research method includes system studies, simulations, and experimental research. The project is a collaboration with Linköping University. For more information, please refer to https://facultyvacancies.com/postdoctoral-students-in-electrical-engineering,i45576.html.

University of Antwerp, Belgium

Job Title: Postdoctoral Scholarship in Electronics Engineering

Description: The Department of Electrical and ICT Engineering Technology in the Faculty of Applied Engineering is looking for a full-time (100%) doctoral scholarship holder in the field of neural representations of medium distortions in multi-modal robotic simulations. The position is within the Cosys-lab research group, under supervision of prof. Jan Steckel and prof. Walter Daems. You will work actively on the preparation and defence of a PhD thesis that is part of the Flanders Make project Harmony. In this project, we will work on the implementation of the simulation of realistic medium distortions in robotic perception simulations. Indeed, dust, fog, rain, etc have a tremendous impact on the perceived data in cameras, lidars, radar and sonar sensors. In this project, we will develop an approach to simulate these medium distortions based on neural BRDF representations. You will publish scientific articles related to the research project. You will collaborate closely with other PhD students in the team and external partners in the SBO project. You will carry out a limited number of teaching and research support tasks for courses related to Cyber-physical systems, electronics lab work or applied image/data processing. You can apply for this vacancy through the University of Antwerp's online job application platform up to and including 18 May 2026 (by midnight Brussels time). For more information, please refer to https://facultyvacancies.com/postdoctoral-scholarship-in-electronics-engineering,i45562.html.

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