Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 56, No. 4

**SIGDA - The Resource for EDA Professionals**

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.

Online archive: https://www.sigda.org/newsletters/

# SIGDA News

1. **EU Invests €330M to Fast-Track Fusion and Nuclear Innovation**
The European Commission has unveiled a €330 million investment package aimed at accelerating fusion energy and strengthening nuclear technologies under its 2026–2027 Euratom Research and Training Programme. The initiative is designed to complement Horizon Europe while reinforcing Europe's long-term energy strategy.

2. **Infineon, NVIDIA Accelerate Humanoid Robots Using Digital Twins**
Infineon and NVIDIA are deepening their collaboration around humanoid robots, combining semiconductor platforms with AI and simulation technologies. The focus is on enabling faster and potentially safer deployment of robots using digital twins and integrated system architectures.

3. **NVIDIA Pushes Physical AI into Real-World Robotics Deployments**
NVIDIA is doubling down on "physical AI," unveiling new simulation frameworks and foundation models while expanding partnerships with major robotics players to accelerate real-world deployments. Announced at GTC, the move highlights how AI-driven robotics is shifting from experimentation to production.

4. **Quantum Machines Unveils Open Stack for Quantum Acceleration**
Quantum Machines has launched a new open framework designed to bridge quantum processors with high-performance classical computing systems. Developed in collaboration with NVIDIA, AMD, and Riverlane, the Open Acceleration Stack aims to accelerate the shift toward scalable, hybrid quantum architectures.

5. **Broadcom Launches Symantec CBX XDR Security Platform**
Broadcom has unveiled Symantec CBX, a new cloud-based extended detection and response (XDR) platform designed to bring enterprise-level security capabilities to organizations with limited security operations resources. The platform combines technologies from the Symantec and Carbon Black portfolios into a single integrated solution.

# Message from the EiC

Dear SIGDA members,

In this edition, we bring you the latest news and activities in our community, upcoming conferences, paper deadlines, an insightful article on What is Adversarial Circuit Rewriting, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

*Sandeep Chandran,*
Editor-in-Chief,
SIGDA e-Newsletter

6. **Arduino VENTUNO Q and AI Prototyping at Embedded World 2026**
At Embedded World 2026, Brian Tristam Williams (Elektor) spoke with Manny Singh at the Qualcomm booth about how Qualcomm is bringing together Arduino, Edge Impulse, and its broader developer strategy to simplify AI and robotics development at the edge.

7. **TI 800 VDC Architecture Targets AI Data Centres**
Texas Instruments has outlined a full power-delivery approach for next-generation AI data centres, built around NVIDIA's emerging 800 VDC rack and facility design. The move is aimed at one of the more awkward problems in AI infrastructure right now: getting ever larger amounts of power into compute trays and GPU clusters without wasting too much of it as heat, copper, and conversion overhead.

8. **SK Hynix Warns Memory Shortage Could Last Up to 2030**
SK hynix chairman Chey Tae-won says the current memory squeeze may last another four to five years, extending a supply crunch that has already pushed up prices and tightened availability across the electronics sector.

# SIGDA Awards

***1. ISFPGA Best Paper Award @ ISFPGA 2026***
https://www.isfpga.org/program/

**KANELÉ: Kolmogorov-Arnold Networks for Efficient LUT-based Evaluation**

*Duc Hoang, Aarush Gupta, Philip C Harris*

Massachusetts Institute of Technology

***2. ISPD Best Paper Award @ ISPD 2026***
https://ispd.cc/ispd2026/index.php?page=program

**"Gradient-Guided RC Weighting for Timing-Driven Global Routing"**

*Liang Xiao, Qinkai Duan, Leilei Jin, Jinwei Liu, Tsung-Yi Ho, Evangeline F.Y. Young and Martin Wong*

The Chinese University of Hong Kong

# What is Adversarial Circuit Rewriting?

**Contributing author:** Lilas Alrahis <lilas.malrahis@ku.ac.ae>
Assistant Professor, Computer and Information Engineering, Khalifa University
**AE:** Alberto Marchisio <alberto.marchisio@nyu.edu>

# SIGDA E-News Editorial Board

Machine learning (ML), and in particular graph-based learning models such as graph neural networks (GNNs), have demonstrated state-of-the-art performance in analyzing hardware circuits. Since circuits can naturally be represented as graphs, GNNs can learn embedding representations that capture both structural and functional properties of circuits. These learned representations have been successfully applied to solve a wide range of problems in electronic design automation (EDA), hardware security, and hardware reliability [1].

In hardware security, GNNs have been used to address critical tasks such as hardware Trojan detection. Hardware Trojans are malicious circuit modifications introduced to leak secret assets or disrupt circuit functionality. Such Trojans often leave structural and functional footprints in the design. As a result, GNNs have proven effective at detecting these patterns. GNN-based methods have also been used for functional reverse engineering, where high-level modules are identified from gate-level netlists containing millions of gates [2].

However, the ML community has demonstrated that GNNs are vulnerable to adversarial and poisoning attacks. In adversarial attacks, graphs are deliberately modified, by adding or removing nodes, edges, or features, to cause a GNN to misclassify the input [3].

Adversarial circuit rewriting brings this concept into the hardware domain. Instead of modifying abstract graph structures, it alters real circuits by adding or removing wires, inserting or deleting gates, or changing gate types in a controlled manner to evade detection systems, particularly those targeting malicious constructs such as hardware Trojans.

Unlike standard adversarial attacks on graph data, adversarial circuit rewriting is significantly more complex. Circuit perturbations must obey strict design rules, timing constraints, and functional correctness requirements. Modifications are therefore governed by logic equivalence and synthesis constraints, which significantly restrict the allowable perturbations. Nevertheless, such attacks are feasible and represent an important and emerging research direction.

Existing research often leverages logic synthesis tools to perform functionality-preserving optimizations while strategically selecting circuit locations for modification [4]. Techniques such as reinforcement learning have been used to identify rewrite locations [5], and more recently, large language models have been explored for guiding transformation strategies.

Adversarial circuit rewriting lies at the intersection of hardware design, ML, and security, and opens up compelling research questions about robustness, trust, and resilience in ML-driven EDA workflows.

**References:**

[1] Z. El Sayed, Z. Wang, H. Selmani, J. Knechtel, O. Sinanoglu, and L. Alrahis, “Graph neural networks for integrated circuit design, reliability, and security: survey and tool,” ACM Comput. Surv., vol. 58, no. 4, Art. no. 102, Mar. 2026,
[2] L. Alrahis, S. Patnaik, M. Shafique, and O. Sinanoglu, “Embracing graph neural networks for hardware security,” in 41st IEEE/ACM Int. Conf. Computer-Aided Design (ICCAD), 2022, pp. 1–9.
[3] D. Zügner, O. Borchert, A. Akbarnejad, and S. Günnemann, “Adversarial attacks on graph neural networks: perturbations and their patterns,” ACM Trans. Knowl. Discov. Data, vol. 14, no. 5, Art. no. 57, Oct. 2020, 31 pp., doi: 10.1145/3394520.
[4] A. B. Chowdhury, L. Alrahis, L. Collini, J. Knechtel, R. Karri, S. Garg, O. Sinanoglu, and B. Tan, “ALMOST: Adversarial learning to mitigate oracle-less ML attacks via synthesis tuning,” in ACM/IEEE Design Automation Conf. (DAC), 2023, pp. 1–6.

# Paper Deadlines

**MICRO’26 – IEEE/ACM Int'l Symposium on Microarchitecture**
Athens, Greece
Abstracts due: Mar. 31, 2026
Deadline: Apr. 7, 2026
Oct. 31 - Nov. 4, 2026
http://www.microarch.org/micro59

**VLSI-SoC’26 – IFIP/IEEE Int’l Conference on Very Large Scale Integration**
Limassol, Cyprus
Abstracts due: Apr. 20, 2026
Deadline: Apr. 27, 2026
Oct. 11-14, 2026
http://www.vlsi-soc.com

**ICCAD’26 – IEEE/ACM Int’l Conference on Computer-Aided Design**
San Jose, CA, USA
Abstracts due: Apr. 7, 2026
Deadline: Apr 14, 2026
Nov 8-12, 2026
https://iccad.com

**ICCD’26 – IEEE Int’l Conference on Computer Design**
Hong Kong, China
Abstracts due: May 15, 2026
Deadline: May 22, 2026
Nov. 16-18, 2026
http://www.iccd-conf.com

**MLCAD'26 - ACM/IEEE International Symposium on Machine Learning for CAD**
Jeju Island, Korea
Abstracts due: May 16, 2026
Deadline: May 23, 2026
Sep. 7-9, 2026
https://mlcad.org/symposium

**iSES’26 – IEEE Int’l Symposium on Smart Electronic Systems**
Goa, India

[5] V. Gohil, S. Patnaik, D. Kalathil, and J. Rajendran, “AttackGNN: Red-teaming GNNs in hardware security using reinforcement learning,” in Proc. 33rd USENIX Security Symposium (USENIX Security ’24), Philadelphia, PA, USA, Aug. 2024, pp. 73–90.

# SIGDA Partner Journal

**ACM Transactions on Design Automation of Electronic Systems (TODAES)** features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor increased to 2.2 in 2023, more than doubling its value from 2020. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through the best paper and rookie of the year awards. Authors can send their paper submissions to the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Prabhat Mishra, Senior Associate Editor, at prabhat@ufl.edu

**Call for Special Issue on Advances in Physical Design Automation**
**Submission Deadline: July 7, 2026**
For questions and further information, please contact the guest editors at:
• Rickard Ewetz, rewetz@ufl.edu
• Tung-Chieh Chen, donchen@synopsys.com
• Stephan Held, held@dm.uni-bonn.de
• Gracieli Posser, gposser@cadence.com

**Call for Special Issue on Open, Reliable, and Generalizable Datasets for AI in EDA**
**Submission Deadline: August 31, 2026**
For questions and further information, please contact the guest editors:
• Qi Sun, Zhejiang University, qisunchn@zju.edu.cn
• Tsung-Yi Ho, The Chinese University of Hong Kong, tyho@cse.cuhk.edu.hk
• Grace Li Zhang, TU Darmstadt, grace.zhang@tu-darmstadt.de
• Haoyu Yang, NVIDIA, haoyuy@nvidia.com

## SIGDA Vision 2030

ACM SIGDA is launching SIGDA Vision 2030, a community-driven initiative to identify key challenges and define strategic priorities for the Design Automation field.

You can contribute by completing a short survey (5-10 minutes): https://bit.ly/SIGDA-Vision-2030-Survey

The input collected will be discussed in upcoming interactive sessions at major conferences (including DATE, DAC, and ICCAD) and will contribute to a strategic report outlining priorities and concrete actions for the coming years. Your input is extremely valuable in shaping the future of the community.

Deadline: June 6, 2026
Dec. 15-17, 2026
http://www.ieee-ises.org

**ASP-DAC'27 - Asia and South Pacific Design Automation Conference**
Tokyo, Japan
Abstracts due: July 3, 2026
Deadline: July 10, 2026
Jan. 25-28, 2027
http://www.aspdac.com

## ACM/SIGDA Pioneering Achievement Award

The ACM/SIGDA Pioneering Achievement Award honors an individual for lifetime, outstanding contributions within the scope of electronic design automation. These contributions may be evidenced by pioneering ideas introduced through publications, industrial products, or other significant achievements. The award recognizes the enduring impact of the nominee's contributions over the course of their career.

**Eligibility**
The award is open to researchers in the field of electronic design automation who have made outstanding lifetime contributions to the field. Current members of the ACM SIGDA Executive Committee or members of the Award Selection Committee are not eligible for the award. The awardee is typically invited to present a lecture at ICCAD.

**Award Items**
The award consists of a plaque, a citation, and a USD 1,000 honorarium. The honorarium is funded by the SIGDA annual budget.

**Nominee Solicitation**
The call for nominations is typically announced via email to SIGDA members, posted on the ACM SIGDA website, and advertised in the SIGDA newsletter. Nominations must be submitted by someone other than the nominee.

A complete nomination package should include the following:

- A nomination letter containing:
  - A concise 100-word summary describing the nominee's contributions and their overall impact
  - A detailed description of up to ten major products, such as papers, patents, or software, explaining the contributions embodied in these works and their impact
  - A list of up to ten citations corresponding to the major products discussed
- Up to three letters of recommendation, excluding letters from the nominator or the nominee
- Contact information for the nominator
- Biographical information for the nominee, including education and employment history, professional activities, publications, and prior recognition
- Up to three additional endorsements attesting to the impact of the nominee's work

All standard conflict-of-interest regulations as defined by ACM policy apply. Members of the Award Selection Committee will recuse themselves from consideration of any nomination where a conflict of interest exists.

The submission deadline for the 2026 ACM/SIGDA Pioneering Achievement is the **10th April 2026**. Please email the nomination to sigda.awards@acm.org.

**Selection and Basis for Judging**
This award honors an individual who has made outstanding technical contributions within the scope of electronic design automation over the course of their lifetime. Selection is based on the breadth, depth, and sustained impact of the nominee's contributions. Nominees from academia, industry, and government worldwide are eligible and encouraged.

# Upcoming Conferences

**ISQED'26 - Int'l Symposium on Quality Electronic Design**
San Francisco, CA, USA
Apr. 8-10, 2026
http://www.isqed.org

**DATE'26 - Design Automation and Test in Europe**
Verona, Italy
Apr. 20-22, 2026
http://www.date-conference.com

**HOST'26 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust**
Washington DC, USA
May 4-7, 2026
http://www.hostsymposium.org

**FCCM' 26 - IEEE International Symposium On Field-Programmable Custom Computing Machines**
Atlanta, GA, USA
May 13-16, 2026
https://www.fccm.org

**MDTS'26 – IEEE Microelectronics Design & Test Symposium**
Albany, NY, USA
May 18-20, 2026
http://natw.ieee.org

**RTAS'26 - IEEE Real-Time and Embedded Technology and Applications Symposium**
Saint Malo, France
May 12-14, 2026
http://2026.rtas.org

**ISCAS'26 – IEEE Int'l Symposium on Circuits and Systems**
Shanghai, China
May 24-27, 2026
https://2026.ieee-iscas.org

This is not a best-paper or single-contribution award. Rather, it recognizes lifetime achievement and long-term influence on the EDA field.

**Presentation**
The ACM/SIGDA Pioneering Achievement Award is presented annually at the Design Automation Conference (DAC) and is also recognized at the SIGDA Annual Member Meeting and Dinner at ICCAD.

## ACM Outstanding Ph.D. Dissertation Award in Electronic Design Automation (OPDA)

Design automation has gained widespread acceptance within the VLSI circuits and systems design community. Continued advances in computer-aided design methodologies, algorithms, and tools are essential to addressing rapidly increasing design complexity, rising performance and energy-efficiency demands, and ever-shorter time-to-market requirements.

To encourage innovative and ground-breaking research in electronic design automation, SIGDA established an annual award recognizing an outstanding Ph.D. dissertation that makes the most substantial contribution to the theory and or application of electronic design automation.

The award consists of a plaque and a USD 1,000 honorarium. The recipient is selected by a committee of experts from academia and industry, appointed by ACM in consultation with the SIGDA Chair.

**Eligibility and Nomination Requirements**
For the 2026 award cycle, the nominated dissertation must have been completed and dated between 1 July 2024 and 31 December 2025.

Each nomination package must include the following materials:

- A PDF copy of the Ph.D. dissertation, written in English
- A statement of up to two pages from the nominee describing the significance, originality, and major contributions of the dissertation
- A nomination letter endorsing the application, submitted by the nominee's advisor, department chair, or dean of the school
- Up to three optional letters of recommendation from experts in the field

The submission deadline for the 2026 ACM Outstanding Ph.D. Dissertation Award in Electronic Design Automation will be the **30th April 2026**. Please email the nomination to sigda.awards@acm.org.

**2025 Award Committee**
Ismail Bustany (AMD), Mustafa Badaroglu (Qualcomm), Jintong Hu (University of Pittsburgh), Sharad Malik (Princeton University), Mark Ren (NVIDIA), Aviral Shrivastava (Arizona State University), Linghao Song (Yale University), Peh Li Shiuan (National University of Singapore), Natarajan Viswanathan (Cadence), Robert Wille (Technical University of Munich).

All standard conflict-of-interest regulations as stated in ACM policy apply.

## ACM SIGDA Outstanding New Faculty Award (ONFA)

The ACM SIGDA Outstanding New Faculty Award (ONFA) recognizes a junior faculty member early in their academic career who demonstrates outstanding potential as

**IWLS'26 - International Workshop on Logic & Synthesis**
Hong Kong, China
May 29-31, 2026
https://www.iwls.org

**GLSVLSI'256– ACM Great Lakes Symposium on VLSI**
Finger Lakes, NY, USA
June 22-24, 2026
http://www.glsvlsi.org

**ICECET'26 - IEEE International Conference on Electrical, Computer and Energy Technologies**
Rome, Italy
July 6-9, 2026
www.icecet.com

**ISVLSI'26 – IEEE Computer Society Annual Symposium on VLSI**
Kolkata, India
July 7-10, 2026
http://www.ieee-isvlsi.org

**DAC'26 – Design Automation Conference**
Long Beach, CA, USA
July 26-29, 2026
http://www.dac.com

**ICLAD'26 - IEEE International Conference on LLM-Aided Design**
Standford, CA, USA
July 30-31, 2026
https://iclad.ai

**ISLPED'26 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design**
Chicago, IL, USA
Aug. 5-7, 2026
http://www.islped.org

an educator and or researcher in the field of electronic design automation. While prior teaching and research accomplishments are important, the selection committee places particular emphasis on the impact achieved during the initial years of the candidate's academic appointment, both within their department and in the broader EDA community.

The award consists of a USD 1,000 cash prize, along with a plaque and a citation.

**Eligibility**
Outstanding new faculty developing academic careers in areas related to electronic design automation are encouraged to apply. This award is not intended for senior or highly experienced investigators who have already established independent research careers, even if they are new to academia.

Eligible candidates must have completed at least one full academic year and no more than four and a half full academic years in a tenure-track position. Applications will also be considered from individuals in continuing (non-visiting) academic positions with substantial educational responsibilities, regardless of whether they are tenure track. Individuals holding research-only positions are not eligible.

Exceptions to the timing requirements may be made for candidates who have interrupted their academic careers for substantive reasons, such as family or medical leave. The presence of such reasons must be attested by the sponsoring institution; no further explanation is required.

**Application Requirements**
Applicants must submit the following materials to the selection committee:

- A two-page statement summarizing the candidate's teaching and research accomplishments since beginning their current academic position, along with plans for further development over the next five years
- A current curriculum vitae
- A letter of endorsement from the candidate's department chair or dean

The submission deadline for the 2026 ACM SIGDA Outstanding New Faculty Award is the **30th April 2026**. Please email the nomination to sigda.awards@acm.org.

**2025 Award Committee**
Ron Duncan (Synopsys), Tsung-Yi Ho (The Chinese University of Hong Kong), Ambar Sarkar (NVIDIA), Chengmo Yang (University of Delaware), Dirk Ziegenbein (Bosch).

All standard conflict-of-interest regulations as stated in ACM policy apply. Any award committee member will recuse themselves from consideration of any candidate where a conflict of interest exists.

# Technical Activities

### 1. Why AI in Semiconductor Inspection Is Becoming a Two-Layer Game

Artificial intelligence is rapidly reshaping semiconductor defect detection, but not along a single trajectory. Instead, the industry is beginning to coalesce around two distinct, and potentially complementary, architectural approaches. One embeds AI tightly within advanced inspection hardware to extract new physical insight from wafers; the other sits above the manufacturing data stack, correlating signals across tools to flag emerging yield risks…

2. **Cellular IoT LPWAN Milestone**

According to the GSMA, by the end of 2025, the global telecommunications sector reached 1 billion active NB-IoT and LTE-M low-power wide area network (LPWAN) connections. This milestone crowns a decade of strategic collaboration among mobile operators, hardware vendors, and standards organizations to build a unified, interoperable foundation for massive machine-type communications…

3. **Nvidia Advances AI-Native Strategy at MWC**

At the 2026 Mobile World Congress (MWC) in Barcelona, the telecom industry confronted a pivotal question: how to integrate AI into wireless networks. This debate is reflected in different strategic approaches: Nvidia supports the use of software-defined, distributed graphics processing units (GPUs), turning the network into a platform for both telecom and AI use cases. In contrast, Intel and Ericsson prefer a central processing unit (CPU)-based approach to manage network workloads while staying within power limits…

4. **Arm Launches First Silicon CPU, Targets Data Center Agentic AI Workloads**

Arm finally made it official this week: the launch of its first production-ready silicon, the Arm AGI CPU, co-developed in conjunction with Meta and targeting agentic AI workloads in the data center. It was dubbed by some as Arm 2.0, a new era for Arm, and Arm CEO Rene Haas highlighted the company's shift into selling silicon for the first time, as opposed to just licensing IP…

# Job Positions

## Technical University of Munich, Germany

**Job Title:** Doctoral Candidate in Computational Proteomics/Bioinformatics

**Description:** Mapping how proteins form and remodel their interaction networks is essential for deciphering the dynamic proteome. Our DC will combine co-expression patterns from the crop proteome atlas, new proteomics data, and protein structure predictions to build a graph neural network that predicts condition-specific protein-protein interactions. High-confidence predictions are expected to feed into protein function classification, shedding light on the uncharacterized and dark proteome. We aim to integrate post-translational modification information mined from the crop proteome atlas, newly generated data, and publicly available resources to complement the network. Ultimately, this project will guide strategies to enhance crop resilience and productivity by leveraging condition-specific networks in plant proteomes. In addition, the doctoral candidate will actively participate in the maintenance and further development of ProteomicsDB particularly in relation to all data acquired in the context of the graduate college "The Proteome that Feed the World". Candidates must hold a master's degree in Data Engineering, Data Science, Bioinformatics, Informatics, or a related discipline. Essential skills include theoretical knowledge of and practical skills in statistical analysis, data mining, data integration, machine learning, programming, backend or frontend development, and database design. For more information, please refer to https://facultyvacancies.com/doctoral-candidate-in-computational-proteomicsbioinformatics,i45348.html.

## Cyprus Institute, Cyprus

**Job Title:** Faculty Position in Machine Learning

**Description:** The selected faculty applicant will enhance the competencies of the Institute in one or more of the following research areas: foundation models and efficient training/adaptation methods on HPC systems; generative AI and multimodal learning; causal representation learning and counterfactual reasoning; robustness, safety, and trustworthy ML (including interpretability and fairness); continual, federated, and edge learning; ML for scientific discovery. Preference will be given to candidates with expertise in AI and ML methodologies complemented with experience in the utilization of advanced computing technologies such as HPC and/or cloud computing. The selected applicant will implement and advance the research agenda of the Institute in general and of CaSToRC in particular in close collaboration with faculty, research staff and the leadership of CyI. As a faculty member, an aptitude and/or experience in mentoring and teaching doctoral and master's students is necessary as the successful candidate will be expected to actively contribute to the Institute's graduate program. For more information, please refer to https://professorpositions.com/faculty-position-in-machine-learning,i45153.html.