Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 56, No. 2

SIGDA - The Resource for EDA Professionals

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.

Online archive: https://www.sigda.org/publications/newsletter

SIGDA News

1. **Semiconductor Revenue 2025 Hits $793 Billion as AI Reshuffles the Rankings**

Worldwide chip industry revenue reached $793 billion in 2025, up 21% year-on-year, according to Gartner's preliminary results. The analyst firm says the jump was driven by AI-related silicon, with AI processing semiconductor revenue exceeding $200 billion.

2. **CES 2026 Highlights AI, Mobility, and Industrial Tech Directions**

CES 2026 took place in Las Vegas earlier this month, bringing together more than 4,000 exhibitors across 13 venues to outline how digital technologies could shape consumer and industrial systems over the coming decade. The event spanned accessibility, AI, energy, mobility, digital health, and robotics, with a strong emphasis on how software-defined and AI-driven approaches are moving from concept to deployment.

3. **TSMC Arizona Expansion Plan Jumps to $465bn Under Proposed US–Taiwan Tariff Deal**

TSMC is reportedly preparing a major new phase of its US build-out that would take its total Arizona spend from $165 bn to $465 bn, as part of a proposed US–Taiwan trade deal that would cut tariffs on Taiwanese exports to 15%. A Reuters report, citing the New York Times, says the package is still being finalized, while a separate Reuters update says Taiwan has reached a "broad consensus" with the US on tariff talks and is working towards a concluding meeting.

4. **Intel Outlines Thick-Core Glass Substrate Concept for AI Data Centre Packaging**

Intel has reportedly showcased a thick-core glass substrate integrated with its EMIB advanced packaging technology, signalling continued development work in glass-based substrates despite earlier uncertainty around its roadmap. The

Message from the EiC

Dear SIGDA members,

In this edition, we bring you the latest news and activities in our community, upcoming conferences, paper deadlines, an insightful article on What is Neuromorphic Computing, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

demonstration was said to have taken place at NEPCON Japan, with the technology positioned for high-performance data centre processors.

5. Cadence and Partners Line Up for Pre-Validated Chiplets
Cadence is trying to make chiplets less of a bespoke science project by pulling IP partners and packaging know-how into a "spec-to-packaged-parts" flow. Cadence says the target is to reduce integration risk for multi-die designs aimed at "physical AI", data-centre and HPC workloads.

6. Cisco Launches 360 Partner Program for the AI Era
Cisco has officially launched its Cisco 360 Partner Program, a redesigned framework aimed at helping partners deliver outcomes in the AI era. The program is the result of 15 months of co-design with Cisco's global partner ecosystem and is now live worldwide.

7. NVIDIA BioNeMo Platform Moves AI Drug Discovery Closer to the Lab
NVIDIA is ramping up its push into AI-driven drug discovery with a major expansion of its BioNeMo platform, backed by new partnerships across pharma, life sciences tools and AI-native biotech. Announced at the J.P. Morgan Healthcare Conference, the move is aimed at closing the loop between AI models and real-world lab experiments.

8. SK Hynix to Invest $12.9 Billion to Boost HBM Packaging
SK Hynix has outlined plans to build a new advanced packaging and test fab in Cheongju, South Korea, as it tries to keep up with fast-rising demand for high-bandwidth memory (HBM) used in AI accelerators. In a Korean-language explainer, the company said the project—called P&T7—will involve total investment of ₩19 trillion ($12.9 billion) and will focus on advanced packaging processes required for AI memory products such as HBM.

SIGDA Awards

1. ASP-DAC Best Paper Award @ ASP-DAC 2026
http://www.aspdac.com/

FESTAL: Dataflow Accelerator Synthesis Framework with Graph-Based Fusion for FPGA
Ruifan Xu, Yuyang Zou, Yun Liang
Peking University

2. ASP-DAC Best Paper Award @ ASP-DAC 2026
http://www.aspdac.com/

C3PO: Commercial-Quality Global Placement via Coherent, Concurrent Timing, Routability, and Wirelength Optimization
Yi-Chen Lu, Hao-Hsiang Hsiao, Rongjian Liang, Wen-Hao Liu, and Haoxing Ren
NVIDIA Research

SIGDA E-News Editorial Board

3. ***ASP-DAC 10-Year Retrospective Most Influential Paper Award @ ASP-DAC 2026***

http://www.aspdac.com/

Design Space Exploration of FPGA-Based Deep Convolutional Neural Networks

Mohammad Motamedi, Philipp Gysel, Venkatesh Akella and Soheil Ghiasi
University of California, Davis

What is Neuromorphic Computing?

Contributing author: Stefano Di Carlo <stefano.dicarlo@polito.it>
Full Professor, Control and Computer Engineering Department, Politecnico di Torino, Italy
AE: Alberto Marchisio <alberto.marchisio@nyu.edu>

Why the Definition Is Breaking—and Why Hardware Designers Should Care

Neuromorphic computing is fashionable again. Funding calls, conference tracks, and startup pitches increasingly invoke the term, often accompanied by claims of brain-like efficiency, intelligence, or adaptability. Yet as the community grows, the meaning of *neuromorphic* is becoming dangerously diluted—and hardware designers should be among the most concerned.

Originally, neuromorphic engineering had a very strict definition. As articulated by pioneers such as Carver Mead [1] and recently refined by Giacomo Indiveri [2], neuromorphic systems were originally defined as *analog, asynchronous, event-driven circuits* that exploited device physics to emulate the dynamics of biological neurons and synapses. Time was physical, noise was not a bug, and computation emerged from the interaction between circuit dynamics and network structure. In short: **the hardware was the algorithm**.

This vision is deeply uncomfortable for traditional digital design and EDA workflows. Analog mismatch, limited precision, lack of standard abstractions, and weak tool support make neuromorphic chips hard to design, verify, and scale. Unsurprisingly, the hardware architecture community reacted by proposing *digital* platforms that retain spikes, events, and sparse communication while discarding analog dynamics [3][4][5][6]. These digital spiking systems are easier to reason about, simulate, and benchmark—and they have undeniably expanded the community.

A provocative claim, meant as a bridge rather than a challenge, is that **the growth of digital and hybrid neuromorphic platforms has been essential to the field's survival and visibility**. This broader interpretation does not negate the original analog vision; instead, it creates a larger ecosystem in which different

Paper Deadlines

ISVLSI'26 – IEEE Computer Society Annual Symposium on VLSI
Kolkata, India
Deadline: Feb. 10, 2026
July 7-10, 2026
http://www.ieee-isvlsi.org

GLSVLSI'256– ACM Great Lakes Symposium on VLSI
Finger Lakes, NY, USA
Deadline: Mar. 2, 2026
June 22-24, 2026
http://www.glsvlsi.org

ICLAD'26 - IEEE International Conference on LLM-Aided Design
Standford, CA, USA
Abstracts due: Mar. 2, 2026
Deadline: Mar 9, 2026
July 30-31, 2026
https://iclad.ai/

ISLPED'26 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
Chicago, IL, USA
Abstracts due: Mar. 2, 2026
Deadline: Mar. 9, 2026
Aug. 5-7, 2026
http://www.islped.org

IWLS'26 - International Workshop on Logic & Synthesis
Hong Kong, China
Abstracts due: Mar. 20, 2026
Deadline: Mar. 27, 2026
May 29-31, 2026
https://www.iwls.org

MICRO'26 – IEEE/ACM Int'l Symposium on Microarchitecture
Athens, Greece
Abstracts due: Mar. 31, 2026
Deadline: Apr. 7, 2026
Oct. 31 - Nov. 4, 2026
http://www.microarch.org/micro59

levels of biological realism and hardware abstraction can coexist and cross-fertilize.

But the pendulum risks swinging too far. Today, almost anything loosely "brain-inspired" risks being labeled neuromorphic. In-memory computing is a prime example. Yes, the brain blurs the boundary between memory and computation—but **memory-centric hardware alone does not make a system neuromorphic**. Without spikes, temporal dynamics, local learning, and asynchronous interaction with the environment, in-memory accelerators are simply another point in the architecture design space, not a fundamentally new computing paradigm. An even more concerning trend is the increasing detachment between "neuromorphic" models and hardware reality. Many works focus on abstract representations of cognition, learning, or reasoning while remaining agnostic to timing, noise, precision, or physical constraints. This research is valuable—but it belongs more naturally to the emerging field of **NeuroAI** [7], not neuromorphic computing in its original or even extended architectural sense.

Why does this matter? Because **definitions shape tools**. If neuromorphic computing becomes purely algorithmic, EDA loses its central role. If, instead, we treat neuromorphic systems as *physically grounded computing machines*, then new challenges emerge:

- How do we verify time-continuous, event-driven systems?
- How do we co-design devices, circuits, architectures, and learning rules?
- What does "correctness" mean when noise and mismatch are features, not flaws?

When the community was small, agreeing on a single definition was easy. Today, it is impossible—and that is not inherently bad. But failing to acknowledge these distinctions creates hype without clarity. For new researchers, especially hardware designers, this confusion can be actively harmful.

References:

[1] C. Mead, "Neuromorphic electronic systems," in Proceedings of the IEEE, vol. 78, no. 10, pp. 1629-1636, Oct. 1990, doi: 10.1109/5.58356.

[2] G. Indiveri, Neuromorphic is dead. Long live neuromorphic., Neuron, Volume 113, Issue 20, 2025, ISSN 0896-6273, https://doi.org/10.1016/j.neuron.2025.09.020.

[3] S. B. Furber, F. Galluppi, S. Temple and L. A. Plana, "The SpiNNaker Project," in Proceedings of the IEEE, vol. 102, no. 5, May 2014, doi: 10.1109/JPROC.2014.2304638.

[4] M. Davies et al., "Loihi: A Neuromorphic Manycore Processor with On-Chip Learning," in IEEE Micro, vol. 38, no. 1, pp. 82-99, January/February 2018, doi: 10.1109/MM.2018.112130359.

[5] A. Carpegna, A. Savino and S. D. Carlo, "Spiker+: A Framework for the Generation of Efficient Spiking Neural Networks FPGA Accelerators for Inference at the Edge," in IEEE Transactions on Emerging Topics in Computing, vol. 13, no. 3, pp. 784-798, July-Sept. 2025, doi: 10.1109/TETC.2024.3511676.

[6] C. Frenkel, M. Lefebvre, J. -D. Legat and D. Bol, "A 0.086-mm2 12.7-pJ/SOP 64k-Synapse 256-Neuron Online-Learning Digital Spiking Neuromorphic Processor in 28-nm CMOS," in IEEE Transactions on Biomedical Circuits and Systems, vol. 13, no. 1, pp. 145-158, Feb. 2019, doi: 10.1109/TBCAS.2018.2880425.

[7] Sadeh, S., Clopath, C. The emergence of NeuroAI: bridging neuroscience and artificial intelligence. Nat. Rev. Neurosci. 26, 583–584 (2025). https://doi.org/10.1038/s41583-025-00954-x

VLSI-SoC'26 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Limassol, Cyprus
Abstracts due: Apr. 20, 2026
Deadline: Apr. 27, 2026
Oct. 11-14, 2026
http://www.vlsi-soc.com

MLCAD'26 - ACM/IEEE Workshop on Machine Learning for CAD
Jeju Island, Korea
Abstracts due: May 16, 2026
Deadline: May 23, 2026
Sep. 7-9, 2026
https://mlcad.org/symposium/

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES) features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor increased to 2.2 in 2023, more than doubling its value from 2020. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through the best paper and rookie of the year awards. Authors can send their paper submissions to the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Prabhat Mishra, Senior Associate Editor, at prabhat@ufl.edu

TODAES Rookie Author of the Year (RAY) Award - Call for Nominations

ACM TODAES introduced the Rookie Author of the Year (RAY) Award, which aims to highlight the achievement of junior researchers in the Design and Design Automation of Electronic Systems field. Specifically, the award recognizes an author whose first-ever peer-reviewed journal paper as a lead author is published in ACM TODAES.

The lead author of a paper refers to the author who contributed the most to the submission. Since people may adopt different ways to order the authors, any nomination for the RAY Award must make it clear that the nominee is the lead author. If two authors satisfy this requirement (meaning they made equal contributions and are both rookie authors), both can receive the RAY award.

The nomination deadline is **February 10, 2026**.

All papers published in the ACM TODAES between January 2025 and December 2025 are eligible. The RAY award will be selected based on originality, timeliness, potential impact, and overall quality. The RAY award will be announced and recognized during the 2026 Design Automation Conference, July 26-29, 2026, Long Beach, CA.

A nomination should include the following material:

- Name and email of the nominator
- Title and author list of the paper, and the issue in which the paper was published
- Confirmation that the paper is the **first** peer-reviewed journal publication in ACM or IEEE, where the nominee is the lead author.
- A brief supporting statement of no more than 150 words.
- A PDF copy of the paper

Upcoming Conferences

ISSCC'26 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA, USA
Feb. 16-20, 2026
http://isscc.org

FPGA'26 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Seaside, CA, USA
Feb. 22-24, 2026
http://www.isfpga.org

ISPD'26 – ACM Int'l Symposium on Physical Design
Bonn, Germany
Mar 15-18, 2026
http://www.ispd.cc/

ISQED'26 - Int'l Symposium on Quality Electronic Design
San Francisco, CA, USA
Apr. 8-10, 2026
http://www.isqed.org

DATE'26 - Design Automation and Test in Europe
Verona, Italy
Apr. 20-22, 2026
http://www.date-conference.com

HOST'26 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
Washington DC, USA
May 4-7, 2026
http://www.hostsymposium.org

FCCM' 26 - IEEE International Symposium On Field-Programmable Custom Computing Machines
Atlanta, GA, USA
May 13-16, 2026
https://www.fccm.org/

Submit the nominations using this link: https://forms.gle/36YAq2TZ6cemxrdVA. If you have questions, e-mail Ann Franchesca Laguna at ann.laguna@dlsu.edu.ph, Managing Editor of ACM TODAES. No self-nomination is allowed.

TODAES Test of Time Paper Award - Call for Nominations

ACM TODAES introduced the TODAES Test of Time Paper Award. This award will recognize an outstanding paper that was published in ACM TODAES at least 10 years ago and has created a significant impact in the field of EDA.

We are now seeking nominations for the 2026 TODAES Test of Time Paper Award. The nomination deadline is **February 10, 2026**. As the inaugural Test of Time Paper Award selection, eligibility is restricted to papers published in ACM TODAES between January 1996 and December 2005. The award will be selected based on evident impact in the field of EDA. The award will be announced and recognized during the 2026 Design Automation Conference, July 26-29, 2026, Long Beach, CA.

A nomination should include the following material:

- Name and email of the nominator
- Title and author list of the paper, and the issue in which the paper was published
- A brief supporting statement of no more than 200 words
- One sentence quote that summarizes the impact of this paper
- A PDF copy of the paper

Submit the nominations using this link: https://forms.gle/55NajeW5eU6YqUtH8 If you have questions, e-mail Ann Franchesca Laguna at ann.laguna@dlsu.edu.ph, Managing Editor of ACM TODAES. No self-nomination is allowed.

Technical Activities

1. CES 2026 Signals the Year Physical AI was Born

CES 2026 has just come to a close, and one thing is clear: This is the year that AI leaps off our monitors and into the physical world at scale. The future of physical AI and humanoid robotics is bright thanks to major announcements spanning the entire technology stack and the broader ecosystem. At the foundation of this push are big SoC players, such as Qualcomm, AMD, Nvidia, and Intel, which unveiled new hardware and software platforms designed to enable large-scale deployment of AI in physical systems. As a result, robots are beginning to transition from research demonstrations to commercial products ready for real-world use…

2. Next UFS Standard to Include Support for AI

The next Universal Flash Storage (UFS) standard has yet to be released, but the standards organization overseeing it has made the uncharacteristic move to disclose its goals for version 5.0. Among the features that can be expected are increased sequential performance up to 10.8 GB/s to meet the demands of AI…

MDTS'26 – IEEE Microelectronics Design & Test Symposium
Albany, NY, USA
May 18-20, 2026
http://natw.ieee.org

RTAS'26 - IEEE Real-Time and Embedded Technology and Applications Symposium
Saint Malo, France
May 12-14, 2026
http://2026.rtas.org

ISCAS'26 – IEEE Int'l Symposium on Circuits and Systems
Shanghai, China
May 24-27, 2026
https://2026.ieee-iscas.org/

ICECET'26 - IEEE International Conference on Electrical, Computer and Energy Technologies
Rome, Italy
July 6-9, 2026
www.icecet.com

DAC'26 – Design Automation Conference
Long Beach, CA, USA
July 26-29, 2026
http://www.dac.com/

3. **Researchers Demonstrate 84.4% Efficiency Silicon Single-Photon Detector**

Silicon single-photon detectors (Si SPDs) are a key component in quantum photonics and single-photon imaging systems operating in the visible spectrum. These applications typically require high photon detection efficiency (PDE) to maximize photon collection. While Si SPDs are compact and relatively easy to operate, pushing their efficiency beyond 80% has remained difficult…

4. **As Demand for Fast AI Tokens Grows, D-Matrix Develops Fast NIC**

Fast LLM token generation is getting a lot of attention as demand grows. D-Matrix is banking on market demand for low latency tokens combined with trends towards inference disaggregation and heterogeneity in data center hardware to sell its AI accelerators and new, specially-designed low-latency NIC cards, Sree Ganesan, VP of product at D-Matrix…

Job Positions

King's College London, UK

Job Title: Research Associate in Computer Science

Description: The post holder will work closely with Prof Elena Simperl and a team of 15+ researchers and PhD students in the area of human-centric AI. The role covers research in the areas mentioned above, as well as the production of scientific publications and application showcases to drive research impact. The researcher will be expected to support impact creation activities, including hackathons, workshops, tutorials and to actively contribute to ongoing AI standardisation efforts such as MLCommons Croissant. The research and innovation outputs will inform work undertaken in the group in several large collaborative grants and application areas, including arts and culture, enterprise data management, and legal compliance. The ideal candidate will have solid expertise in the technical areas mentioned earlier, as well as a proven track record of scientific excellence (through publications in A and A* conferences and journals) and of open science and FAIR practices (through software, datasets and other research outputs, participation in challenges etc). Familiarity with semantic technologies and neuro-symbolic AI, in theory and practice, is a firm requirement. For more information, please refer to https://facultyvacancies.com/research-associate-in-computer-science,i44525.html.

Oak Ridge National Laboratory, US

Job Title: Research Assistant in Computer Science

Description: Oak Ridge National Laboratory (ORNL) is seeking a highly motivated Postdoctoral Research Associate to contribute to the NEUROPIX project, an interdisciplinary effort at the intersection of: High-energy physics (HEP) detectors; Neuromorphic computing; FPGA/ASIC design; Machine learning for edge processing. The successful candidate will work with a multi-institutional,

multidisciplinary team to develop AI-enabled, low-latency signal-processing algorithms for next-generation pixel detectors used in high-energy physics experiments. This position resides in the Relativistic Nuclear and High Energy Physics group, Physics Division, Physical Science Directorate, at ORNL. For more information, please refer to https://facultyvacancies.com/research-assistant-in-computer-science,i44492.html.

United Arab Emirates University, United Arab Emirates

Job Title: Instructor in Computer Science

Description: The College of Information Technology (CIT), UAE University is looking to hire an instructor in the area of computer science or a related field. The candidate must hold an MSc or PhD in computer science or a related field and must have teaching and hands-on experience related to programming languages, database systems, web development, operating systems, Machine Learning and Artificial Intelligence. Application Instructions: Applications must be submitted online at https://jobs.uaeu.ac.ae/. A completed application must include: • A cover letter • An up-to-date curriculum vitae; • and • The names and contact information for at least three recommenders.

Notice to authors