



Special Interest Group on Design Automation ACM/SIGDA E-NEWSLETTER, Vol. 56, No. 1

SIGDA - The Resource for EDA Professionals

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Online archive: <https://www.sigda.org/publications/newsletter>

SIGDA News

1. AI in 2025: Chips, Robots, and the Race for Scale

2025 saw a dramatic change in the fortunes of AI chip makers, with Nvidia in particular benefiting. The growth in AI by companies such as OpenAI catapulted Nvidia into the top slot as the world's most valuable company, while others fell by the wayside.

2. Warehouse Robotics Market Headed for \$31B by 2032

The global warehouse robotics sector is on a fast growth track, driven by escalating demand for automated fulfillment and distribution operations. A new report from Allied Market Research projects the market will climb from \$7.07 billion in 2023 to \$31.34 billion by 2032.

3. IBM to Acquire Confluent in \$11B Deal to Build Smart Data Platform for Enterprise AI

IBM has announced its intent to acquire Confluent for US\$11 billion in cash, a move that signals how seriously the company views real-time data infrastructure as the backbone of enterprise AI.

4. US Approves Samsung, SK Hynix Tool Shipments to China in 2026

The United States has approved annual export licenses allowing Samsung Electronics and SK Hynix to ship US-made semiconductor manufacturing equipment to their China-based fabs in 2026, according to people familiar with the decision. The move applies under a new system that replaces the broad waivers previously granted to certain foreign chipmakers operating in China.

5. Manus Joins Meta to Expand General AI Agent Deployment

Meta has confirmed that Manus will become part of Meta in an acquisition that will see the general-purpose AI agent integrated across the company's consumer and business products, including Meta AI. The financial terms of the deal were not disclosed.

Message from the EiC

Dear SIGDA members,

On behalf of the team, I wish you all a very happy new year. As always, we bring you the latest news and activities in our community, paper deadlines, upcoming conferences, job openings, and an insightful article on What is Posit Arithmetic, in this edition.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

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AE for Researcher spotlight

Xin Zhao,

AE for Paper submission

Ying Wang,

AE for Technical activities

Jiaqi Zhang,

AE for Technical activities

6. [NVIDIA Intel Stake Finalised With \\$5 Billion Share Purchase](#)

NVIDIA has completed its previously announced \$5 billion investment in Intel, finalizing a private placement agreed in September and approved earlier this month by US regulators.

7. [Hyundai Outlines AI Robotics Strategy for CES 2026](#)

Hyundai Motor Group is preparing to put AI-powered robotics firmly in the spotlight at CES 2026, where it will unveil a group-wide AI Robotics Strategy under the theme “Partnering Human Progress.” A newly released teaser signals a strong focus on human-robot collaboration and next-generation manufacturing.

8. [Cadence Tapes Out UCle IP at 64Gbps on TSMC N3P](#)

Cadence has taped out a third-generation Universal Chiplet Interconnect Express (UCle) IP solution supporting data rates of up to 64 Gbps per lane on TSMC’s N3P process. The development reflects continued momentum around chiplet-based architectures as designers push for higher bandwidth and tighter integration at advanced nodes.

9. [Infineon and Lenovo Team Up on Autonomous Driving Compute](#)

Infineon Technologies and Lenovo say they are stepping up their collaboration around in-vehicle compute as carmakers push more functions into centralized architectures for autonomous driving. The companies are positioning Lenovo’s automotive controllers to use Infineon’s automotive microcontrollers for safety-oriented vehicle compute.

10. [Imec Tackles Thermal Limits in 3D HBM-on-GPU Architectures](#)

Imec has unveiled a significant advance in managing heat in next-generation 3D HBM-on-GPU architectures, showing that its system-technology co-optimization (STCO) approach can dramatically reduce GPU temperatures under AI training workloads. Presented this week at the 2025 IEEE International Electron Devices Meeting (IEDM) and explained in a release, the work demonstrates how cross-layer design strategies can bring peak heat levels in 3D-integrated compute platforms down from more than 140°C to roughly 70°C.

What is Posit Arithmetic?

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Posit arithmetic is an emerging alternative to the traditional IEEE 754 [1] floating-point system for representing real numbers in modern computing. Introduced by John Gustafson as a response to long-standing numerical issues in floating-point formats, posits redefine how sign, scale, and precision are encoded through a tapered-precision structure [2, 3]. With growing computational demands and increasingly heterogeneous hardware architectures, posit arithmetic has become a compelling candidate for improving numerical accuracy, dynamic range, and

reproducibility across scientific computing, signal processing, and machine-learning workloads [4].

IEEE 754 formats, although dominant for decades, exhibit several well-known limitations, including multiple NaN encodings, signed zeros, and implementation-dependent rounding and reproducibility behavior [1, 4]. Posits aim to address these issues through a unified representation that eliminates +/- infinity and redundant special cases, offering instead a single Not-a-Real (NaN) value and a more compact encoding of scale and precision [2, 3]. Recent research studied posit arithmetic for scientific computing [5, 6, 7], signal processing [8], and machine learning applications [9, 10]. These highlight its potential to outperform traditional floating-point formats in diverse domains.

Yet, accurate evaluation of numeric formats also requires hardware-level insight. Recently, posit-aware hardware design has been actively explored using dedicated adders, multipliers, dividers, square-root units, and quire-based fused operators [11]. The quire is an accumulation register that enables exact computation of dot products without intermediate rounding, making it attractive for BLAS kernels and ML inference engines [2, 3]. Besides arithmetic blocks, several studies have developed full accelerators and RISC-V cores with custom posit instructions, to leverage parallelism and fused operations directly in hardware. Many of these designs have been implemented in FPGA and ASIC platforms, revealing competitive area-energy trade-offs [4].

In summary, although floating-point arithmetic remains a classic and foundational pillar of modern computing, emerging design constraints and new application domains increasingly motivate a re-examination of alternative numerical formats. Posit arithmetic has become a particularly promising candidate, offering the potential for higher accuracy, improved reproducibility, and more efficient hardware-software co-design [12]. With steady progress in arithmetic units, accelerator architectures, and compiler and toolchain support, posits are rapidly evolving into a realistic option for next-generation computing platforms [4].

References:

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- [7] F. de Dinechin, L. Forget, J.-M. Muller, and Y. Uguen, "Posits: The good, the bad and the ugly," in Proceedings of the conference for next generation arithmetic 2019, in CoNGA'19. New York, NY, USA: Association for Computing Machinery, 2019. doi: 10.1145/3316279.3316285.
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- [9] R. Murillo, A. A. Del Barrio, and G. Botella, "Deep PeNSieve: A deep learning

Paper Deadlines

DAC'26 – Design Automation Conference

Long Beach, CA
Engineering Tracks Deadline: Jan. 12, 2026
July 26-29, 2026
<http://www.dac.com/>

ICECET'26 - IEEE International Conference on Electrical, Computer and Energy Technologies

Rome, Italy
Deadline: Jan. 12, 2026
July 6-9, 2026
www.icecet.com

FCCM' 26 - IEEE International Symposium On Field-Programmable Custom Computing Machines

Atlanta, GA
Deadline: Jan. 17, 2026 (Abstracts due: Jan. 10, 2026)
May 13-16, 2026
<https://www.fccm.org/>

ISVLSI'26 – IEEE Computer Society Annual Symposium on VLSI

Kolkata, India
Deadline: Feb. 10, 2026
July 7-10, 2026
<http://www.ieee-isvlsi.org>

framework based on the posit number system,” Digital Signal Processing, vol. 102, p. 102762, July 2020, doi: 10.1016/j.dsp.2020.102762.

[10] G. Raposo, P. Tomás, and N. Roma, “Positnn: Training Deep Neural Networks with Mixed Low-Precision Posit,” in ICASSP 2021 - 2021 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), June 2021, pp. 7908–7912. doi: 10.1109/ICASSP39728.2021.9413919.

[11] R. Murillo, A. A. D. Barrio, G. Botella and C. Pilato, "Generating Posit-Based Accelerators With High-Level Synthesis," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 10, pp. 4040-4052, Oct. 2023, doi: 10.1109/TCSI.2023.3299009

[12] Gustafson, J. L. (2024). Every Bit Counts: Posit Computing. Chapman & Hall/CRC Computational Science. ISBN 978-1-03-273805-5

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES) features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor increased to 2.2 in 2023, more than doubling its value from 2020. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through the [best paper](#) and [rookie of the year](#) awards. Authors can send their paper submissions to the [manuscript portal](#).

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Prabhat Mishra, Senior Associate Editor, at prabhat@ufl.edu

TODAES Special Issue Call for Papers

Special Issue on Co-Design and Design Automation for Optical/Photonic Computing Systems

This special issue seeks original submissions on pioneering research aimed at advancing co-design and EDA methodologies to support the modeling, simulation, design optimization, and physical implementation toward hybrid integration of optical computing/interconnect and electronic systems with high reliability, scalability, and efficiency. All these topics, as well as further potential topics mentioned below, are of interest to this special issue.

Important Dates

- Submissions deadline EXTENDED: January 31, 2026
- First-round review decisions EXTENDED: March 31, 2026
- Deadline for revision submissions EXTENDED: April 30, 2026
- Notification of final decisions EXTENDED: May 30, 2026
- Tentative publication EXTENDED: Summer 2026

Submissions should be made through the ACM TODAES submission site (<http://mc.manuscriptcentral.com/todaes>)

Upcoming Conferences

VLSID'26 – International Conference on VLSI Design & International Conference on Embedded Systems

Pune, Maharashtra, India

Jan. 3 - 7, 2026

<https://vlsid.org/>

ASP-DAC'26 - Asia and South Pacific Design Automation Conference

Hong Kong, China

Jan. 19-22, 2026

<http://www.aspdac.com/>

HiPEAC'26: Int'l Conference on High Performance Embedded Architectures & Compilers

Krakow, Poland

Jan. 26-28, 2026

<https://www.hipeac.net/2026/krakow/>

Arch4Health: Workshop on Architecture for Health

(In conjunction with HPCA 2026)

Sydney, Australia

Jan. 31, 2026

<https://events.safari.ethz.ch/hpca26-arch4health/>

ISSCC'26 – IEEE Int'l Solid-State Circuits Conference

San Francisco, CA

Feb. 16-20, 2026

<http://isscc.org/>

FPGA'26 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays

Seaside, CA

Feb. 22-24, 2026

<http://www.isfpga.org>

For questions and further information, please contact guest editors at:

- Jiaqi Gu, Arizona State University, jiaqigu@asu.edu
- Cunxi Yu, University of Maryland, cunxiyu@umd.edu
- Sudeep Pasricha, Colorado State University, sudeep@colostate.edu
- Xu Wang, Cadence Design Systems, xubc@cadence.com

More information can be found in this [call for papers](#).

ACM TECS Editor-In-Chief Call for Nominations

The term of the current Editor-in-Chief (EiC) of the ACM Transactions on Embedded Computing Systems (TECS) is coming to an end, and the ACM Publications Board has set up a nominating committee to assist the Board in selecting the next EiC. TECS forms an archival source for publishing high-quality research and developmental results referring to analysis, design, behavior, and experience with embedded computing systems.

The subjects of emphasis are embedded perspectives on: system-level modeling, specification, and synthesis; hardware/software codesign; real-time systems; validation verification; fault tolerance, robustness, reliability and dependability; security and privacy. The scope of TECS also includes emerging technologies, embedded devices and networks for Internet of Things and edge computing, e.g., edge AI and embedded system architectures for TinyML.

Nominations, including self-nominations, are invited for a three-year term as TECS EiC, beginning on April 1, 2026. The EiC appointment may be renewed at most one time. This is a voluntary position, but ACM will provide appropriate administrative support.

Appointed by the ACM Publications Board, Editors-in-Chief (EiCs) of ACM journals are delegated full responsibility for the journal's editorial management consistent with the journal's charter and general ACM policies. The Board relies on EiCs to ensure that the journal's content is of high quality and that the editorial review process is both timely and fair. They have the final say on the acceptance of papers, the Editorial Board size, and Associate Editors' appointment. The ACM Volunteer Editors Position Description contains a complete list of responsibilities. Self-nominations are encouraged and should include a CV and a statement of the candidate's vision for the future development of TECS.

The deadline for submitting nominations is January 15, 2026, although nominations will continue to be accepted until the position is filled. Please send all nominations to the search committee chair. The search committee members are:

- Krishnendu Chakrabarty (Arizona State University), Chair
- Partha Pratim Pande (Washington State University)
- Preeti Ranjan Panda (Indian Institute of Technology, Delhi)
- Wei Zhang (Hong Kong University of Science and Technology)
- Sebastian Steinhorst (Technical University of Munich)

The ACM Publications Board Liaison is: Sartaj Sahni (University of Florida)

ISPD'26 – ACM Int'l Symposium on Physical Design

Bonn, Germany
Mar 15-18, 2026
<http://www.ispd.cc/>

ISQED'26 - Int'l Symposium on Quality Electronic Design

San Francisco, CA
Apr. 8-10, 2026
<http://www.isqed.org>

DATE'26 - Design Automation and Test in Europe

Verona, Italy
Apr. 20-22, 2026
<http://www.date-conference.com>

HOST'26 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust

Washington DC
May 4-7, 2026
<http://www.hostsymposium.org>

MDTS'26 – IEEE Microelectronics Design & Test Symposium

Albany, NY
May 18-20, 2026
<http://natw.ieee.org>

RTAS'26 - IEEE Real-Time and Embedded Technology and Applications Symposium

Saint Malo, France
May 12-14, 2026
<http://2026.rtas.org>

ISCAS'26 – IEEE Int'l Symposium on Circuits and Systems

Shanghai, China
May 24-27, 2026
<https://2026.ieee-iscas.org/>

EDITOR'S PICK FROM ACM TODAES ISSUE 5, 2025

Empirical Guidelines for Deploying LLMs onto Resource-constrained Edge Devices

Ruiyang Qin¹, Dancheng Liu², Chenhui Xu², Zheyu Yan³, Zhaoxuan Tan³, Zhengge Jia³, Amir Nassereldine², Jiajie Li², Meng Jiang³, Ahmed Abbasi³, Jinjun Xiong², and Yiyu Shi³

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Abstract: The scaling laws have become the de facto guidelines for designing large language models (LLMs), but they were studied under the assumption of unlimited computing resources for both training and inference. As LLMs are increasingly used as personalized intelligent assistants, their customization (i.e., learning through fine-tuning) and deployment onto resource-constrained edge devices will become more and more prevalent. An urgent but open question is how a resource-constrained computing environment would affect the design choices for a personalized LLM. We study this problem empirically in this work. In particular, we consider the tradeoffs among a number of key design factors and their intertwined impacts on learning efficiency and accuracy. The factors include the learning methods for LLM customization, the amount of personalized data used for learning customization, the types and sizes of LLMs, the compression methods of LLMs, the amount of time afforded to learn, and the difficulty levels of the target use cases. Through extensive experimentation and benchmarking, we draw a number of surprisingly insightful guidelines for deploying LLMs onto resource-constrained devices. For example, an optimal choice between parameter learning and RAG may vary depending on the difficulty of the downstream task, the longer fine-tuning time does not necessarily help the model, and a compressed LLM may be a better choice than an uncompressed LLM to learn from limited personalized data.

Continue reading more on [ACM DL](#).

Technical Activities

1. [Marvell Eyeing Connectivity as the Next Big Thing in AI](#)

At this year's Marvell Industry Analyst Day, held on Dec. 9, Marvell Technology's President and chief operating officer Chris Koopmans called the company an end-to-end connectivity company. That underscores how connectivity is rapidly emerging as the next big thing in the AI bandwagon...

2. [Stripped Down CXL Scales Memory Wall](#)

The first member of Credo Technology Group's OmniConnect family aims to boost memory bandwidth and memory density to optimize computing efficiency of accelerators and XPUs for AI inference workloads...

3. India Launches DHRUV64, First Indigenous 64-Bit Dual-Core Processor

The Centre for Development of Advanced Computing (C-DAC), under the Indian Ministry of Electronics and Information Technology (MeitY), has launched an indigenously built 1.0 GHz, 64-bit dual-core microprocessor called DHRUV64...

4. Broadcom Hardens Storage Security Against Quantum Threats

The availability of the Brocade X8 Directors and Brocade G820 56-port switch address both the demands of mission-critical workloads and enterprise AI applications while preparing to protect storage from quantum-based threats...

Job Positions

Aalto University, Finland

Job Title: Assistant Professor in Computer Science

Description: The Department of Computer Science at Aalto University invites applications for a tenure-track position at the Assistant Professor level in computer science. This is a broad call and all areas of computer science will be considered. We are in particular interested in candidates whose research is on datacenter-scale computing systems, comprising high-performance computing (HPC); quantum computing and integration with classical HPC; accelerator platforms and accelerated computing; parallel, distributed, and HPC programming models and languages; software design, verification, and optimization; energy-efficient computing; HPC-AI integration. Applicants must be early-career and demonstrate excellent research potential in addition to teaching ability. Women and others whose hiring would increase diversity in computer science are especially encouraged to apply. Our department is committed to fostering an inclusive environment with diverse faculty members. The position has a competitive salary as well as a competitive start-up package. The contract includes occupational health benefits. Relocation services are also available for people coming from abroad. For more information, please refer to <https://computeroxy.com/assistant-professor-in-computer-science,i16014.html>.

Forschungszentrum Jülich, Germany

Job Title: PhD Position in Ensuring Power System Security under Extreme Conditions using Exascale Computing

Description: In this PhD project, you will shape the future of power system security by harnessing exascale computing. Your research will focus on understanding and enhancing grid resilience under extreme scenarios. Your tasks: Conduct security and resilience studies for highly stressed systems

(e.g., multiple faults, high renewable shares, or equipment failures); Evaluate system vulnerabilities and design recovery and stability strategies using large-scale simulation workflows; Build and expand realistic, continent-scale power system models (e.g., the European transmission grid); Implement and test GPU-capable, parallelized simulation frameworks; Work closely with experts in HPC and power systems to enhance scalability and computational performance; Disseminate your findings through scientific publications, conferences, and collaborations; Supervise Bachelor's and Master's students and represent the institute in national and international research contexts. For more information, please refer to <https://facultyvacancies.com/phd-position-in-ensuring-power-system-security-under-extreme-conditions-using-exascale-computing.i44264.html>.

HongKong University of Science and Technology Guangzhou, China

Job Title: Assistant Professor/Associate Professor/Professor

Description: We seek talents in cutting-edge research in FinTech. Applicants must have PhD degrees in FinTech or related fields, e.g., Computational Mathematics, Computer Science, Economics, Finance, Financial Engineering, Information Systems, Machine Learning, Mathematical Finance, Operations Research, Optimization, Probability, And Statistics. Areas of interest include but are not limited to: Blockchain technologies, smart contracts, and digital currencies; Robo-advising, quantitative investing, and risk management; Machine learning, artificial intelligence, and big data analytics in finance; Technological innovations for financial services; Regulatory issues and challenges in FinTech; Digital economy and financial inclusion. For more information, please refer to <https://career.hkust-gz.edu.cn/en/job-detail?jobId=862>.

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