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SIGDA News

1. President Trump Just Chilled the US Smartphone Market
President Trump has said that all smartphones made outside of the US will be subject to a 25 percent tariff, adding to the cost of smartphones and likely slowing the market.

2. Intel, Micron, Qualcomm, TI Join Call for Chip Tariff Exemptions
US chip giants, Intel, Micron, Qualcomm, and Texas Instruments have each submitted comments to the US Department of Commerce seeking to lighten the burden of expected US semiconductor import tariffs or obtain exemptions.

3. TSMC Gets Tough, Warns US Over Chip Import Tariffs
Taiwanese foundry chip maker TSMC has warned the administration of President Trump that if the US imposes import tariffs on chips, or does not provide an exemption to them, it may have to rethink its plan to build six wafer fabs in Arizona.

4. TSMC Looks to 5nm MRAM, Plans First European Design Centre
Taiwanese foundry TSMC is to set up its first design centre in Europe and is looking at a significant leap in memory technology for automotive applications.

5. 1 Tbyte NAND Memory with 321 Layers Fits in AI Smartphones
The memory is optimised for on-device AI with fast sequential read performance and low power, and the thickness is reduced by 15% to fit into flagship AI smartphone designs with 512GB and 1 TB. The NAND memory stack supports the UFS 4.1 protocol for mobile applications.

6. Aion Silicon Wins $12m RISC-V AI Chip Design
UK chip design house Aion Silicon (formerly Sondrel) has won a $12m project to develop a RISC-V accelerator for high-performance computing (HPC) and artificial intelligence (AI) applications.

Message from the EiC

Dear Readers,

In this edition, we bring you the latest news and activities in our community, upcoming conferences, paper deadlines, an insightful article on What is Quantum Compilation, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

7. UK Startup Raises £2.5 Million for Secure MCU Development
SCI Semiconductor Ltd. (Sheffield, England) has raised £2.5 million towards developing a microcontroller based on CHERI, a memory security framework.

8. $30m for US Projects to Add AI into the RF Design Flow
Natcast, a nonprofit that operates the National Semiconductor Technology Centre (NSTC), is funding the first Artificial Intelligence Driven Radio Frequency Integrated Circuit Design Enablement (AIDRFIC) programme with projects from Keysight, Princeton, and the University of Texas.

What is Quantum Compilation?

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Quantum compilation is a core component of the quantum computing stack that translates high-level quantum programs into low-level instructions executable on physical quantum hardware. While the concept is analogous to classical compilation, quantum compilation must operate under drastically different physical and mathematical constraints, making it a rich area of research and innovation.

Quantum programs are typically expressed in the language of quantum circuit or quantum assembly language (QASM) [11], which provide abstractions over quantum operations like unitary transformations (quantum gates), measurement, etc. However, current quantum processors support only a limited set of native gates and impose stringent constraints on qubit connectivity and coherence times. The role of a quantum compiler is to map the abstract program into a sequence of native hardware instructions while preserving its semantics and minimizing execution overhead in terms of time, operation count, error rate, etc. Note that there exist high-level quantum programming languages [9,10] beyond the quantum circuit, while they are still in their infancy.

The quantum compilation process is typically multi-layered. It starts with high-level optimizations, such as removing redundant gates, reordering operations, or simplifying expressions using algebraic identities. It then performs gate decomposition, translating abstract operations into sequences of native gates supported by the hardware. This is followed by qubit mapping and routing, which assigns logical qubits to physical ones and inserts SWAP operations to satisfy connectivity constraints [1]. Finally, hardware-aware optimization steps may reorder instructions or adjust gate choices to reduce error rates or circuit execution time.

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One of the unique challenges in quantum compilation is that even small overheads in depth or gate count can dramatically increase the error probability of a computation. Unlike classical systems, where noise can often be ignored or corrected easily, quantum computations are highly susceptible to decoherence and operational errors. Thus, quantum compilers often include noise-aware optimizations and work closely with hardware calibration data.

Several compiler frameworks have emerged in both academia and industry. IBM's Qiskit [2] and Google's Cirq [3], are open-source efforts tailored to their respective hardware platforms. Third-party tools such as TKET (Quantinuum) [4], QCOR/XACC (Oak Ridge National Laboratory) [5] support more general or cross-platform compilation. These compilers often include techniques such as peephole optimizations, template matching, and machine learning-based decision heuristics for routing and gate selection.

Recent research also explores advanced strategies such as architecture-specific compilation, where the compiler is co-designed with a particular hardware backend, and variational compilation, which uses feedback loops between software and hardware to find optimal compilation paths. In parallel, researchers are working on formal verification techniques [6] to ensure that compiled quantum circuits are semantically equivalent to their source programs, addressing a critical correctness challenge in quantum software.

Quantum compilation is also expanding to support broader types of quantum systems, including analog quantum simulators [7] and high-dimensional encodings such as bosonic modes [8]. These directions call for new abstractions, intermediate representations, and optimization techniques tailored to continuous-variable operations and non-binary encodings.

In summary, quantum compilation is an essential enabler for practical quantum computing. It lies at the intersection of programming languages, computer architecture, optimization theory, and quantum physics. As quantum hardware continues to evolve, advances in compilation will be crucial to unlocking the performance and reliability of future quantum systems.

References:

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Paper Deadlines

iSES'25 – IEEE Int'l Symposium on Smart Electronic Systems
Hyderabad, India
Abstracts due: June 18, 2025
Deadline: June 25, 2025
Dec. 17-20, 2025
http://www.ieee-ises.org/

ASP-DAC'26 - Asia and South Pacific Design Automation Conference
Hong Kong, China
Abstracts due: July 4, 2025
Deadline: July 11, 2025
Jan. 19-22, 2026
http://www.aspdac.com/

FPT'24 - Int'l Conference on Field-Programmable Technology
Shanghai, China
Abstracts due: July 14, 2025
Deadline: July 23, 2025
Dec. 2-5, 2025
http://icfpt.org/

VLSID'26 – International Conference on VLSI Design & International Conference on Embedded Systems
Pune, Maharashtra, India
Deadline: July 25, 2025
Jan. 3 - 7, 2026
https://vlsid.org/

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[11] Nielsen, Michael A., and Isaac L. Chuang. Quantum computation and quantum information. Cambridge university press, 2010.

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES) features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor increased to 2.2 in 2023, more than doubling its value from 2020. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through the best paper and rookie of the year awards. Authors can send their paper submissions to the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

Technical Activities

1. MRAM and ReRAM Target Automotive Opportunities
MRAM and ReRAM technologies are being targeted at automotive reliability, aiming to replace traditional NOR flash…

2. How Digital Twins Are Accelerating Vision AI Training for Robotics
Digital twins are no longer a theoretical concept but a strategic imperative for any robotics team aiming to scale AI vision systems in real-world industrial applications…

3. Aeluma Ramps InGaAs Sensors, Quantum-Dot Lasers
California-based Aeluma is ramping up production of sensors and quantum-dot lasers with the company's new tech that marries indium gallium arsenide (InGaAs) for the first time with 300-mm silicon wafers, promising to boost InGaAs into a range of new devices…

Upcoming Conferences

IWLS'25 - International Workshop on Logic & Synthesis
Verona, Italy
June 12-13, 2025
https://www.iwls.org/

OSCAR'25 - Second Workshop on Open-Source Computer Architecture Research
Tokyo, Japan (co-located with ISCA 2025)
June 21, 2025
https://oscar-workshop.github.io/

DAC'25 – Design Automation Conference
San Francisco, CA, USA
June 22-25, 2025
http://www.dac.com/

GLSVLSI'25 – ACM Great Lakes Symposium on VLSI
New Orleans, LA, USA
June 30 - July 2, 2025
http://www.glsvlsi.org/

ICECET'25 - IEEE International Conference on Electrical, Computer and Energy Technologies
Paris, France
July 3-6, 2025
www.icecet.com

ISVLSI'25 – IEEE Computer Society Annual Symposium on VLSI
Kalamata, Greece
July 6-9, 2025
http://www.ieee-isvlsi.org/

ISLPED'25 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
University of Iceland, Iceland
Aug. 6-8, 2025
http://www.islped.org/

4. Cadence AICP Accelerates Physical AI Applications
Cadence's Tensilica NeuroEdge 130 AI Co-Processor complements any NPU and enables end-to-end execution of the latest agentic and physical AI networks…

Job Positions

Queen's University, Canada

Job Title: Canada Excellence Research Chair in Artificial Intelligence and Exascale Computing

Description: The Queen's University Department of Electrical and Computer Engineering in the Stephen J. R. Smith Faculty of Engineering and Applied Science welcomes applications from outstanding established scholars in the area of Artificial Intelligence and Exascale Computing. Applicants will have a world-leading research program focused on one or more of the following areas related to Artificial Intelligence (AI): Agentic AI, Reinforcement Learning, AI Reasoning, Multimodal AI, Generative AI, Biologically Inspired Models, or AI in Robotics. The research of the candidate is expected to push the frontiers of the above fields through theoretical innovation and practical deployment, with demonstrated impact on applications such as physical and embodied AI, visual understanding, image processing, generative AI, large language models, or related applications. Related research within the Department includes Generative AI, exascale computing at the Caesar Lab, natural language processing, robotics, wearable computing, intelligent communication systems, bio-inspired design, human-computer interaction, and software engineering. For more information, please refer to https://computeroxy.com/canada-excellence-research-chair-in-artificial-intelligence-and-exascale-computing,i15711.html.

University of Nottingham, UK

Job Title: PhD Studentship in Computer Science

Description: This exciting, fully-funded PhD opportunity invites applications from candidates with a robust foundation in data science, modelling, and/or engineering, and a keen interest in deploying data analysis and artificial intelligence (AI) to solve real-world problems in the built environment. The project will advance the capabilities of Pulse, an innovative low-pressure airtightness testing technology co-developed by the University of Nottingham and Build Test Solutions Ltd (BTS). This is a fantastic opportunity to work towards a PhD whilst working with both academia and industry. We are looking for a self-motivated student, with an inquiring mind who would revel in pushing the boundaries of technology. The successful candidate will benefit from cross-disciplinary supervision by experts in building physics and artificial intelligence. The student will have access to research facilities within the Department of Architecture and Built Environment and the School of Computer Science. They will also undertake industrial placement and

MLCAD'25 - ACM/IEEE International Symposium on Machine Learning for CAD
Santa Cruz, CA, USA
Sep. 8-10, 2025
https://mlcad.org/symposium/2025/

ESWEEK'25 - Embedded Systems Week
Taipei, Taiwan
Sept. 28 - Oct. 3, 2025
http://www.esweek.org/

VLSI-SoC'25 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Puerto Varas, Chile
Oct. 12-15, 2025
http://www.vlsi-soc.com

MICRO'25 – IEEE/ACM Int'l Symposium on Microarchitecture
Seoul, Korea
Oct. 18-22, 2025
http://www.microarch.org/micro58

ICCAD'25 – IEEE/ACM Int'l Conference on Computer-Aided Design
Munich, Germany
Oct 26-30, 2025
https://iccad.com/

PACT'25 - Int'l Conference on Parallel Architectures and Compilation Techniques
Irvine, CA, USA
Nov. 3-6, 2025
http://www.pactconf.org

ICCD'25 – IEEE Int'l Conference on Computer Design
Dallas, TX, USA
Nov. 10-12, 2025
http://www.iccd-conf.com

mentorship at BTS, where they will interact with practitioners, gain insights into commercial R&D, and participate in government and industry working groups. For more information, please refer to https://facultyvacancies.com/phd-studentship-in-computer-science,i42105.html.

University of Applied Sciences Northwestern Switzerland, Switzerland

Job Title: Researcher position - Control for reliability of Electromobility Systems

Description: The researcher will participate in a project under the NCCR Automation consortium, collaborating with Principal Investigators from FHNW and ETHZ. The research project is dedicated to designing multi-objective controllers to optimize the efficiency, reliability, and lifespan of electric vehicles. The individual will tackle the challenge of defining reliability and lifespan models for electric vehicle components, including batteries, converters, and capacitors. They will utilize various time and frequency domain control techniques to integrate these sustainability criteria into the design phase. They will also establish optimal, reconfigurable operating profiles for different driving conditions, highlighting the controller's adaptability. The researcher will be involved in national research projects within the NCCR framework, which will include collaboration with other NCCR researchers at ETH, EPFL, and EMPA. The initial contract will be for two years, with the option for renewal. For more information, please refer to https://apply.refline.ch/655298/4221/pub/2/index.html.

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