Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 55, No. 9

SIGDA - The Resource for EDA Professionals

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.

Online archive: https://www.sigda.org/publications/newsletter

SIGDA News

1. **US Buys Intel Stake with Chips Act Cash**
The purchase of 433m shares direct from Intel cost the US government $8.9bn, a 20% discount to the market value, and will be funded by the remaining $5.7bn in grants previously awarded, but not yet paid, to Intel under the U.S. CHIPS and Science Act and $3.2bn awarded to the company as part of the Secure Enclave programme.

2. **Nvidia Ships Long-Awaited Jetson Thor AI Chips**
Nvidia has finally shipped its long-awaited Jetson Thor GPU chip for embedded AI designs. There are two versions with different power envelopes, the T5000 and T4000, aimed at humanoid robots, image processing, and multi-modal edge AI.

3. **IBM and AMD Collaborate on Computing Architecture**
IBM and AMD plan to develop next-generation computing architectures based on the combination of quantum computers and high-performance computing, known as quantum-centric supercomputing. The collaboration aims to develop scalable, open-source platforms that could redefine the future of computing by leveraging quantum computers and software from IBM with high-performance computing and AI accelerators from AMD.

4. **Nvidia Taps Cadence Power Analysis Tool as It Respins Rubin Chip**
Cadence Design Systems has developed a Dynamic Power Analysis (DPA) app that can scale to chip designs with over 40 billion gates, such as the latest Rubin GPU from Nvidia. The DPA runs on the Palladium Z3 emulator to assess the dynamic power consumption of a design across billions of cycles in a few hours with 97 percent accuracy.

5. **Q-CTRL Wins DARPA Awards to Develop Quantum Sensors for Navigation**
Under the DARPA Robust Quantum Sensors (RoQS) program, Q-CTRL has been awarded contracts valued at A$38M (US$24.4M) to augment its field-validated

Message from the EiC

Dear Readers,

In this edition, we bring you the latest news and activities in our community, upcoming conferences, paper deadlines, an insightful article on What are Critical Infrastructure Cyber Twins, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

quantum sensing technologies for demanding real-world use cases in high-performance military vehicles.

6. SanDisk, SK Hynix Team for HBF High Bandwidth Flash

SanDisk and SK Hynix are teaming up to develop a specification for high-bandwidth flash (HBF) memory for AI systems. A technical advisory board is directing the development of the open specification, although this is based on the proprietary Sandisk BiCS (Bit Cost Scalable) process technology and proprietary CBA wafer bonding, and was developed over the past year with input from leading AI industry players, including competitor Kioxia. SanDisk has been in merger discussions with Kioxia since its spin-out from Western Digital.

7. First Wireless OLED Contact Lens for Wearable Diagnostics

A team of Korean researchers has developed a next-generation wireless ophthalmic diagnostic technology that replaces the existing stationary, darkroom-based retinal testing method by incorporating an "ultrathin OLED" into a contact lens.

8. PCIe 8.0 Looks to 256GT/s for AI

The PCI special interest group (SIG) is targeting speeds of 256GTransactions/s with PCI Express (PCIe) 8.0 to provide faster links between chips for AI. At the same time, the Universal Chiplet Interconnect Express (UCIe) Consortium has announced UCIe 3.0. The PCIe 8.0 specification will double the data rate of the PCIe 7.0 specification, with release planned by 2028.

SIGDA Awards

1. 2025 Best Paper @ ISLPED 2025

https://www.islped.org/2025/files/2025_ISLPED_Program_Booklet.pdf

GenSoC: A Multi-Agent-Assisted SoC Generation Methodology Leveraging Open-Source Hardware

Peiran Yan, Qinzhe Zhi, Lifeng Liu, Tianyu Jia

2. 2025 Best Paper CANDIDATE @ ISLPED 2025

https://www.islped.org/2025/files/2025_ISLPED_Program_Booklet.pdf

- ***Partial-Sum Quantization Based on Pseudo-Quantization Noise for Variation-Tolerant Analog In-Memory Computing***
  Nameun Kang, EunHyeok Park, Sangsu Park, Jongil Kim, Jaeyun Yi, Jae-Joon Kim

- ***Minimizing Redundant Checkpoint Triggers for Efficient Intermittent Systems***
  Youngbin Kim, Yoojin Lim

- ***E-Flash: Energy-Efficient DNN Mapping on NAND Flash Memory with State-Switching Algorithm***
  Gisan Ji, Sanghun Shin, Jangho Baik, Wonbo Shim, Sungju Ryu

SIGDA E-News Editorial Board

- ***Accelerating LLM Inference with Flexible N:M Sparsity via A Fully Digital Compute-in-Memory Accelerator***
  Akshat Ramachandran, Souvik Kundu, Arnab Raha, Shamik Kundu, Deepak K. Mathaikutty, Tushar Krishna

- ***Faster Ternary and Binary Neural Network Inference on CPU by Reducing Popcount***
  Olivier Fischer, Shien Zhu, Gustavo Alonso

- ***Cost-efficient Processing-in-Memory Architecture with Training-free and Universal Error Compensation***
  MyeongJi Yun, Jung Gyu Min, Sein Oh, Jiwoung Choi, Minkyu Je, Jang-Sik Lee, Youngjoo Lee

- ***DPIMA: A DRAM-Based Processing-in-Memory Accelerator for Privacy-Preserving Machine Learning***
  Bokyung Kim

3. 2025 SBCCI Best Paper Candidate @SBCCI 2025
http://www.psi.poli.usp.br/chipinsampa/sbcci-program/

- ***Fine-grain Temperature Monitoring for Many-Core Systems***
  Alzemiro Henrique Lucas da Silva, André Luís del Mestre Martins and Fernando Moraes

- ***DNAr-Logic: A constructive logic DNA circuit design library in R language for Molecular Computing***
  Renan Marks, Daniel Kneipp, Marcos Guterres, Poliana Oliveira and Omar Neto

- ***NMLSim 2.0: A robust CAD and simulation tool for in-planeNanomagnetic Logic based on the LLG equation***
  Lucas Augusto Lascasas Freitas, João Guilherme Nizer Rahmeier, Omar Paranaíba Vilela Neto, Luiz Guilherme C. Melo

- ***Energy efficient fJ/spike LTS e-Neuron using 55-nm node***
  Pietro Maris Ferreira, Nathan De Carvalho, Geoffroy Klisnick and Aziz Benlarbi-Delai

- ***Amplifier-based MOS Analog Neural Network Implementation and Weights Optimization***
  Tiago Weber, Diogo Labres and Fabian Cabrera

4. 2025 Sforum best paper candidate @SBCCI2025
http://www.psi.poli.usp.br/chipinsampa/sbcci-program/

- ***Radiation Robustness Evaluation on XOR Logic Gates at 16nm CMOS and FinFET Technology***
  Rafael N. M. Oliveira and Cristina Meinhardt

Paper Deadlines

ISSCC'26 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA, USA
Deadline: Sept. 3, 2025
Feb. 16-20, 2026
http://isscc.org

DATE'26 - Design Automation and Test in Europe
Verona, Italy
Abstracts due: Sept 7, 2025
Deadline: Sept. 14, 2025
April 20-22, 2026
http://www.date-conference.com

ISQED'26 - Int'l Symposium on Quality Electronic Design
San Francisco, CA, USA
Deadline: Sept. 17, 2025
Apr. 8-10, 2026
http://www.isqed.org

FPGA'26 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Seaside, CA, USA
Abstracts due: Sept. 24, 2025
Deadline: Oct. 1, 2025
Feb. 22-24, 2026
http://www.isfpga.org

ISPD'26 – ACM Int'l Symposium on Physical Design
Bonn, Germany
Abstracts due: Sept. 21, 2025
Deadline: Sept. 28, 2025
Mar 15-18, 2026
http://www.ispd.cc/

ISCAS'26 – IEEE Int'l Symposium on Circuits and Systems
Shanghai, China
Deadline: Oct. 12, 2025
May 24-27, 2026
https://2026.ieee-iscas.org/

- ***Proposal and Evaluation of Pin Access Algorithms for Detailed Routing***
  Marcelo Danigno, Paulo Butzen, Jorge Ferreira, André Oliveira, Eder Monteiro, Mateus Fogaça and Ricardo Reis

What are Critical Infrastructure Cyber Twins?

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We have been witnessing an increasing number of cyberattacks against our critical infrastructure in the decade, such as Ukrainian power plant attack in 2025, cyberattack against a water treatment system in Florida in 2021, and Colonial Pipeline ransomware attack in 2021. To protect our smart city infrastructure, education and training of cybersecurity experts particularly trained for critical infrastructure operation technology (OT) systems is of high demand globally. However, use of real infrastructure for such exercise or training is not a realistic option owing to the potential risk of disruption of real critical infrastructure. Although the 2nd best solution would be to utilize a sandboxed testbed using the same set of devices and hardware consisting of the real system, for instance critical infrastructure cybersecurity testbeds established in Singapore (https://itrust.sutd.edu.sg/itrust-labs_overview/) [1,2,3,4], such hardware-based testbeds have faced difficulty and limitation in terms of configurability and scalability to meet the practical demands. Moreover, the deployment and maintenance cost of hardware-based testbed is often prohibitively high, which often prohibits experimentation of high-risk cyberattack for safety of a testbed itself.

Cyber twins are digital twins or virtual replicas of modernized (i.e., ICT-powered) critical infrastructures that are specifically intended for cybersecurity purposes. In other words, cyber twins are cyber ranges simulating cyber-physical systems consisting of modernized critical infrastructures. Just like the cyber ranges for enterprise IT systems, cyber twins allow interactive cybersecurity training as well as experiments in a virtual, but high-fidelity, environment. At the high level, cyber twins consist of backend simulators of physical plant behaviors that are tightly coupled with virtual industrial control systems (ICS) devices, such as programmable logic controllers (PLCs), communicating with each other by using industrial control systems (ICS) network protocols on a virtual OT network topology. Because of the software-based nature, cyber twins address the aforementioned challenges of hardware-based testbeds, while allowing practical hands-on cybersecurity exercises that sufficiently reflects the real-world critical infrastructure system. Therefore, cyber twins have been increasingly utilized in many of the cybersecurity training programs and competition events, including NATO's Locked Shields and CISS (Critical Infrastructure Security Showdown) by Singapore University of Technology and Design (SUTD).

RTAS'26 - IEEE Real-Time and Embedded Technology and Applications Symposium
Saint Malo, France
Deadline: Nov. 13, 2025
May 12-14, 2026
http://2026.rtas.org

HOST'26 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
Washington DC, USA
Abstracts due (Winter): Dec. 1, 2025
Deadline (winter): Dec. 8, 2025
May 4-7, 2026
http://www.hostsymposium.org

While a cyber twin is a practical, cost-efficient, customizable-based solution, its design and implementation require extensive domain knowledge on both the cyber and physical sides of modernized critical infrastructures of interest as well as engineering efforts. Although there are a number of efforts made in this area, most of the offerings are either closed-source or one-off implementations (e.g., [5,6]), thus leaving it difficult for end users to have a twin that meets their technical demands and specific preferences. In order to address this challenge, we have been working on reconfigurable cyber twins [7] as well as a framework for automated generation of cyber twins [8,9] based on the standard-based, XM-based model files, which is available as an open-source project at https://github.com/smartgridadsc/CyberRange. This technology was further utilized as a building block for cloud-based cyber range as a service (CRaaS) [10]. These solutions can further enhance not only accessibility to a cyber twin of the desired specification but also portability and reproducibility of virtual critical infrastructure for cybersecurity research.

In sum, a cyber twin is a valuable tool to offer a high-fidelity, virtual platform for critical infrastructure cybersecurity education, training, competition, as well as interactive, hardware-in-the-loop device testing. Beyond that, it is also a promising tool for generating and collecting datasets for cybersecurity research using AI and machine-learning techniques, where scarcity of data is a universal challenge. By enabling cyber-physical risk assessments and resilience analysis through automated, iterative simulation of cyberattack and disturbance as well as recovery strategies empowered by AI technologies, a cyber range can contribute to the design and operation of secure and trustworthy smart city infrastructure.

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[7] Mathur AP. Reconfigurable digital twin to support research, education, and training in the defense of critical infrastructure. IEEE Security & Privacy. 2023 Jun 15;21(4):51-60.

[8] Mashima D, Roomi MM, Ng B, Kalberczyk Z, Hussain SS, Chang EC. Towards automated generation of smart grid cyber range for cybersecurity experiments and training. In 2023 53rd Annual IEEE/IFIP International Conference on Dependable

Upcoming Conferences

MLCAD'25 - ACM/IEEE International Symposium on Machine Learning for CAD
Santa Cruz, CA, USA
Sep. 8-10, 2025
https://mlcad.org/symposium

ESWEEK'25 - Embedded Systems Week
Taipei, Taiwan
Sept. 28 - Oct. 3, 2025
http://www.esweek.org

VLSI-SoC'25 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Puerto Varas, Chile
Oct. 12-15, 2025
http://www.vlsi-soc.com

MICRO'25 – IEEE/ACM Int'l Symposium on Microarchitecture
Seoul, Korea
Oct. 18-22, 2025
http://www.microarch.org/micro58

ICCAD'25 – IEEE/ACM Int'l Conference on Computer-Aided Design
Munich, Germany
Oct 26-30, 2025
https://iccad.com/

PACT'25 - Int'l Conference on Parallel Architectures and Compilation Techniques
Irvine, CA, USA
Nov. 3-6, 2025
http://www.pactconf.org

ICCD'25 – IEEE Int'l Conference on Computer Design
Dallas, Texas, USA
Nov. 10-12, 2025
http://www.iccd-conf.com

Systems and Networks-Supplemental Volume (DSN-S) 2023 Jun 27 (pp. 49-55). IEEE.
[9] Mashima D, Chen Y, Roomi MM, Lakshminarayana S, Chen D. Cybersecurity for Modern Smart Grid Against Emerging Threats. In Foundations and Trends in Privacy and Security: Vol. 5: No. 4, pp 189-285.
[10] Chng B, Ng B, Roomi MM, Mashima D, Lou X. CRaaS: Cloud-based Smart Grid Cyber Range for Scalable Cybersecurity Experiments and Training. In2024 IEEE International Conference on Communications, Control, and Computing Technologies for Smart Grids (SmartGridComm) 2024 Sep 17 (pp. 333-339). IEEE.

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES) features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor increased to 2.2 in 2023, more than doubling its value from 2020. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through the best paper and rookie of the year awards. Authors can send their paper submissions to the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Prabhat Mishra, Senior Associate Editor, at prabhat@ufl.edu

TODAES Special Issue Call for Papers

Special Issue on Co-Design and Design Automation for Optical/Photonic Computing Systems

This special issue seeks original submissions on pioneering research aimed at advancing co-design and EDA methodologies to support the modeling, simulation, design optimization, and physical implementation toward hybrid integration of optical computing/interconnect and electronic systems with high reliability, scalability, and efficiency. All these topics, as well as further potential topics mentioned below, are of interest to this special issue.

Important Dates

- Submissions deadline: Oct 15, 2025
- First-round review decisions: Dec 15, 2025
- Deadline for revision submissions: Jan 15, 2026
- Notification of final decisions: Feb 15, 2026
- Tentative publication: Spring 2026

Submissions should be made through the ACM TODAES submission site (http://mc.manuscriptcentral.com/todaes)

For questions and further information, please contact guest editors at:

- Jiaqi Gu, Arizona State University, jiaqigu@asu.edu

FPT'25 - Int'l Conference on Field-Programmable Technology
Shanghai, China
Dec. 2-5, 2025
http://icfpt.org

ISED'25 – Int'l Conference on Intelligent Systems and Embedded Design
Chhattisgarh, India
Dec. 17-19, 2025
http://isedconf.org

iSES'25 – IEEE Int'l Symposium on Smart Electronic Systems
Hyderabad, India
Dec. 17-20, 2025
http://www.ieee-ises.org

HiPC'25 – IEEE Int'l Conference on High Performance Computing, Data, And Analytics
Hyderabad, India
Dec. 17-20, 2025
http://www.hipc.org

VLSID'26 – International Conference on VLSI Design & International Conference on Embedded Systems
Pune, Maharashtra, India
Jan. 3 - 7, 2026
https://vlsid.org/

ASP-DAC'26 - Asia and South Pacific Design Automation Conference
Hong Kong, China
Jan. 19-22, 2026
http://www.aspdac.com

HiPEAC'26: Int'l Conference on High Performance Embedded Architectures & Compilers
Krakow, Poland
Jan. 26-28, 2026
https://www.hipeac.net/2026/krakow/

- Cunxi Yu, University of Maryland, cunxiyu@umd.edu
- Sudeep Pasricha, Colorado State University, sudeep@colostate.edu
- Xu Wang, Cadence Design Systems, xubc@cadence.com

More information can be found in this call for papers.

Technical Activities

1. **U.K. Startup Scaling Quantum Computing With Photonics**

There's value from different modalities of deploying qubits; the value of quantum computing isn't just from deploying a million-qubit machine; and that quantum computing is already here now and solving problems…

2. **Embedded SRAM Adds AI Horsepower**

Static random-access memory (SRAM) has become such a well-established memory that it is now perceived as off-the-shelf "plumbing," but Marvell Technology's latest custom SRAM aims to demonstrate how the incumbent memory has a role to play in artificial-intelligence data centers…

3. **UCIe 3.0 Doubles Data Rate For 2D Chiplets**

The UCIe Consortium released the 3.0 version of its UCIe open standard, designed for high-speed, interoperable connectivity between chiplets in the same package. The new version of the standard is fully backwards compatible with earlier versions…

4. **U.S. Startups Debut First E-Beam Tools for Wafer Writing**

Two U.S. startups, Multibeam and SecureFoundry, are making the world's first e-beam lithography tools that write chip designs directly to a silicon wafer without using masks…

Job Positions

University College London, UK

Job Title: Lecturer in Software Engineering

Description: The appointee will be based in the Software Systems Engineering (SSE) group within the Department of Computer Science at UCL. The post holder will be responsible to: Act as module lead for modules offered by the specialised MSc programmes run by the SSE group (Software Systems Engineering and Artificial Intelligence and Data Engineering); Design new modules as well as contribute to existing modules as required; Teach lectures and tutorials across other related modules in collaboration with other tutors; Contribute to administration activities within the Department of Computer Science, as agreed with their line manager; Additionally, they may be asked to teach lectures and tutorials for postgraduate and undergraduate students across other related

modules in collaboration with other tutors. For more information, please refer to https://facultyvacancies.com/lecturer-in-software-engineering,i42878.html.

Technical University of Munich, Germany

Job Title: Full Professor in Software

Description: We seek to appoint an expert in the research area of Software & System Security with some of the following focus areas: Secure software engineering: methods and tools; Secure system engineering, in particular, system software and embedded systems; Automated analysis of the security of complex software systems; Risk analysis and security assessment, security metrics; Security in communication systems; Secure AI and AI for security; Privacy-enabling technologies. Teaching responsibilities include courses in the university's bachelor and master programs. The professorship is associated with the directorship at Fraunhofer AISEC, which includes the scientific, technical, and entrepreneurial control and development of the institute within the Fraunhofer model (a key aspect of the Fraunhofer model is the collaboration with industry). In addition to the thematic orientation of the research, you will be involved in project acquisition and management, the transfer of results to industry as well as personnel management – with an emphasis on modern leadership and change processes. Please send your application no later than 22 September 2025. For more information, please refer to https://facultyvacancies.com/full-professor-in-software,i42870.html.

ETH Zurich, Switzerland

Job Title: Research Software Engineer

Description: Scientific Software and Data Management (SSDM) is part of ETH's central IT department. It comprises software engineers from diverse backgrounds who develop software to support research projects across a broad spectrum of ETH's academic departments, including biology, physics, engineering, economics, architecture and more. Due to a growing portfolio of projects, we are looking for a versatile software engineer to work to lead or contribute to a number of projects. You will work on a Horizon-funded project, EOSC Data Commons, alongside other developers within SIS and at partner institutions, to build a framework for discovering, sharing and executing data and algorithms in a distributed environment. The main technology will be Python, though Scala and Typescript knowledge are a plus. Most importantly, we are looking for a person who is flexible, communicates well and interested in and able to aquire new skills. For more information, please refer to https://facultyvacancies.com/research-software-engineer,i42785.html.