Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 55, No. 7

SIGDA - The Resource for EDA Professionals

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
Circulation: 2,700

Online archive: https://www.sigda.org/publications/newsletter

SIGDA News

1. **AI demand is driving the market, uncertainty lies ahead, says SEMI**
According to SEMI, the electronics and chip markets in 1Q25 markets followed typical seasonality, but the industry has warned of atypical market shifts due to tariff uncertainty.

2. **UK Plans $1 Billion AI Supercomputer**
The UK government is allocating $1bn (£750m) for a next-generation AI supercomputer based in Edinburgh, Scotland.

3. **Cadence, Samsung Bring AI to SoC, 3D-IC and Chiplet Design**
Cadence and Samsung Foundry have expanded their collaboration with a new multi-year IP agreement and joint development of advanced AI-driven flows on the latest SF2P and other advanced process nodes.

4. **Mitsubishi Verifies 7 GHz Band 5G GaN PA Module**
Mitsubishi Electric Corporation claims to have developed the first compact 7 GHz band gallium nitride (GaN) power amplifier module (PAM) with the highest power efficiency.

5. **AI Restructures Siemens EDA Tools**
Siemens EDA is restructuring the structure of its EDA tools to adopt a new architecture for artificial intelligence (AI) and machine learning (ML).

6. **TI, Micron Fabs Highlight the High Cost of Politics**
Texas Instruments (TI) has re-announced its plans to invest in seven semiconductor fabs in the US at an increased cost of $60bn.

7. **NFC Release 15 Extends Range to Grow Use Cases**
NFC Release 15, announced by the NFC Forum, will extend the range of certified compliant NFC contactless connections up to 2 cm, which is 4x greater than the current range of 0.5 cm, supporting faster, more reliable contactless interactions

Message from the EiC

Dear Readers,

In this edition, we bring you the latest news and activities in our community, upcoming conferences, paper deadlines, an insightful article on What is Hardware Software Co-Design, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

across a growing number of use cases such as wireless charging, kitchen appliances, wearables, and digital keys.

8. Intel Closes Automotive Chip Business

This is separate from Intel's 88% stake in ADAS and self-driving controller chip designer Mobileye, which was spun out as a separate company in 2022. Intel says that 50 million cars use its chips, but these are mainly general-purpose processors.

SIGDA Awards

1. 2025 MARIE R. PISTILLI WOMEN IN ENGINEERING ACHIEVEMENT AWARD @ DAC 2025

https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

Marilyn Wolf
Elmer E. Koch Professor of Engineering,
University of Nebraska—Lincoln, US

2. 2025 DAC UNDER-40 INNOVATORS AWARD @ DAC 2025

https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

- **Tsung-Wei Huang,** *University of Wisconsin, Madison*
- **Tushar Krishna,** *Georgia Institute of Technology*
- **Xiaolin Xu,** *Northeastern University*
- **Hajar Falahati,** *Barcelona Supercomputing Center*
- **Souvik Kundu ,** *Intel Corporation*

3. 2025 MOST INFLUENTIAL PAPER AWARD @ DAC 2025

https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

Chisel: Constructing Hardware in a Scala Embedded Language (in DAC'12)

Jonathan Bachrach, Huy Vo, Brian Richards, Yunsup Lee, Andrew Waterman, Rimas Avižienis, John Wawrzynek, Krste Asanovic

University of California Berkeley, US

4. 2025 BEST PAPER NOMINEES @ DAC 2025

https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

- *INSTA: An Ultra-Fast, Differentiable, Statistical Static Timing Analysis Engine for Industrial Physical Design Applications*
- *LVM-MO: A Large Vision Model Pioneer for Full-Chip Mask Optimization*
- *GEM: GPU-Accelerated Emulator-Inspired RTL Simulation*

SIGDA E-News Editorial Board

- *CirSTAG: Circuit Stability Analysis on Graph-based Manifolds*
- *PICK: An SRAM-based Processing-in-Memory Accelerator for K-Nearest-Neighbor Search in Point Clouds*
- *ZenLeak: Practical Last-Level Cache Side-Channel Attacks on AMD Zen Processors*
- *BoolE: Exact Symbolic Reasoning via Boolean Equality Saturation*

5. ACM TODAES ROOKIE AUTHOR OF THE YEAR (RAY) AWARD @ DAC 2025 ACM/SIGDA

https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

Enhanced Compiler Technology for Software-based Hardware Fault Detection

Davide Baroffio
Politecnico di Milano, Italy

6. 2025 ACM TODAES BEST PAPER AWARD @ DAC 2025 ACM/SIGDA

https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

VeriGen: A Large Language Model for Verilog Code Generation

Shailja Thakur[1], Baleegh Ahmad[1], Hammond Pearce[2], Benjamin Tan[3], Brendan Dolan-Gavitt[1], Ramesh Karri[1], Siddharth Garg[1]

[1] New York University, USA | [2] University of New South Wales, Australia | [3] University of Calgary, CA

7. 2024 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO EDA @ DAC 2025 IEEE/CEDA

https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

Prof. Jason Cong
UCLA

8. ACM SIGDA DISTINGUISHED SERVICE AWARD @ DAC 2025 ACM/SIGDA

https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

- **Sharon Hu,** *University of Notre Dame*
- **Ulf Schlichtmann,** *Technical University of Munich*

9. SIGDA SERVICE AWARD @ DAC 2025 ACM/SIGDA

https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

- **Yuan-Hao Chang,** *Academia Sinica*
- **Preeti Ranjan Panda,** *Indian Institute of Technology Delhi*

Paper Deadlines

ASP-DAC'26 - Asia and South Pacific Design Automation Conference
Hong Kong, China
Abstracts due: July 4, 2025
Deadline: July 11, 2025
Jan. 19-22, 2026
http://www.aspdac.com/

FPT'25 - Int'l Conference on Field-Programmable Technology
Shanghai, China
Abstracts due: July 14, 2025
Deadline: July 23, 2025
Dec. 2-5, 2025
http://icfpt.org/

VLSID'26 – International Conference on VLSI Design & International Conference on Embedded Systems
Pune, Maharashtra, India
Deadline: July 25, 2025
Jan. 3-7, 2026
https://vlsid.org/

ISSCC'26 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Deadline: Sept 3, 2025
Feb 15-19, 2026
http://isscc.org/

ISPD'26 – ACM Int'l Symposium on Physical Design
Bonn, Germany
Abstracts due: Sept. 21, 2025
Deadline: Sept. 28, 2025
Mar 15-18, 2026
http://www.ispd.cc/

- **Frank Schirrmeister,** *Synopsys*
- **Ziegenbein Dirk,** *Robert Bosch*

10. IEEE FELLOWS @ DAC 2025 IEEE/CEDA
https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

- **Umit Ogras,** *University of Wisconsin, Madison*
- **Patrick Schaumont,** *Worcester Polytechnic Institute*
- **Peilin Song,** *IBM Thomas J. Watson Research Center*
- **Sheldon Tan,** *University of California, Riverside*

11. IEEE/ACM A RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION @ DAC 2025 IEEE/CEDA
https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

- **Luca Carloni,** *Columbia University*
- **Kenneth L. McMillan,** *UT Austin*
- **Alberto Sangiovanni-Vincentelli,** *UC Berkeley*

12. IEEE CEDA OUTSTANDING SERVICE AWARD @ DAC 2025 IEEE/CEDA
https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

Vivek De
Intel

13. IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS DONALD O. PEDERSON BEST PAPER AWARD @ DAC 2025 IEEE/CEDA
https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

SpikeSim: An End-to-End Compute-in-Memory Hardware Evaluation Tool for Benchmarking Spiking Neural Networks

Abhishek Moitra1, Abhiroop Bhattacharjee1, Runcong Kuang2, Gokul Krishnan3, Yu Cao2, Priyadarshini Panda1

[1] Yale University | [2] Arizona State University | [3] Meta Reality Labs

14. IEEE GUSTAV ROBERT KIRCHOFF AWARD @ DAC 2025 IEEE/CEDA
https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

Prof. Giovanni di Micheli
EPFL

Upcoming Conferences

ISVLSI'25 – IEEE Computer Society Annual Symposium on VLSI
Kalamata, Greece
July 6-9, 2025
http://www.ieee-isvlsi.org/

ISLPED'25 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
University of Iceland, Iceland
Aug. 6-8, 2025
http://www.islped.org/

MLCAD'25 - ACM/IEEE International Symposium on Machine Learning for CAD
Santa Cruz, CA, USA
Sep. 8-10, 2025
https://mlcad.org/symposium/2025/

ESWEEK'25 - Embedded Systems Week
Taipei, Taiwan
Sept. 28 - Oct. 3, 2025
http://www.esweek.org/

VLSI-SoC'25 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Puerto Varas, Chile
Oct. 12-15, 2025
http://www.vlsi-soc.com

MICRO'25 – IEEE/ACM Int'l Symposium on Microarchitecture
Seoul, Korea
Oct. 18-22, 2025
http://www.microarch.org/micro58

ICCAD'25 – IEEE/ACM Int'l Conference on Computer-Aided Design
Munich, Germany
Oct 26-30, 2025
https://iccad.com/

15. IEEE JUN-ICHI NISHIZAWA MEDAL @ DAC 2025 IEEE/CEDA
https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

Prof. Robert W. Dutton
Stanford University

16. IEEE JAMES H. MULLIGAN, JR. EDUCATION MEDAL @ DAC 2025 IEEE/CEDA
https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

Prof. Jan Rabaey
UC Berkeley

17. IEEE COMPUTER SOCIETY EDWARD J. MCCLUSKEY TECHNICAL ACHIEVEMENT AWARD @ DAC 2025 IEEE/CEDA
https://www.dac.com/Portals/0/62DAC/Program/62DACProgram.pdf?ver=M_DMJU3AU3OMZhX6dDjwsQ%3d%3d

Prof. Hai (Helen) Li
Duke University

PACT'25 - Int'l Conference on Parallel Architectures and Compilation Techniques
Irvine, CA, USA
Nov. 3-6, 2025
http://www.pactconf.org

ICCD'25 – IEEE Int'l Conference on Computer Design
Dallas, TX, USA
Nov. 10-12, 2025
http://www.iccd-conf.com

What is Hardware-Software Co-Design?

Contributing author: Yi Sheng <ysheng2@gmu.edu>
Incoming Assistant Professor, University of South Florida
AE: Han Wang <han.wang.hw@temple.edu>

As modern computing systems demand ever higher performance, efficiency, and adaptability, traditional design methods—where hardware and software are developed in isolation—are reaching their limits [1][2]. Hardware-software co-design is a holistic approach that develops both hardware and software components together, enabling them to be optimized in tandem [3][4]. This method is increasingly essential for embedded systems, AI accelerators, and real-time applications where tight resource constraints and high-performance requirements coexist.

Historically, hardware and software were developed sequentially, adapting one to fit the other. This separation often results in inefficiencies and underutilized hardware. In contrast, co-design allows for concurrent development, enabling designers to balance constraints across layers and meet ambitious design goals. Take edge AI for example. Devices like wearables or drones must run intelligent applications with strict energy, latency, and fairness constraints. Our group developed a hybrid vision model for edge medical AI that was co-designed from neural architecture to hardware execution. This system achieved low latency and

high fairness, which would not be possible through isolated software or hardware optimization [3].

Another prominent application of co-design is in AI accelerators. Rather than relying on general-purpose hardware, designers now co-optimize neural network architectures alongside specialized chips and compilers. This coordinated approach allows smaller, co-designed models to outperform larger, generic ones in fairness, latency, and efficiency—an especially valuable outcome in resource-constrained environments [4]. A key driver of these gains is energy efficiency: by aligning software features such as quantization and memory access patterns with hardware capabilities, systems can significantly reduce power consumption [5].

Predictability is paramount in real-time and safety-critical systems. Here, co-design plays a central role in mapping time-sensitive operations to hardware while allowing control logic to remain in software. This separation, coordinated through proper scheduling and analysis, ensures that timing constraints are satisfied without over-provisioning resources [6].

To achieve such results, co-design employs several core techniques:

- Partitioning, to determine which functions run in hardware (e.g., accelerators) versus software (e.g., general-purpose code) [6].
- Scheduling, which coordinates computation across processors, hardware units, and memory subsystems [6].
- Cross-layer optimization, where design decisions take into account constraints and capabilities across algorithm, architecture, and hardware levels [2].
- Design space exploration (DSE), used to evaluate many candidate configurations to find optimal trade-offs [7].

Looking forward, co-design is expected to play a growing role in addressing the demands of heterogeneous computing platforms and domain-specific accelerators. As systems scale in complexity, the integration of tools for neural architecture search, quantization-aware training, and hardware simulation becomes increasingly necessary [7]. These tools help automate the co-design process, making it more accessible and scalable.

In conclusion, hardware-software co-design enables efficient and principled development for modern computing systems. From edge AI to real-time control, this methodology improves energy efficiency, fairness, and overall performance. It offers a practical pathway to build systems that are not only more powerful but also more adaptable to the diverse and growing demands of modern applications [8][9].

References:

[1] Wolf, W. H. (2002). Hardware-software co-design of embedded systems. Proceedings of the IEEE, 82(7), 967-989.
[2] Bringmann, O., Ecker, W., Feldner, I., Frischknecht, A., Gerum, C., Hämäläinen, T., ... & Shafique, M. (2021, September). Automated HW/SW co-design for edge AI: State, challenges and steps ahead. In Proceedings of the 2021 International Conference on Hardware/Software Codesign and System Synthesis (pp. 11-20).
[3] Yang, C., Sheng, Y., Dong, P., Kong, Z., Li, Y., Yu, P., ... & Wang, Y. (2023, October). Fast and Fair Medical AI on the Edge Through Neural Architecture Search for Hybrid Vision Models. In 2023 IEEE/ACM International Conference on Computer Aided Design

(ICCAD) (pp. 01-09). IEEE.
[4] Sheng, Y., Yang, J., Wu, Y., Mao, K., Shi, Y., Hu, J., ... & Yang, L. (2022, July). The larger the fairer? small neural networks can achieve fairness for edge devices. In Proceedings of the 59th ACM/IEEE Design Automation Conference (pp. 163-168).
[5] Chen, Y. H., Krishna, T., Emer, J. S., & Sze, V. (2016). Eyeriss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks. IEEE journal of solid-state circuits, 52(1), 127-138.
[6] Yazdanbakhsh, A. (2025). Beyond Moore's Law: Harnessing the Redshift of Generative AI with Effective Hardware-Software Co-Design. arXiv preprint arXiv:2504.06531.
[7] Ponzina, F. (2023). Hardware-software co-design methodologies for edge AI optimization (Doctoral dissertation, EPFL).
[8] Yazdanbakhsh, A. (2025). Beyond Moore's Law: Harnessing the Redshift of Generative AI with Effective Hardware-Software Co-Design. arXiv preprint arXiv:2504.06531.
[9] Hooker, S. (2021). The hardware lottery. Communications of the ACM, 64(12), 58-65.

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES) features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor increased to 2.2 in 2023, more than doubling its value from 2020. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through the best paper and rookie of the year awards. Authors can send their paper submissions to the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Prabhat Mishra, Senior Associate Editor, at prabhat@ufl.edu

TODAES Special Issue Call for Papers

Special Issue on Co-Design and Design Automation for Optical/Photonic Computing Systems

This special issue seeks original submissions on pioneering research aimed at advancing co-design and EDA methodologies to support the modeling, simulation, design optimization, and physical implementation toward hybrid integration of optical computing/interconnect and electronic systems with high reliability, scalability, and efficiency. All these topics, as well as further potential topics mentioned below, are of interest to this special issue.

Important Dates

- Submissions deadline: Oct 15, 2025
- First-round review decisions: Dec 15, 2025
- Deadline for revision submissions: Jan 15, 2026

- Notification of final decisions: Feb 15, 2026
- Tentative publication: Spring 2026

Submissions should be made through the ACM TODAES submission site (http://mc.manuscriptcentral.com/todaes)

For questions and further information, please contact guest editors at:

- Jiaqi Gu, Arizona State University, jiaqigu@asu.edu
- Cunxi Yu, University of Maryland, cunxiyu@umd.edu
- Sudeep Pasricha, Colorado State University, sudeep@colostate.edu
- Xu Wang, Cadence Design Systems, xubc@cadence.com

More information can be found in this call for papers.

EDITOR'S PICK FROM ACM TODAES ISSUE 3, 2025

A Survey of Research in Large Language Models for Electronic Design Automation

Jingyu Pan[1], Guanglei Zhou[1], Chen-Chia Chang[1], Isaac Jacobson[1], Jiang Hu[2], Yiran Chen[1]

[1] Duke University, USA | [2] Texas A&M University, USA

Abstract: This article presents a comprehensive survey of Large Language Model (LLM) applications in Electronic Design Automation (EDA), analyzing how these models transform hardware design across system-level design, RTL design, logic synthesis, and physical design stages. Through analysis of over 40 recent research works, the survey reveals that domain-adapted LLMs with specialized fine-tuning significantly outperform general-purpose models, while autonomous agent frameworks demonstrate superior capabilities compared to single-shot generation methods. The paper identifies key innovations including multi-modal feature representations combining textual, graph-based, and image-based circuit data, custom tokenization for hardware description languages, and feedback-enhanced methodologies enabling autonomous design refinement. The analysis uncovers a performance correlation between model size and functional correctness, while advanced customization techniques achieve superior results even with smaller models. The survey categorizes application bottlenecks including data privacy concerns, domain adaptation challenges, and computational constraints, while highlighting promising research directions in explainable hardware design and multi-modal circuit understanding.

Continue reading more on ACM DL.

Technical Activities

1. AI Demand Drives Disaggregated Storage

The massive, exponential growth of AI data is driving the need for disaggregated storage, and Western Digital sees both hard drives and SSDs in the mix. The flurry of announcements are aimed at helping customers scale up flexible storage

infrastructures to meet the accelerated demands of AI, machine learning and data-heavy workloads as storage is pushed outside the confines of the server…

2. **Want A Smart Factory? It's All About the Data**
At last week's MES & Industry 4.0 conference in Porto, Portugal, the message was clear: production is king, and we can only make factories smart – and even intelligent as a next logical step – if you manage to unlock real value from the data to improve production without making the operator's job harder…

3. **Red Hat Taps APAC with Open-Source AI, Hybrid Cloud**
Red Hat has launched its AI Inference Server, a new product designed to make LLM deployment faster, more portable and easier to manage across hybrid cloud environments. The solution is part of both Red Hat OpenShift AI and Red Hat Enterprise Linux AI (RHEL AI) but is also available as a standalone offering. The company has also made OpenShift Virtualization now available across all major public cloud providers, positioning itself as a key partner for South Asian enterprises…

Job Positions

The University of Hong Kong, China

Job Title: Associate Professor/Assistant Professor of Microelectronics

Description: Applications are invited for appointment as Tenure-Track Associate Professor/Assistant Professor of Microelectronics in the Department of Mechanical Engineering (Ref.: 531059), to commence as soon as possible, on a three-year fixed-term basis, with the possibility of renewal and consideration for tenure before the expiry of a second three-year fixed-term contract. Applicants should possess a Ph.D. degree in a related engineering field, with an excellent research record. Candidates with industry experience or strong connections to the industry are preferred. The appointee is expected to conduct frontier research in next-generation microelectronics technology, deliver high-quality teaching to undergraduate and postgraduate students, engage in knowledge transfer activities, and provide administrative support to the University/Faculty/Department. He/She will also engage in unparalleled opportunities to interact with industrial partners and help reshape and elevate the microelectronics industry in one of the world's fastest-growing regions. For more information, please refer to https://engineeroxy.com/associate-professorassistant-professor-of-microelectronics,i14599.html.

University of Victoria, Canada

Job Title: Research Stream Faculty Positions at the Intersection of Software Engineering and AI

Description: We invite applications from talented scholars for one of four tenure-track positions at the assistant professor level working at the intersection of Software Engineering and AI, to commence January 1, 2026, or soon thereafter. Preferred: Prior teaching experience; Prior student supervision or mentoring; Evidence of collaboration and professionalism in academic environments; Complementary expertise to current faculty; Engagement with Generative AI and its

impact on SE practices. For more information, please refer to https://polytechnicpositions.com/research-stream-faculty-positions-at-the-intersection-of-software-engineering-and-ai,i13801.html.

Drexel University, US

Job Title: Assistant/Associate Professor of Information Science

Description: The Information Science Department invites applications with expertise in one or more specialized areas of information science at the rank of assistant or associate professor. Following the University's newly approved Non–Tenure-Track Full-Time Faculty Policy, the initial contract is for 2–3 years, and reappointment terms are typically longer. The University also offers numerous professional development opportunities for teachers, such as programming from the Teaching and Learning Center. Required Qualifications: Minimum of Master's Degree; Experience in teaching in both on-campus and online environments; Expertise in one or more specialized areas of information science, including computing security, information systems, and other areas relevant to our department's course programs; Broad knowledge in the cutting edge of information science and interest in promoting information science to a wide audience; A vision for interdisciplinary information science education in the 21st century. For more information, please refer to https://facultyvacancies.com/assistantassociate-professor-of-information-science,i42319.html.

Notice to authors