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SIGDA News

1. Nvidia looks to silicon photonics to cut datacentre AI power
Nvidia has worked with foundry TSMC for high speed optical interconnect to reduce the power consumption of AI datacentres with millions of GPUs. The first version of the technology will be used later this year for a MultiRing Module (MRM) that will then be used in the Spectrum-X switch in the second half of 2026.

2. Tiny pacemaker is powered by light
Engineers in the US have developed a pacemaker small enough to be injected into the body. The pacemaker developed at Northwestern University is aimed at the tiny, fragile hearts of newborn babies with congenital heart defects.

3. TSMC opens up 2nm wafer fab, races to mass production
Foundry chipmaker TSMC held an expansion ceremony for 2nm at its second module at Fab 22 in Kaohsiung on Monday March 31, aiming for a manufacturing capacity of 30,000 wafer starts per month by year end.

4. imec to set up €40m chiplet development centre in Germany
imec is to set up a centre in Germany to develop automotive chiplet technology. The Advanced Chip Design Accelerator (ACDA) will be based in Baden-Württemberg, southwest Germany, following backing of €40m over the next five years.

5. Quantum computing shows strong growth into the datacenter
The market for quantum computing, communications and sensing technology was worth US$954 million in 2024 and will grow by about 15 percent to about US$1.1 billion in 2025, according to Yole.

6. Hardware to dominate $260bn edge AI spending
Global spending on edge AI is set to top $260 billion this year and grow 13.8% a year to reach $380bn by 2028. The report from IDC sees the largest sector is still

Message from the EiC

Dear Readers,

In this edition, we bring you the latest news and activities in our community, upcoming conferences, paper deadlines, an insightful article on What is AI driven Chip Design, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

hardware until 2028 from the move to edge AI accelerator chips for real time processing.

7. Compostable sensors for digital agriculture
Compostable, screen-printed soil sensors are being used to monitor crops in the UK as part of a pan-European 'digital agriculture' project. The system combines a screen-printed biodegradable impedance sensor with a reusable electronic module powered by a solar cell.

8. Turning smartphone sensors into an antimatter camera
A team from the Technical University of Munich, has repurposed smartphone camera sensors to create a detector capable of imaging antiproton annihilations in real time.

SIGDA Awards

1. Best Paper Award @ ISFPGA 2025
https://www.isfpga.org/

FlightVGM: Efficient Video Generation Model Inference with Online Sparsification and Hybrid Precision on FPGAs

Jun Liu[1], Shulin Zeng[2,3], Li Ding[1], Widyadewi Soedarmadji[2], Hao Zhou[1], Zehao Wang[2], Jinhao Li[1], Jintao Li[3], Yadong Dai[3], Kairui Wen[3], Shan He[3], Yaqi Sun[3], Yu Wang[2], Guohao Dai[1,3]

[1] *Shanghai Jiao Tong University* | [2] *Tsinghua University* | [3] *Infinigence-AI*

2. ISPD Best Paper Award @ ISPD 2025
https://www.acm.org/conferences/best-paper-awards

Cypress: VLSI-Inspired PCB Placement with GPU Acceleration

Niansong Zhang[1], Anthony Agnesina[2], Noor Shbat[2], Yuval Leader[2], Zhiru Zhang[1] and Haoxing Ren[2]

[1] *Cornell University* | [2] *NVIDIA*

3. ISPD Lifetime Achievement Award @ ISPD 2025
https://ispd.cc/ispd2024/index.php?page=awards

Prof. Jason Cong

The 2025 International Symposium on Physical Design pays tribute to Prof. Jason Cong for his contributions to the physical design community.

SIGDA E-News Editorial Board

What is

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What is AI-Driven Chip Design?

Banafsheh Saber Latibari

University of Arizona

With the growing demand for efficient chips, the design process has become increasingly challenging. Designers must meet many design constraints, including power consumption, area, performance, thermal management, verification and security. The process involves iterative refinement leading to an increase in time to market and design cost, plus there is a possibility of human error and failure to consider all the scenarios that may affect the functionality of the design later. AI is revolutionizing different applications, from natural language processing, computer vision to healthcare, education and autonomous vehicles. AI models are able to digest vast amounts of data and find patterns and make decisions. As a result, researchers have decided to apply AI models to different stages of chip design to resolve these challenges.

Physical design and timing closure are challenging tasks. To perform timing analysis, AI models such as BiLSTM have been proposed as a replacement for Path-Based timing Analysis (PBA) [1]. During the Clock Tree Synthesis (CTS), physical design tools optimize the design to achieve zero skew. However, it causes a simultaneous switching and clock transition at the clock pin of all registers resulting in significant voltage drop. Reinforcement Learning (RL) [2] has been leveraged to optimize the CTS process by updating the clock arrival time of each register through the following actions: adding a buffer, removing a buffer, or no action. AI can also assist with vulnerability detection in hardware [3, 4].

With the introduction of Transformers [5] and Large Language Models (LLMs) such as GPT [6], their application in code generation, has gained significant attention [7]. Inspired by this, researchers proposed CHIPChat, a GPT-based model for hardware description language generation to design circuits at the RTL level using Verilog [8]. This research marked the beginning of a new era, and LLMs have since been used for debugging [9], verification [10], and, more recently, securing the design [11].

In the industry, tech giants such as NVIDIA [12], Google [13], Synopsys [14], and Cadence [15], have integrated AI into their hardware design process and are focusing on advancing their design process capabilities by leveraging LLMs. Moreover, startup companies such as PrimisAI have emerged offering LLM-based solutions for chip development.

In summary, AI is speeding up the chip development process and reducing design cost. However, generative AI based tools still need improvement which could be achieved through enriching the available datasets throughout the entire design cycle, from code generation to layout design, verification and testing. So by introducing new AI models each day, we should anticipate further innovation in chip design.

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Paper Deadlines

RTCSA'25 - The 30th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications
Singapore
Deadline: Apr. 05, 2025
Aug. 20-22, 2025
https://rtcsa2025.github.io/

ICECET'25 - IEEE International Conference on Electrical, Computer and Energy Technologies
Paris, France
Deadline: Apr. 10, 2025
July 03-06, 2025
www.icecet.com

MICRO'25 – IEEE/ACM Int'l Symposium on Microarchitecture
Austin, TX, USA
Deadline: Apr. 11, 2025
(Abstracts due: Apr. 4, 2025)
Oct. 18-22, 2025
https://microarch.org/micro58/

ICCAD'25 – IEEE/ACM Int'l Conference on Computer-Aided Design
Munich, Germany
Deadline: Apr. 21, 2025
(Abstracts due: Apr. 14, 2025)
Oct. 26-30, 2025
https://2025.iccad.com/

VLSI-SoC'25 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Puerto Varas, Chile
Deadline: April 25, 2025
(Abstracts due: April 18, 2025)
Oct. 12-15, 2025
https://asic-chile.cl/vlsisoc/

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OSCAR'25 - Fourth Workshop on Open-Source Computer Architecture Research
Tokyo, Japan (co-located with ISCA 2025)
Abstract deadline: May 5, 2025
June 21, 2025
https://oscar-workshop.github.io/

ICCD'25 – IEEE Int'l Conference on Computer Design
Dallas, TX, USA
Deadline: May 11, 2025
(Abstracts due: May 4, 2025)
Nov. 10-12, 2025
http://www.iccd-conf.com

MLCAD'25 - ACM/IEEE International Symposium on Machine Learning for CAD
Chaminade Resort, Santa Cruz, CA, USA
Deadline: May 23, 2025
(Abstract due: May 16, 2025)
Sep. 8-10, 2025
https://mlcad.org/symposium/2025/

Upcoming Conferences

ISQED'25 - Int'l Symposium on Quality Electronic Design
San Francisco, CA, USA
Apr. 9-11, 2025
http://www.isqed.org

FCCM' 25 - IEEE International Symposium On Field-Programmable Custom Computing Machines
Fayetteville, AR, USA
May 4-7, 2025
https://www.fccm.org/

HOST'25 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
San Jose, CA, USA
May 5-8, 2025
http://www.hostsymposium.org

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES) features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor rose to 2.2 in 2023, more than doubling its 2020 value. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through best paper and rookie of the year award. Authors can send their paper submissions on the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

Technical Activities

1. Micron Drives Down DRAM Power
Reducing DRAM's power footprint has always been table stakes for vendors like Micron Technology, but AI-driven data centers are putting more pressure on memory makers to make further advances in power efficiency…

2. Synopsys: Autonomous AI Agents to Tame Chip Design Complexity
At the annual Synopsys SNUG conference here in Santa Clara, Calif., the company's CEO Sassine Ghazi spelled out the path to using AI agents to "tame" the increasing complexity of chip design…

3. Memory Safety is Key to Addressing Cyber Security
Earlier this month, a U.K. government initiative called Digital Security by Design (DSbD) held a showcase in London to enable companies with pioneering technologies to demonstrate their products, technologies and solutions that could tackle a perceived market failure in integrating fundamental hardware security and, ultimately, reduce the economic impact of cyber major security breaches caused by memory safety vulnerabilities…

4. Wolfspeed: Delivering Efficiency and Durability in Cost-Optimized Systems
Wolfspeed's Gen 4 SiC MOSFET technology improves switching behaviors and design challenges commonly experienced in high-power designs…

RTAS'25 - IEEE Real-Time and Embedded Technology and Applications Symposium
Irvine, CA, USA
May 6-9, 2025
http://2025.rtas.org

MDTS'25 – IEEE Microelectronics Design & Test Symposium
Albany, NY, USA
May 19-21, 2025
http://natw.ieee.org

ISCAS'25 – IEEE Int'l Symposium on Circuits and Systems
London, United Kingdom
May 25-28, 2025
https://2025.ieee-iscas.org/

DAC'25 – Design Automation Conference
San Francisco, CA, USA
June 22-25, 2025
http://www.dac.com/

GLSVLSI'25 – ACM Great Lakes Symposium on VLSI
New Orleans, LA, USA
June 30 - July 2, 2025
http://www.glsvlsi.org

ICECET'25 - IEEE International Conference on Electrical, Computer and Energy Technologies
Paris, France
July 3-6, 2025
www.icecet.com

ISVLSI'25 – IEEE Computer Society Annual Symposium on VLSI
Kalamata, Greece
July 6-9, 2025
http://www.ieee-isvlsi.org

Job Positions

University of California Irvine, US

Job Title: Postdoctoral Scholar in Computer Science

Description: The Department of Computer Science at UC Irvine anticipates openings for Postdoctoral Scholars. A compelling research portfolio in an area related to Computer Science is preferred. Use this link to explore research areas and faculty who may sponsor appointments: https://www.cs.uci.edu/cs-research-areas/. A doctoral degree (e.g., Ph.D.) or a foreign equal is required. Positions are dependent on extramural funding and research contracts of individual Principal Investigators. The initial appointment is for two years. Renewal is based on the availability of support and need. The start date is negotiable. A reasonable estimate for this position is $64,480 - $77,237. The total service as a postdoctoral scholar can not exceed five years. This includes postdoctoral service at other institutions.

CISPA, Germany

Job Title: Positions in Computer Science

Description: CISPA is a world-leading research center that focuses on Information Security and Artificial Intelligence at large. To expand and further strengthen our center, we are looking for a Tenure-Track Faculty in all areas related to Information Security and Artificial Intelligence. All applicants are expected to grow a research team that pursues an internationally visible research agenda. To aid you in achieving this, CISPA provides institutional base funding for three full-time researcher positions and a generous budget for expenditures. Upon successful tenure evaluation, you will hold a position that is equivalent to an endowed full professorship at a top research university.

In view of the current geopolitical landscape and in order to further strengthen research in information security and trustworthy AI in Germany and Europe, we have decided to invite a further round of applications of renowned candidates with an outstanding track record in Information Security, Artificial Intelligence, or related areas, including Cybersecurity and Privacy, Machine Learning and Data Science, Efficient Algorithms and Foundations of Theoretical Computer Science, Software Engineering, Program Analysis and Formal Methods. The application deadline is April 8, 2025 23:59 AoE with interviews starting in mid April 2025. For more information, please refer to https://computeroxy.com/tenure-track-faculty-in-all-areas-related-to-information-security-and-artificial-intelligence-fmd-extended-call,i15642.html.

University of Cambridge, UK

Job Title: Research Assistant in AI Education

Description: We are looking for a Research Assistant to join the Raspberry Pi Computing Education Research Center (RPCERC) in the Department of Computer Science and Technology. The Research Assistant will work together with other

researchers and students in the field of AI education on developing our understanding of curriculum concepts and pedagogical strategies that underpin the teaching and learning of AI to young people. As a Research Assistant within our team, you will play a key part in data collection and analysis, working collaboratively with other researchers. You will support the development of resources for teaching AI to young people, and potentially be involved in the development of learning environments that support AI literacy in an age-appropriate way. You will also be part of the wider team and be willing to support other computing education projects within the RPCERC as needed. The person we are looking for will have a keen interest in AI education as well as a good technical understanding of AI technologies. For more information, please refer to https://facultyvacancies.com/research-assistant-in-ai-education,i41543.html.

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