Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 55, No. 3

SIGDA - The Resource for EDA Professionals

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
Circulation: 2,700

Online archive: https://www.sigda.org/publications/newsletter

SIGDA News

1. €100bn European Deal for Cleantech, Battery Recycling
The European Commission is aiming to boost the development and scaling up of clean technologies and recycling of materials in a €100bn 'clean industrial deal' and a Circular Economy Act.

2. Amazon Announces 'Ocelot' Bosonic Quantum Chip
Amazon Web Services (AWS) has announced its first-generation superconducting quantum device called Ocelot, which it claims has a scalable architecture that can reduce the need for error correction by up to 90 percent.

3. R&S, Nvidia Team on AI-Driven 6G Wireless Research
A proof of concept system to be shown at the Mobile World Congress next month with a framework for testing 5G-Advanced and 6G neural receivers under realistic propagation conditions using digital twin technology.

4. Nvidia Preps Blackwell Ultra, Vera, Rubin Chips
Following the mishap with the production of the latest Blackwell chip, Nvidia's chief executive says it is on track to ship the Blackwell Ultra chip later this year, followed by its next-generation processor and GPU, codenamed Vera and Rubin.

5. GlobalFoundries, MIT Team on Photonic AI Chips
GlobalFoundries has expanded its work with the Massachusetts Institute of Technology (MIT) on silicon photonics.

6. Europe clears Nokia's $2.3bn Infinera AI takeover at the last minute
The European Commission has approved the $2.3bn acquisition by Nokia of US competitor Infinera by Nokia in the nick of time.

Message from the EiC

Dear Readers,

In this edition, we bring you the latest news and activities in our community, upcoming conferences, paper deadlines, an insightful article on What is Logic Locking, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

7. **First Monolithic Quad-Band Satellite Receiver for Industrial, Automotive**
STMicroelectronics has developed the first quad-band monolithic satellite navigation receiver for automotive and industrial applications.

8. **First ARMv9 processor for edge AI is 'Fundamental Shift'**
The move to a microprocessor rather than a microcontroller is all about memory management for AI frameworks. UP to four ARM Cortex-A320 cores can be clustered together with a U85 neural processing unit (NPU) for an embedded processor.

SIGDA Awards

Best Paper Award @ ASP-DAC 2025

"ViDA: Video Diffusion Transformer Acceleration with Differential Approximation and Adaptive Dataflow"

Li Ding, Jun Liu, Shan Huang, Guohao Dai

Shanghai Jiao Tong Univ., China

"A Practical Randomized GMRES Algorithm for Solving Linear Equation System in Circuit Simulation"

Baiyu Chen, Jiawen Cheng, Wenjian Yu

Tsinghua Univ., China

What is

Contributing author: Yuntao Liu <yule24@lehigh.edu>
AE: Han Wang <han.wang.hw@temple.edu>

What is Logic Locking?

Yuntao Liu

Lehigh University

Due to the increasing cost of maintaining IC foundries with advanced technology nodes, many chip designers have become fabless and outsource their fabrication to off-shore foundries. However, such foundries are not under the designer's control which puts the security of the IC supply chain at risk. Untrusted foundries are capable of malicious activities, including hardware

SIGDA E-News Editorial Board

Trojan insertion, piracy, counterfeiting, overbuilding, etc. Many design-for-trust techniques have been studied as countermeasures, among which logic locking has been the most widely studied [1]. A logic-locked circuit requires a secret key input and the correct key is kept by the designer and not known to the foundry. The functionality of the circuit is correct only if the key is correct. After the foundry manufactures the locked circuit and returns it to the designer, the correct key is applied to the circuit by connecting a tamper-proof memory containing the key to the key inputs. This process is called activation. Over the years, different types of logic locking mechanisms have been suggested. Each protection technique is intended for a specific model of the adversary's capabilities and resources, which can be broadly differentiated by whether the adversary has access to a working chip (i.e., a chip supplied with the correct key).

An adversary without access to a working chip has the layout, and hence gate-level netlist, of the chip being manufactured. The earliest research in IC IP protection considered this threat model. The techniques proposed generally used XOR/XNOR gates, multiplexers (MUX), or look-up tables (LUT) [2-5]. Follow-up studies used fault analysis to guide the insertion of key-controlled logic gates to achieve an average output error of 50% Hamming Distance (HD) compared to the correct output given incorrect keys [6-9].

Working chips can be used by adversaries as oracles to obtain the correct output for any given input. Hence, attack methods requiring such an oracle are called oracle-guided attacks. The first oracle-guided attack was based on Boolean satisfiability theory, called the SAT attack [10}. This attack was a game changer in the field and was able to break any prior circuit IP protection approaches, such as those based on XOR/XNOR gates [2-3] or LUTs [4-5]. The SAT attack requires read-and-write access to internal flip-flops on the working chip, which is usually achieved by accessing the chip's scan chain in the test mode. If scan chain access is not available, sequential SAT-based formulations, such as model checkers, can be used to facilitate the attack [11-13].

Besides the Boolean functionality of a circuit, locking can be incorporated by introducing setup or hold time violations with wrong keys [14, 15]. Since Boolean SAT formulas cannot incorporate timing information, this approach is immune to the SAT attack.

Based on the perceived threats faced by the chip design, logic locking techniques should be chosen carefully to balance the cost and resilience to applicable attack methods.

References:

[1] Chakraborty, Abhishek, et al. "Keynote: A disquisition on logic locking." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 39.10 (2019): 1952-1972.
[2] Roy, Jarrod A., Farinaz Koushanfar, and Igor L. Markov. "EPIC: Ending piracy of integrated circuits.", DATE. 2008.
[3] Rajendran, Jeyavijayan, et al. "Security analysis of logic obfuscation." DAC 2012.
[4] Baumgarten, Alex, Akhilesh Tyagi, and Joseph Zambreno. "Preventing IC piracy using reconfigurable logic barriers." IEEE Design & Test of computers 27.1 (2010)
[5] Khaleghi, Soroush, Kai Da Zhao, and Wenjing Rao. "IC piracy prevention via

Paper Deadlines

ISLPED'25 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
University of Iceland, Iceland
Deadline: Mar. 10, 2025 (Abstracts due: Mar. 3, 2025)
Aug. 6-8, 2025
http://www.islped.org

IWLS'25 - International Workshop on Logic & Synthesis
Verona, Italy
Deadline: Mar. 28, 2025 (Abstracts due: Mar. 21, 2025)
June 12-13, 2025
https://www.iwls.org

ESWEEK'25 - Embedded Systems Week
Taipei, Taiwan
Deadline: Mar. 30, 2025 (Abstracts due: Mar. 23, 2025)
Sept. 28 - Oct. 3, 2025
http://www.esweek.org

ICCD'25 – IEEE Int'l Conference on Computer Design
Dallas, TX, USA
Deadline: May 11, 2025 (Abstracts due: May 4, 2025)
Nov. 10-12, 2025
http://www.iccd-conf.com

MLCAD'25 - ACM/IEEE Workshop on Machine Learning for CAD
Santa Cruz, CA, USA
Deadline: May 23, 2025 (Abstracts due: May 16, 2025)
Sep. 8-10, 2025
https://mlcad-workshop.org

design withholding and entanglement.", ASPDAC 2015.
[6] Rajendran, Jeyavijayan, Huan Zhang, Chi Zhang, Garrett S. Rose, Youngok Pino, Ozgur Sinanoglu, and Ramesh Karri. "Fault analysis-based logic encryption." IEEE Transactions on computers 64, no. 2 (2013): 410-424.
[7] Lee, Yu-Wei, and Nur A. Touba. "Improving logic obfuscation via logic cone analysis." In 2015 16th Latin-American Test Symposium (LATS), pp. 1-6. IEEE, 2015.
[8] Alasad, Qutaiba, Yu Bi, and Jiann-Shuin Yuan. "E2LEMI: energy-efficient logic encryption using multiplexer insertion." Electronics 6, no. 1 (2017): 16.
[9] Karousos, Nikolaos, Konstantinos Pexaras, Irene G. Karybali, and Emmanouil Kalligeros. "Weighted logic locking: a new approach for IC piracy protection." In 2017 IEEE 23rd International Symposium on On-Line Testing and Robust System Design (IOLTS), pp. 221-226. IEEE, 2017.
[10] Subramanyan, Pramod, Sayak Ray, and Sharad Malik. "Evaluating the security of logic encryption algorithms." In 2015 IEEE International Symposium on Hardware Oriented Security and Trust (HOST), pp. 137-143. IEEE, 2015.
[11] El Massad, Mohamed, Siddharth Garg, and Mahesh Tripunitara. "Reverse engineering camouflaged sequential circuits without scan access." In ICCAD 2017.
[12] Shamsi, Kaveh, Meng Li, David Z. Pan, and Yier Jin. "KC2: Key-condition crunching for fast sequential circuit deobfuscation." In DATE 2019.
[13] Azar, Kimia Zamiri, Hadi Mardani Kamali, Farimah Farahmandi, and Mark Tehranipoor. "Warm up before circuit de-obfuscation? An exploration through bounded-model-checkers." In 2022 IEEE International Symposium on Hardware Oriented Security and Trust (HOST), pp. 13-16. IEEE, 2022.
[14] Xie, Yang, and Ankur Srivastava. "Delay locking: Security enhancement of logic locking against IC counterfeiting and overproduction." In Proceedings of the 54th Annual Design Automation Conference 2017, pp. 1-6. 2017.
[15] Chakraborty, Abhishek, Yuntao Liu, and Ankur Srivastava. "Evaluating the security of delay-locked circuits." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 40, no. 4 (2020): 608-619.

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES) features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor rose to 2.2 in 2023, more than doubling its 2020 value. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through best paper and rookie of the year award. Authors can send their paper submissions on the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

Upcoming Conferences

ISPD'25 – ACM Int'l Symposium on Physical Design
Austin, TX, USA
Mar. 16-19, 2025
http://www.ispd.cc

DATE'25 - Design Automation and Test in Europe
Lyon, France
Mar. 31 - April. 2, 2025
http://www.date-conference.com

ISQED'25 - Int'l Symposium on Quality Electronic Design
San Francisco, CA, USA
Apr. 9-11, 2025
http://www.isqed.org

FCCM' 25 - IEEE International Symposium On Field-Programmable Custom Computing Machines
Fayetteville, AR, USA
May 4-7, 2025
https://www.fccm.org/

HOST'25 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
San Jose, CA, USA
May 5-8, 2025
http://www.hostsymposium.org

RTAS'25 - IEEE Real-Time and Embedded Technology and Applications Symposium
Irvine, CA, USA
May 6-9, 2025
http://2025.rtas.org

MDTS'25 – IEEE Microelectronics Design & Test Symposium
Albany, NY, USA
May 19-21, 2025
http://natw.ieee.org

EDITOR'S PICK FROM ACM TODAES ISSUE 1, 2025

A Cascaded ReRAM-based Crossbar Architecture for Transformer Neural Network Acceleration

Jiahong Xu, Haikun Liu, Xiaoyang Peng, Zhuohui Duan, Xiaofei Liao, and Hai Jin

Huazhong University of Science and Technology, Wuhan, China

Abstract: Emerging resistive random-access memory (ReRAM) based processing-in-memory (PIM) accelerators have been increasingly explored in recent years because they can efficiently perform in-situ matrix-vector multiplication (MVM) operations involved in a wide spectrum of artificial neural networks. However, there remain significant challenges to applying existing ReRAM-based PIM accelerators to the most popular Transformer neural networks. Since Transformers involve a series of matrix-matrix multiplication (MatMul) operations with data dependencies, they should write intermediate results of MatMuls to ReRAM crossbar arrays for further processing. Conventional ReRAM-based PIM accelerators often suffer from high latency of ReRAM writes and intra-layer pipeline stalls.

In this paper, we propose ReCAT, a ReRAM-based PIM accelerator designed particularly for Transformers. ReCAT exploits transimpedance amplifiers (TIAs) to cascade a pair of crossbar arrays for MatMul operations involved in the self-attention mechanism. The intermediate result of a MatMul generated by one crossbar array can be directly mapped to another crossbar array, avoiding costly analog-to-digital conversions. In this way, ReCAT allows MVM operations to overlap with the corresponding data mapping, hiding the high latency of ReRAM writes. Furthermore, we propose an analog-to-digital converter (ADC) virtualization scheme to dynamically share scarce ADCs among a group of crossbar arrays, and thus significantly improve the utilization of ADCs to eliminate the performance bottleneck of MVM operations. Experimental results show that ReCAT achieves 207.3×, 2.11×, and 3.06× performance improvement on average compared with other Transformer acceleration solutions—GPUs, ReBert, and ReTransformer, respectively.

Continue reading more on ACM DL.

Call for Special Issue on Machine Learning for CAD

Guest Editors:

- Yibo Lin, Peking University, yibolin@pku.edu.cn
- Siddharth Garg, New York University, sg175@nyu.edu
- Hussam Amrouch, Technical University of Munich (TUM), amrouch@tum.de

Advances in machine learning (ML) over the past half-dozen years have revolutionized the effectiveness of ML for a variety of applications. However,

ISCAS'25 – IEEE Int'l Symposium on Circuits and Systems
London, United Kingdom
May 25-28, 2025
https://2025.ieee-iscas.org/

DAC'25 – Design Automation Conference
San Francisco, CA, USA
June 22-25, 2025
http://www.dac.com/

GLSVLSI'25 – ACM Great Lakes Symposium on VLSI
New Orleans, LA, USA
June 30 - July 2, 2025
http://www.glsvlsi.org

ICECET'25 - IEEE International Conference on Electrical, Computer and Energy Technologies
Paris, France
July 3-6, 2025
www.icecet.com

ISVLSI'25 – IEEE Computer Society Annual Symposium on VLSI
Kalamata, Greece
July 6-9, 2025
http://www.ieee-isvlsi.org

design processes present challenges that require parallel advances in ML and CAD as compared to traditional ML applications such as image classification.

This special issue seeks original submissions on ML applications to the entire design flow – including ML applications to validation and testing. The application of machine learning to mask preparation and layout generation are topics that are seeing very active research recently. ML is also being applied to improve the robustness of integrated circuits and systems. Power and thermal management are probably the most important limiting factors for ICs today. - ML-based techniques are being explored to address this bottleneck. All these topics, as well as further potential topics mentioned below, are of interest to this special issue.

In addition to submissions from academia, submissions from industry are much welcome.

Authors are encouraged to submit high-quality original research contributions. Please clearly identify the additional material from any original conference or workshop paper in your submitted manuscript. Submissions should be made through the ACM TODAES submission site (http://mc.manuscriptcentral.com/todaes) and formatted according to TODAES author guidelines that can be found at: https://dl.acm.org/journal/todaes/author-guidelines. Select the paper type "Special Issue on Machine Learning for CAD".

Technical Activities

1. New Quantum Computing Breakthrough by Microsoft

Microsoft has unveiled its Majorana 1 chip, marking a notable development in quantum computing. This chip uses a topological qubit architecture, distinguishing it from other approaches in the field and opening new avenues for scalability and stability…

2. EDA Tool Preserves Floorplan, Intelligence in Analog IP Design Migration

This week, U.K.-based Thalia Design Automation plans to release the latest version of its analog IP design migration EDA tool suite to ensure that a migrated layout maintains the existing floorplan, hence ensuring DRC/ LVS integrity. Its Amalia suite, claiming to be the first AI-powered, end-to-end analog IP reuse platform, uses a custom AI design transformer engine for analog physical implementation, leveraging the source layout and PDK to reliably achieve migration design time savings of up to 40%, according to the company…

3. Startup Positron Takes On Nvidia With FPGAs

Data center AI systems startup Positron, just 18 months old, has been shipping its FPGA-based LLM inference systems to customers since last summer, and recently delivered the first systems in a multi-million-dollar order to its Tier 2 CSP customer…

4. Apple Gets Its Own Cellular Modem to Market
This week, a significant piece of news was the launch by Apple of its iPhone 16e, which features the first cellular modem designed by Apple, the C1…

Job Positions

Toronto Metropolitan University, Canada

Job Title: Assistant Professor in Electrical Engineering

Description: The Department of Electrical, Computer, and Biomedical Engineering in the Faculty of Engineering and Architectural Science at Toronto Metropolitan University invites applications for a tenure track position at the rank of Assistant Professor in electrical engineering with the focus on electromagnetic and/or photonic devices, circuits, and systems effective July 1, 2025, subject to final budgetary approval. Applications from candidates who self identify as a member of an underrepresented group, as recognized by Tri-Council Agencies, are particularly encouraged, and such candidates are encouraged to self identify through our Applicant Diversity Self-ID questionnaire. Applications must be received by March 15, 2025. The successful candidate will engage in a combination of teaching, scholarly research, and service duties while maintaining an inclusive, equitable, and collegial work environment across all activities. Teaching duties will entail teaching at undergraduate and graduate levels, supervision of graduate and undergraduate students, curriculum development, and contribution to the curricular strength of the department. The successful candidate will develop a strong, innovative, independent research program that is externally funded and that produces cutting-edge, high-quality results. The candidate is expected to provide service to the University and engineering profession. The candidates must hold a Ph.D. degree in Electrical Engineering or Computer Engineering by the appointment date. For more information, please refer to https://facultyvacancies.com/lecturer-in-electrical-engineering,i41211.html.

Lund University, Sweden

Job Title: Positions in Computer Science

Description: There is a growing research group in foundations of computer science at Lund University. We expect to have 8 PhD students by the autumn, in addition to three faculty and two postdocs.
At the heart of computational complexity theory is the quest to understand the nature of efficient computation. What makes a problem computationally hard or easy? How can we show that every algorithm that solves a certain problem must necessarily consume a large amount of resources (such as time or memory, say)? The study of the potential and limits of efficient computation is about foundational, mathematical, research, but research results in computational complexity theory have had major impact in other areas of computer science and other scientific disciplines, and have given rise to some of the most important open problems in modern mathematics.

The main duties involved in a post-doctoral position is to conduct research. Teaching may also be included, but up to no more than 20% of working hours. The position includes the opportunity for three weeks of training in higher education teaching and learning. The purpose of the position is to develop independence as a researcher and to create the opportunity of further development. The postdoc is expected to collaborate with PhD students in the group and can be asked to assist with supervising degree projects. For more information, please refer to https://facultyvacancies.com/postdoctor-position-in-computer-science,i41332.html.

University of Manchester, UK

Job Title: Research Associate in Electronic Engineering

Description: A researcher at the postdoctoral level (i.e., holding a PhD or doctorate) with a strong track record of relevant research and an appetite for tackling real-world robotics and autonomous system problems is required for this position within the CRADLE Prosperity Partnership. The CRADLE Prosperity Partnership is a significant joint activity between Amentum, the Manchester Centre for Robotics and AI, and the UKRI. The successful candidate will primarily work on robot state estimation and sensor fusion for various robots and sensors. They will work on theoretical and practical state estimation problems applied to ground robots (wheeled, tracked, legged), mobile manipulators, and aerial and aquatic robots as required by the CRADLE research programme. They will interact with other work packages to integrate the developed state estimators into a broader system architecture for robots expected to work in challenging environments. Successful candidates are expected to assist in field trials, engage with potential industrial partners, and translate complex mathematical concepts into real-world applications. For more information, please refer to https://facultyvacancies.com/research-associate-in-electronic-engineering,i41326.html.

Notice to authors