Special Interest Group on Design Automation
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SIGDA - The Resource for EDA Professionals

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
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SIGDA News

1. Farewell to the US CHIPS Act
The US CHIPS and Science Act is not expected to last long as the new President takes over. Despite being agreed by both Democrats and Republicans, the new administration is not a fan of the Act and its spending.

2. US Sets the Science and Technology Advisory Council
The new US administration is setting up a science and technology advisory council focusing on AI, 5G, and driverless cars.

3. European 1nm, Photonics Chip Pilot Lines Launch
The heads of four leading research institutes in Europe have met up for the launch of the first five EU Chips Act pilot lines.

4. ARM Boost in $100bn Stargate Data Centre Project
ARM and its owner Softbank are key partners in a data center infrastructure program called Stargate.

5. Quantinuum to Build Photonic Quantum R&D Centre in New Mexico
Quantinuum was formed from the merger of Cambridge Quantum Computing in the UK and Honeywell's quantum business. It is the largest dedicated quantum technology company with 550 staff members.

6. MediaTek Adopts AI-Driven Cadence Tools for 2nm Designs
Cadence has announced that MediaTek has adopted the AI-driven Cadence® Virtuoso® Studio and Spectre® X Simulator on the NVIDIA accelerated computing platform for its 2nm development.

7. Meta Taps Singular Photonics for Single Photon Image Sensors
A startup in Scotland has been working with tech giant Meta on an ultra-sensitive sensor for wearables.

Message from the EiC

Dear Readers,

In this edition, we bring you the latest news and activities in our community, upcoming conferences, paper deadlines, an insightful article on what is a Digital Twin, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

8. ARM Cortex-M4-based MCUs Target Motor Control Applications
Toshiba Electronics Europe GmbH has introduced seven new 32-bit microcontrollers (MCUs) with Arm® Cortex®-M4 cores, expanding its motor control lineup.

9. Self-Supervised Memristor AI Chip
Researchers in South Korea have developed a self-supervised neuromorphic AI processor using a memristor array to learn and process data.

10. Camera inspired by Insect Vision Hits 1920 Frame/s
Researchers in South Korea have developed a high-speed camera that can operate in low light based on the visual system of insects.

What is

Contributing author: Vijaykrishnan Narayanan <vijaykrishnan.narayanan@psu.edu>
AE: Muhammad Shafique <muhammad.shafique@nyu.edu>

What are Digital Twins? Accelerating Innovation in Chip Design and Manufacturing

Vijaykrishnan Narayanan,
The Pennsylvania State University

The quest for more powerful processors and denser memory chips continues to accelerate with the advent of data-intensive machine learning workloads. With traditional scaling at its limit, a complex combination of materials, process, device and packaging innovations are critical for enabling this computational need. Developing and optimizing such new semiconductor technologies is time-consuming and costly. For example, recent data shows that the cost of moving to new process nodes has become prohibitive; wafer costs increase by 50% for 2 nm compared to 3 nm feature sizes, and the foundry cost quadruples from five billion dollars for the 3 nm logic technology node to around 20 billion for a new 2 nm logic fabrication facility. The limited capacity to support these large investments is already impacting economic growth and lead times for acquiring leading-edge AI hardware. The seemingly conflicting requirement, securing cost-competitiveness and producing the highest-value-added computing technologies, presents a daunting task. The use of simulation tools and hierarchical abstractions is a widely adopted methodology for predictive exploration of chip designs even before they are fabricated in the electronic design automation (EDA) community. Building on this EDA foundation and the power of data-driven machine learning innovation, the concept of digital twins for semiconductors is emerging as a cost-effective option for both developing new processes as well as training the next generation of workforce. A digital twin involves developing a data-driven virtual model that dynamically evolves through interaction with a deeply instrumented physical system in a fab. The digital twins can allow experimentation of a wide range of what if scenarios in the virtual world while limiting the number of expensive and time-consuming physical experiments.

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Data collection for a digital twin involves integrating processing equipment with sensors such as thermal and pressure sensors and monitoring the electrical and mechanical properties of the resulting chips/wafers processed through various techniques including microscopic imaging and electrical probe measurements. Data gathered using this technique is used to build predictive virtual models. For example, the ability to predict the electrical characteristics of a ferroelectric memory device given the process conditions of its fabrication is being pursued by my research team along with collaborators with expertise in device fabrication and material science. The broader goal is to develop new process recipes for simultaneously tuning various metrics of a new memory device including speed, power and endurance. There are various challenges in building such a virtual model for a completely new process or new device. First, the available instrumented data for the virtual model is either sparse or non-existent for the developing new process. Techniques such as transfer learning that uses data from older or related technology nodes and physics-informed machine learning approaches that leverage physical constraints to learn better with fewer data are being explored. Further, the use of traditional simulation approaches can be used to augment the physically measured data. However, this requires the incorporation of machine learning approaches that consider the varying fidelity of the simulation generated data and physical measurements. Digital twins are an exciting new opportunity for innovations from our EDA community.

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES) features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor rose to 2.2 in 2023, more than doubling its 2020 value. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through best paper and rookie of the year award. Authors can send their paper submissions on the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

CALL FOR BEST PAPER AWARD NOMINATIONS

Deadline: February 8, 2025

All papers published in the ACM TODAES between January 2024 and December 2024 are eligible. The best paper will be selected based on originality, timeliness, potential impact, and quality.

Both nominations by peers and self-nominations are welcome.

Paper Deadlines

ISVLSI'25 – IEEE Computer Society Annual Symposium on VLSI
Kalamata, Greece
Deadline: Feb. 10, 2025
July 6-9, 2025
http://www.ieee-isvlsi.org

GLSVLSI'25 – ACM Great Lakes Symposium on VLSI
New Orleans, LA, USA
Deadline: Feb. 21, 2025
June 30 - July 2, 2025
http://www.glsvlsi.org

ISLPED'25 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
University of Iceland, Iceland
Deadline: Mar. 10, 2025 (Abstracts due: Mar. 3, 2025)
Aug. 6-8, 2025
http://www.islped.org

ESWEEK'25 - Embedded Systems Week
Taipei, Taiwan
Deadline: Mar. 30, 2025 (Abstracts due: Mar. 23, 2025)
Sept. 28 - Oct. 3, 2025
http://www.esweek.org

IWLS'25 - International Workshop on Logic & Synthesis
Verona, Italy
Deadline: Mar. 28, 2025 (Abstracts due: Mar. 28, 2025)
June 12-13, 2025
https://www.iwls.org

MLCAD'25 - ACM/IEEE Workshop on Machine Learning for CAD
Santa Cruz, CA, USA
Deadline: May 23, 2025 (Abstracts due: May 16, 2025)
Sep. 8-10, 2024
https://mlcad-workshop.org

The complete details of the call for nominations can be found in this link: https://tinyurl.com/todaesbp. Nominations can be submitted using the following link: https://forms.gle/XEwb6vyrQuph5xtz5.

For any questions, email Ann Franchesca Laguna, Managing Editor of ACM TODAES, at ann.laguna@dlsu.edu.ph.

CALL FOR ROOKIE OF THE YEAR AWARD NOMINATIONS

Deadline: February 8, 2025

ACM Transactions on Design Automation of Electronic Systems (TODAES) introduced a new award in 2022, i.e., the TODAES Rookie Author of the Year (RAY) Award. This newly introduced award aims to highlight the achievement of junior researchers in the Design and Design Automation of Electronic Systems field. Specifically, the award recognizes an author whose first-ever peer-reviewed journal paper as a lead author is published in ACM TODAES.

The lead author of a paper refers to the author who contributed the most to the submission. Since people may adopt different ways to order the authors, any nomination for the RAY Award must make it clear that the nominee is the lead author. If two authors satisfy this requirement (meaning they made equal contributions and are both rookie authors), both can receive the RAY award.

The complete details of the call for nominations can be found in this link: https://tinyurl.com/todaesray. Submit the nominations using this link: https://forms.gle/8NWbmTTNCW97DeKf6 by February 8, 2025.

If you have questions, e-mail Ann Franchesca Laguna at ann.laguna@dlsu.edu.ph, Managing Editor of ACM TODAES. No self-nomination is allowed.

CALL FOR SPECIAL ISSUE PAPERS FOR MLCAD

Deadline: February 15, 2025

Advances in machine learning (ML) over the past half-dozen years have revolutionized the effectiveness of ML for a variety of applications. However, design processes present challenges that require parallel advances in ML and CAD as compared to traditional ML applications such as image classification.

This special issue seeks original submissions on ML applications to the entire design flow – including ML applications to validation and testing. The application of machine learning to mask preparation and layout generation are topics which are seeing very active research recently. ML is also being applied to improve the robustness of integrated circuits and systems. Power and thermal management are probably the most important limiting factors for ICs today - ML-based techniques are being explored to address this bottleneck. All these topics, as well as further potential topics mentioned below, are of interest to this special issue.

Submit to : http://mc.manuscriptcentral.com/todaes

Upcoming Conferences

ISSCC'25 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA, USA
Feb. 16-20, 2025
http://isscc.org

FPGA'25 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Monterey, CA, USA
Feb. 27- Mar 1, 2025
http://www.isfpga.org

ISPD'25 – ACM Int'l Symposium on Physical Design
Austin, Texas, USA
Mar. 16-19, 2025
http://www.ispd.cc

DATE'25 - Design Automation and Test in Europe
Lyon, France
Mar. 31 - April. 2, 2025
http://www.date-conference.com

ISQED'25 - Int'l Symposium on Quality Electronic Design
San Francisco, CA, USA
Apr. 9-11, 2025
http://www.isqed.org

FCCM' 25 - IEEE International Symposium On Field-Programmable Custom Computing Machines
Fayetteville, AR, USA
May 4-7, 2025
https://www.fccm.org/

HOST'25 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
San Jose, CA, USA
May 5-8, 2025
http://www.hostsymposium.org

Technical Activities

1. AMD Launches Versal RF SoCs with Direct RF Sampling
First AMD Versal adaptive SoCs integrating high-resolution RF data converters, dedicated DSP hard IP, AI Engines, and programmable logic in a single-chip device…

2. Microchip's PolarFire FPGA and SoC for Robotics and Imaging
The development of IoT, industrial automation, smart robotics, and the proliferation of medical imaging solutions to the intelligent edge has made developing these types of power and thermally limited applications more difficult than ever. To address the crucial problems of shortening product development cycles and simplifying complex development processes, Microchip Technology has introduced PolarFire® FPGA and SoC solution stacks for smart robotics and medical imaging. These new releases extend Microchip's smart embedded vision, industrial edge, and intelligent edge communications stacks, which are already available…

3.Alps Supercomputer Powers AI and Climate Modeling Advancements
CSCS director Thomas Schulthess explained how the design of Alps, the world's seventh largest computer, anticipated the needs of the current generation of AI as early as 2020…

4. CES 2025 Takeaways: Edge AI and AI PCs
From novel HMIs and edge AI to AI PCs and the next phase of AI value creation, TIRIAS Research's Jim McGregor, Francis Sideco and Caiden McGregor recap key takeaways from CES 2025…

Job Positions

ETH Zurich, Switzerland

Job Title: Professor/Assistant Professor (Tenure Track) of Computer Vision

Description: The new professor is expected to focus on fundamental research in computer vision. Potential focus areas include but are not limited to embodied visual intelligence, advanced machine learning algorithms for computer vision, human perception inspired vision models, and novel hardware-software interfaces for visual perception. Moreover, the research can extend into various applications, encompassing biomedical, autonomous driving, robotics, and advanced sensors. The ideal candidate also establishes synergies with other research areas in the Department of Information Technology and Electrical Engineering and more broadly at ETH Zürich. The successful candidate must be committed to innovative and engaging teaching in both fundamental undergraduate-level courses and advanced graduate-level courses in the areas of computer vision and machine learning. At ETH Zürich, undergraduate-level courses are taught in German or English, and graduate-level courses are taught in English. The ability to lead a research group is expected. For more information, please refer to

RTAS'25 - IEEE Real-Time and Embedded Technology and Applications Symposium
Irvine, CA, USA
May 6-9, 2025
http://2025.rtas.org

MDTS'25 – IEEE Microelectronics Design & Test Symposium
Albany, NY, USA
May 19-21, 2025
http://natw.ieee.org

ISCAS'25 – IEEE Int'l Symposium on Circuits and Systems
London, United Kingdom
May 25-28, 2025
https://2025.ieee-iscas.org/

DAC'25 – Design Automation Conference
San Francisco, CA, USA
June 22-25, 2025
http://www.dac.com/

https://computeroxy.com/professorassistant-professor-tenure-track-of-computer-vision,i15522.html.

University of Nottingham Ningbo, China

Job Title: Assistant Professor of Electrical Engineering

Description: The University of Nottingham Ningbo, China, a pioneer in Sino-foreign tertiary education, is rapidly expanding. It is looking for ambitious, talented academics with a passion for teaching as well as research flair to join its team of science and engineering experts. UNNC is part of the University of Nottingham's Global University, and offers unique teaching and research opportunities in a highly dynamic economy. The successful candidate will be expected to lead and deliver individual and collaborative research and teaching in the area of Electrical and Electronic Engineering in the Department of Electrical and Electronic Engineering. The role holder will be responsible for publishing high-quality research in peer-reviewed journals, presenting findings at national and international conferences, and engaging with internal and external stakeholders to build collaborations that advance the department's research and teaching objectives. For more information, please refer to https://facultyvacancies.com/assistant-professor-of-electrical-engineering,i41037.html.

University of Antwerp, Belgium

Job Title: PhD Position in Electromechanical Engineering

Description: The research group InViLab of the Department of Electromechanical Engineering in the Faculty of Applied Engineering is looking to fill a full-time (100%) PhD position on Optical Coherence Tomography to assess the structural and mechanical properties of the eardrum and inner ear under the supervision of Professor Sam Van der Jeught (InViLab, University of Antwerp) and Professor Joris Dirckx (BIMEF, University of Antwerp). You will actively contribute to the preparation and defence of a PhD thesis in the field of Optical Coherence Tomography (OCT). This project aims to develop a cutting-edge diagnostic tool by leveraging advanced Optical Coherence Tomography (OCT) to assess the structural and mechanical properties of the eardrum and inner ear. The results will support improved cochlear implant procedures and enhanced diagnostic capabilities in otology. Your research will include both theoretical and experimental components. Your research will focus on designing, developing, and optimising an OCT tool tailored for high-resolution middle and inner ear imaging. This includes hardware design, system integration, and validation of the imaging setup in relevant experimental conditions. You will benefit from the unique collaboration between the University of Antwerp and the University of Kent (UK), gaining access to complementary expertise and training opportunities in OCT system development. You will publish scientific articles related to the research project. You will carry out a limited number of teaching and research support tasks for the research group InViLab. For more information, please refer to https://facultyvacancies.com/phd-position-in-electromechanical-engineering,i41061.html.

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