Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 55, No. 1

SIGDA - The Resource for EDA Professionals

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
Circulation: 2,700

Online archive: https://www.sigda.org/publications/newsletter

SIGDA News

1. ARM loses out in Qualcomm court case, wants a re-trial
A jury in Wilmington, Delaware, has found that Qualcomm's latest AI-PC processors – based on the ARM instruction set – are properly licensed. The court thereby rejected ARM's call that the intellectual property should be destroyed or that Qualcomm should be prepared to renegotiate the terms of its license with the implication of a higher royalty rate on the processors in question.

2. Europe okays Italy's €1.3 billion subsidy for chiplet fab
The European Commission has approved a €1.3 billion subsidy from the Italian government to Silicon Box for its advanced packaging and testing facility in Novara, in the Piedmont region.

3. American chip market soars as Asian growth slows
There was a glimmer of an upturn for Europe buried in recently published chip market sales data for October that showed the Americas region up by more than 50 percent year-on-year.

4. US cuts funding for Amkor packaging plant, Samsung fab
The US government has confirmed nearly $5bn for Samsung fabs in Texas and $407m for Amkor in Arizona for packaging, both cut by 20% since the original announcements.

5. Samsung, SK Hynix partner on processing-in-memory
Memory chip manufacturers Samsung and SK Hynix are collaborating to standardize processing-in-memory (PIM) in the form of LP-DDR6 memory, according to …

6. Rigetti launches 84-qubit Ankaa-3 quantum computer
Rigetti Computing in the US has launched its third-generation Ankaa-3 quantum computer with an 84-qubit processor and aims to have a 100-qubit machine next year. The re-designed quantum computer achieves a two-qubit gate fidelity of 99%, halving the previous error rate.

Message from the EiC

Dear Readers,

On behalf of the SIGDA editorial board, I wish you all a very happy new year.

In this edition, we bring you the latest news and activities in our community, upcoming conferences, paper deadlines, an insightful article on Hyperdimensional Computing, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

7. Nvidia boosts Jetson range with Orin Nano Super
Nvidia has launched a Jetson Orin Nano developer kit with a focus on generative AI for robotics or computer vision. The Jetson Orin Nano Super Developer Kit fits in the palm of a hand and costs $249. The developer kit consists of a Jetson Orin Nano 8GB system-on-module (SoM), launched back in 2022, and a reference carrier board for prototyping edge Al applications.

8. Honda, Nissan detail merger plan, add Mitsubishi
Honda and Nissan have signed a memorandum of understanding (MOU) to start discussions on a joint holding company. A separate MoU explores a further merger with Mitsubishi.

What is

Contributing author: Dayane Reis <dayane3@usf.edu>
AE: Muhammad Shafique <muhammad.shafique@nyu.edu>

What is Hyperdimensional Computing?

Dayane Reis,
Assistant Professor,
Department of Computer Science and Engineering, University of South Florida

Hyperdimensional computing (HDC) is an emerging computational paradigm inspired by how the human brain processes information [1]. It operates in high-dimensional spaces, typically using Hypervectors (HVs) with dimensions reaching up to 10,000 elements. Unlike traditional machine learning models, which often demand substantial resources for training and inference, HDC models offer several advantages: they are smaller, resilient to noise, and capable of one- or few-shot learning, making them particularly suitable for low-cost platforms and environments with constrained energy and memory resources [2].

In HDC, data is encoded into high-dimensional binary, bipolar, or integer HVs. These HVs are manipulated using a limited set of operations—binding, bundling, and permutation—to perform tasks such as classification and outlier detection. The high dimensionality of HDC allows it to tolerate noise and errors, improving its robustness in scenarios susceptible to hardware faults. However, HDC faces computational challenges when implemented on traditional hardware. Encoding data into HVs involves substantial data movement between memory and processing units, leading to bottlenecks in terms of latency and energy consumption. These limitations are particularly problematic for real-time and energy-sensitive applications. Balancing precision and efficiency is also a common challenge in HDC.

Both software and hardware solutions have been explored to address these challenges. For instance, [3] introduced a hybrid HDC system using unary bit-streams for lightweight computations, while [4] proposed re-training algorithms to enhance HDC classification accuracy. On the hardware front, processing-in-memory (PIM) technology, which integrates computational capabilities within memory to reduce latency and energy consumption for data-intensive tasks, has been employed in the design of HDC accelerators (e.g., [5-10]). PIM has been implemented using both complementary metal-oxide

SIGDA E-News Editorial Board

semiconductor (CMOS) technology and emerging technologies such as resistive random-access memory (ReRAM) and ferroelectric field-effect transistors (FeFET). While SRAM-based PIM accelerators are a promising alternative for accelerating HDC, as shown in [5,6], challenges such as array size and density could become limiting factors when handling larger datasets. Nevertheless, CMOS remains a reliable and widely used technology, offering proven performance and scalability.

ReRAM-based HDC accelerators (e.g., [7,8]) present an alternative. For example, [8] proposed a ReRAM-based PIM accelerator for HDC, which performs energy-saving computations on high-dimensional hypervectors by exploiting ReRAM's capability for analog computation within crossbar arrays. Similarly, FeFET-based architectures, e.g., [9,10], provide low-power solutions for in-memory HDC computing by minimizing write energy and exploiting FeFET's non-volatile properties. These non-volatile memory (NVM) technologies offer potential energy efficiency improvements over traditional designs, including CMOS-based PIM implementations. However, NVM technologies are still evolving, each with its advantages and trade-offs.

References:

1. Kanerva, P. "Hyperdimensional Computing: An Introduction to Computing in Distributed Representation with High-Dimensional Random Vectors." Cognitive Computation, 2010.
2. Imec Research Report. "In-memory Computing for Edge AI Applications." 2020.
3. Aygun, S., et al. "uHD: Unary Processing for Lightweight and Dynamic Hyperdimensional Computing," in 2024 Design, Automation & Test in Europe Conference & Exhibition (DATE), IEEE, 2024.
4. Hernández-Cano, A., et al. "Onlinehd: Robust, Efficient, and Single-pass Online Learning Using Hyperdimensional System," in 2021 Design, Automation & Test in Europe Conference & Exhibition (DATE), IEEE, 2021.
5. Wang, R., et al. "A Computing-in-Memory-based One-Class Hyperdimensional Computing Model for Outlier Detection," IEEE Transactions on Computers, 2024.
6. Kim, Y., et al. "A 6T SRAM-Based In-Memory Hyperdimensional Computing System for Pattern Recognition." IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019.
7. Liu, J., et al. "Hdc-im: Hyperdimensional Computing In-Memory Architecture Based on RRAM," in 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), IEEE, 2019.
8. Liu, C., et al. "A ReRAM-Based Processing-In-Memory Architecture for Hyperdimensional Computing," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2024.
9. Gupta, S., et al. "FeFET-Based In-Memory Computing for Hyperdimensional Computing." IEEE Transactions on Circuits and Systems I: Regular Papers, 2021.
10. Kazemi, A., et al. "Achieving Software-Equivalent Accuracy for Hyperdimensional Computing with Ferroelectric-Based In-Memory Computing." Scientific Reports, 12, 19201 (2022). https://doi.org/10.1038/s41598-022-23116-w.

Paper Deadlines

DAC'25 – Design Automation Conference
San Francisco, CA, USA
Engineering Tracks Deadline: Jan. 16, 2025
June 22-25, 2025
http://www.dac.com/

FCCM' 25 - IEEE International Symposium On Field-Programmable Custom Computing Machines
Fayetteville, AR, USA
Deadline: Jan. 17, 2025 (Abstracts due: Jan. 10, 2025)
May 4-7, 2025
https://www.fccm.org/

GLSVLSI'25 – ACM Great Lakes Symposium on VLSI
New Orleans, LA, USA
Deadline: Feb. 21, 2025
June-July, 2025
http://www.glsvlsi.org

ISVLSI'25 – IEEE Computer Society Annual Symposium on VLSI
Kalamata, Greece
Deadline: Feb. 10, 2025
July 6-9, 2025
http://www.ieee-isvlsi.org

ISLPED'25 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
University of Iceland, Iceland
Deadline: Mar. 10, 2025 (Abstracts due: Mar. 3, 2025)
Aug. 6-8, 2025
http://www.islped.org

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems (TODAES) features groundbreaking research and development in the specification, design, analysis, simulation, testing, and evaluation of electronic systems, with a focus on computer science and engineering. The journal's impact factor rose to 2.2 in 2023, more than doubling its 2020 value. Additionally, each issue highlights a notable contribution as the Editor's Pick for special recognition.

TODAES also recognizes papers and outstanding junior researchers through best paper and rookie of the year award. Authors can send their paper submissions on the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

Technical Activities

1. Marvell Adds Custom HBM to Optimize AI Data Centers
A big part of Marvell's message during the analyst day presentations was the need for custom compute, storage and connectivity for AI data centers. In this respect, the company announced a new custom high-bandwidth memory (HBM) compute architecture in conjunction with Micron, Samsung Electronics and SK Hynix to achieve greater compute and memory density…

2. Optimizing Parcel Delivery with Quantum Computing
Logistics service provider Hermes Germany has begun experimenting with quantum computing, in hopes of one day solving problems that can't be solved with classical hardware…

3. Fab Maintenance Gets a Robotic Helping Hand
Advanced wafer fabs around the world now have robotic help with optimizing critical maintenance tasks on wafer fabrication equipment…

4. IBM Boasts Industry-Leading Photonics to Cut AI Training Time
IBM said this week that the company leads the semiconductor industry with the development of a silicon photonics technology that could speed data center training by as much as 5x…

Job Positions

Royal Institute of Technology, Sweden

Job Title: Postdoctoral Position in Electrical Engineering

Upcoming Conferences

VLSID'25 – International Conference on VLSI Design & International Conference on Embedded Systems
Bengaluru, India
Jan. 4 - 8, 2025
https://vlsid.org/

HiPEAC'25: Int'l Conference on High Performance Embedded Architectures & Compilers
Barcelona, Spain
Jan. 20-22, 2025
https://www.hipeac.net/2025/barcelona

ASP-DAC'25 - Asia and South Pacific Design Automation Conference
Tokyo Odaiba Miraikan, Japan
Jan. 20-23, 2025
http://www.aspdac.com

FPGA'25 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Monterey, CA, USA
Feb. 27- Mar 1, 2025
http://www.isfpga.org

ISSCC'25 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA, USA
Feb. 16-20, 2025
http://isscc.org

ISPD'25 – ACM Int'l Symposium on Physical Design
Austin, Texas, USA
Mar. 16-19, 2025
http://www.ispd.cc

DATE'25 - Design Automation and Test in Europe
Lyon, France
Mar. 31 - April. 2, 2025
http://www.date-conference.com

ISQED'25 - Int'l Symposium on Quality Electronic Design

Description: In collaboration with Chalmers and Göteborgs university, we develop graphene based miniature sensors, to be placed on the surface of implanted devices, in order to follow the bio-integration process and provide early detection of inflammation, infection or other issues. Your task in the project will be two-fold; to develop and implement principles for wireless reading of sensor data, and to develop and analyse algorithms for analysing the measurements and see how they best can predict the medical conditions. The project is cross-disciplinary and provides good opportunities both to obtain a wide competence in the area of medical sensor technology, and to dive into the theory and practice of inductive communication and medical data analysis. For more information, please refer to https://facultyvacancies.com/postdoctoral-position-in-electrical-engineering,i40743.html.

Last application date: 09-Jan, 2025.

Utrecht University, Netherlands

Job Title: PhD Position in Computer Sciences

Description: Artificial intelligence (AI) is increasingly embedded in educational technologies to support and enhance learning and teaching. Examples include adaptive learning trajectories, automating feedback, and detecting students with additional needs. Despite these promising evolutions, educational stakeholders' interactions with these technologies are currently suboptimal due to a lack of transparency and control with regards to underlying AI models. To give insights into AI outcomes and model behaviour, many explainable AI techniques have been developed. These can be communicated in the form of visualisations, for example, in visual analytics dashboards. However, different contexts and target groups require different explanation methods and modalities. This motivates why human-centred approaches are necessary to make explanations effective. Similarly, there exist different AI control approaches where either people or the AI system takes the initiative or there is a mixed initiative. It is yet unclear which paradigms should be adopted when and for whom and how they can be operationalised in education. In this PhD project, you will contribute to tackling the transparency and control challenges above. Specifically, you will co-design explanation and control interfaces with educational stakeholders in human-centred design processes and evaluate these interfaces in lab or real classroom settings using a broad range of measurements (e.g., model understanding, trust, learning, motivation, reliance). As this is an inherently multidisciplinary project, you will combine technical skills (e.g., data science, algorithm-centred explainable AI, training AI models), design skills (e.g., visualisation, front-end development), human-centred skills (e.g., conducting user studies, human-centred explainable AI), and education-specific skills (e.g., assessment design, applying educational frameworks). For more information, refer to https://facultyvacancies.com/phd-position-in-computer-sciences,i40777.html.

Ryerson University, Canada

Job Title: Postdoctoral Fellow in Computer Science

Description: We are currently accepting applications for tenure stream positions at the rank of Assistant/Associate Professor in the following areas of computer science: Computer Graphics; Visual Computing, AR/VR; HCI (Human-Computer Interaction) and User Experience (UX); Game Design. Successful candidates will

San Francisco, CA, USA
Apr. 9-11, 2025
http://www.isqed.org

RTAS'25 - IEEE Real-Time and Embedded Technology and Applications Symposium
Irvine, CA, USA
May 6-9, 2025
http://2025.rtas.org

HOST'25 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
San Jose, CA, USA
May 5-8, 2025
http://www.hostsymposium.org

MDTS'25 – IEEE Microelectronics Design & Test Symposium
Albany, NY, USA
May 19-21, 2025
http://natw.ieee.org

ISCAS'25 – IEEE Int'l Symposium on Circuits and Systems
London, United Kingdom
May 25-28, 2025
https://2025.ieee-iscas.org/

engage in a combination of teaching, research and service duties, maintaining an inclusive, equitable, and collegial work environment across all activities. Responsibilities will include: pursuing an innovative and independent research program that is externally funded and generates cutting-edge, high quality research; contributing to our undergraduate and graduate programs through teaching, mentoring and supervision of students; contributing to the development of curricula and course design in our graduate and undergraduate programs; and engaging in the life of the Department, Faculty and University through service activities. For more information, please refer to https://facultyvacancies.com/postdoctoral-fellow-in-computer-science,i40724.html.

Notice to authors