Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 54, No. 9

SIGDA - The Resource for EDA Professionals

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
Circulation: 2,700

Online archive: https://www.sigda.org/publications/newsletter

SIGDA News

1. ESIA Calls for More Funds and Support from European Chips Act 2.0
The European Semiconductor Industry Association (ESIA) has asked the European Union to create a Chips Act 2.0, speed up the distribution of subsidies, and create a "Chip Envoy" to champion the sector.

2. OpenAI Joins Apple as A Lead Customer for TSMC's A16 Process
According to Taiwan's Economic Daily News, OpenAI, the developer of the generative AI chatbot ChatGPT, has joined Apple as a lead customer for TSMC's nominal 1.6nm manufacturing process.

3. Intel Core Ultra Processors Target the AI PC Age
Intel has launched its most efficient family of x86 processors, the Intel® Core™ Ultra 200V series processors. They deliver exceptional performance, breakthrough x86 power efficiency, a massive graphics-performance leap, no-compromise application compatibility, enhanced security, and unmatched AI computing.

4. Broadband Platform for Seamless Deployment of Wi-Fi 7
Calix has unveiled its first Wi-Fi 7 systems. As with all Calix GigaSpire® and GigaPro® systems, the new Wi-Fi 7 systems are seamlessly integrated with the Calix Broadband Platform, making them simple and easy to deploy.

5. SiFive, PQShield Encryption Deal for RISC-V Designs
Secure encryption technologies from PQSHield in the UK will be integrated with SiFive's Essential Core range of RISC-V for post-quantum cryptography, including the use of RISC-V vector extensions.

6. 16Gbit DDR5 DRAM Made with 1c-nm Process
SK Hynix has announced it has developed the world's first 16Gbit DDR5 DRAM using its 1c node, the sixth generation of manufacturing processes between 20nm and 10nm.

Message from the EiC

Dear Readers,

In the September edition, we bring you the latest news and activities in our community, upcoming conferences, paper deadlines, an insightful article on Multi-Level Intermediate Representation, and job openings worldwide.

Please do not hesitate to write to us if you want to contribute articles and announcements or share your thoughts and feedback.

Sandeep Chandran,
Editor-in-Chief,
SIGDA e-Newsletter

7. Researchers Develop Ultra-High Efficiency Perovskite LEDs
The College of Engineering at Seoul National University has announced that a research team led by Professor Tae-Woo Lee from the Department of Materials Science and Engineering at Seoul National University, in collaboration with Professor Andrew M. Rappe of the University of Pennsylvania, has developed an ultra-high efficiency perovskite nanocrystal light-emitting diodes (LEDs).

8. Sweden Opens World's First Zinc-Ion Battery Megafactory
Enerpoly in Stockholm has opened the world's first mega factory for zinc ion battery cells and packs. The facility will house all of the Enerpoly operations and is expected to operate at full capacity of 100MWh by 2026 with a fully European supply chain for zinc ion battery cells and packs.

9. Intel Considers Foundry Split, Fab Cancellations
Intel is considering its strategic options around its manufacturing unit known as Intel Foundry, according to a Bloomberg report that cited unnamed sources.

SIGDA Awards

1. Award Winners @ ISLPED 2024
http://www.islped.org/2024/

Track 1: Technology, Circuits, and Architecture

LOCo: LPDDR Optimization with Compression and IECC scheme for DNN Inference

Jae-Youn Hong*, Sungkyu Kim†, Je-woo Jang*, Joon-Sung Yang*
** Yonsei University, South Korea | †Samsung Electronics, South Korea*

Track 2: EDA, Systems, and Software

Sparrow ECC: A Lightweight ECC Approach for HBM Refresh Reduction towards Energy-efficient DNN Inference

Hoseok Kim*, Seung Hun Choi*, Young-Ho Gong†, Joonho Kong‡, Sung Woo Chung*
**Korea University, South Korea | †Soongsil University, South Korea | ‡Kyungpook National University, South Korea*

Track 3: Crosscutting Themes (AI/ML Hardware & Hardware Security)

An Energy-Efficient 3D Point Neural Network Accelerator with Fine-grained LiDAR-SoC Pipeline Structure

SIGDA E-News Editorial Board

Bokyoung Seo*, Jueun Jung*, Donghyeon Han†, Kyuho Jason Lee*
*Ulsan National Institute of Science & Technology, South Korea |
†Massachusetts Institute of Technology, USA

Design Contest Award

A Sub-1μJ/class SoC for Headset-Integrated Mind Imagery and Control in VR/MR Applications

Zhiwei Zhong, Yijie Wei, Lance Go, and Jie Gu
Northwestern University, USA

What is

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What is Multi-Level Intermediate Representation?

Aviral Shrivastava,
Professor, School of Computing and AI, Arizona State University (ASU)

Multi-level Intermediate Representation or MLIR is an highly extensible compiler development framework that allows compiler developers to define intermediate representations at arbitrary levels of abstraction, and then define optimizations at that level, and define methods to lower the IR into lower levels of abstraction – essentially generating a compilation path from specification at a high level of abstraction to application binary that will execute on a given hardware platform.

Traditional compilers, like GCC (GNU C Compiler) and LLVM (Low-Level Virtual Machine) first convert the input program from your favorite programming language (C, C++, etc...) into an Intermediate Representation (lovingly called IR in the compiler community), then optimizations are performed on this IR, and then the instructions in this IR are converted into the target processor instructions.

The problem with traditional compilers is that this IR is at a very low level. The instructions in the IR are similar to the instructions of a typical processor… like add, subtract, XOR. The “low-level” in LLVM is an acknowledgement to the fact that the instructions (of the so-called virtual machine) are at a low level of abstraction. The implication of this “low-level” IR is that once the program is converted into low-level instructions, it is very hard to discover opportunities for optimizations – which would have been super-easy if the IR was at a higher level of abstraction.

Let me explain this by an example. Consider the LLVM IR of a function that adds an integer constant to each element of its input array. Figure 1 shows this loop. Let’s name this function **add_to_array**. The function takes 2 parameters, **c** the integer to add, and **a** — the array.

Paper Deadlines

DATE'25 - Design Automation and Test in Europe
Lyon, France
Deadline: Sept. 22, 2024 (Abstracts due: Sept 15, 2024)
Mar. 31 - April. 2, 2025
http://www.date-conference.com

ISQED'25 - Int'l Symposium on Quality Electronic Design
San Francisco, CA
Deadline: Sept. 27, 2024
Apr. 9-11, 2025
http://www.isqed.org

ISPD’25 – ACM Int’l Symposium on Physical Design
Austin, Texas
Deadline: Sept. 29, 2024 (Abstracts due: Sept. 22, 2024)
Mar. 16-19, 2025
http://www.ispd.cc

FPGA'25 – ACM/SIGDA Int’l Symposium on Field-Programmable Gate Arrays
Monterey, CA
Deadline: Oct. 8, 2024 (Abstracts due: Oct. 1, 2024)
Feb 27 – Mar 1, 2025
http://www.isfpga.org

ISCAS'24 – IEEE Int'l Symposium on Circuits and Systems
London, UK
Deadline: Oct. 14, 2024
May 25-28, 2025
https://2025.ieee-iscas.org/

```
define void @add_to_array(i32* %array, i32 %size, i32 %constant) {
entry:
  %i = alloca i32
  store i32 0, i32* %i
  br label %loop
loop:
  %index = load i32, i32* %i
  %cmp = icmp slt i32 %index, %size
  br i1 %cmp, label %body, label %exit

body:
  %array_elem = getelementptr inbounds i32, i32* %array, i32 %index
  %old_value = load i32, i32* %array_elem
  %new_value = add i32 %old_value, %constant
  store i32 %new_value, i32* %array_elem
  %next_index = add i32 %index, 1
  store i32 %next_index, i32* %i
  br label %loop

exit: ret void }
}
```

Figure 1: llvm IR for a function that adds a constant to every element of an array. At this level, it is very hard for the compiler to detect that a sequence of instructions is adding a constant to every element of an array. Even if the compiler can do that, it must discover two of these and figure out that they are operating on the same array. Only then it can replace two sequences of instructions by one of them.

MLIR makes this simple! MLIR allows compiler developers to create an IR at the level of abstraction of this function. Compiler developer can write this optimization that if there are 2 calls to this function on the same array, then they can be replaced by a single call. MLIR optimization is simpler to apply since the optimization is at a function name basis, and not on instruction sequences.

Now, it is obvious that if two instances of this function are called on the same array one after another, with constants, **c1** and **c2**, then they can be replaced by one call to the function on the array with constant **"c1+c2."**

However, once the application code has been brought down to LLVM IR, and the code looks like figure 1, then it becomes very hard to discover that that the two sets of these instructions (one adding **c1** to the array, and the other one adding **c2** to the array) are indeed similar, and that they can be replaced by another instance of these complicated instructions with a different constant **"c1+c2."** A lot of this has to do with the fact that by their nature, compilers are very conservative tools, and they do not perform a transformation, unless they can be sure that the functionality will remain the same for all inputs. In some specific instances, e.g., when the two loops are inside the same function and one after another, affine transformations can merge the two loops, (and this is a true testament to how powerful affine optimizations are!) — but — in general this is HARD.

MLIR solves this problem. MLIR allows compiler developers to define the IR at a higher level – the level of the function **add_to_array**. To do that, MLIR compiler developers will define an IR that contains operations like **add_to_array**, and similar functions, and the application is converted in terms of these functions. The compiler developer now can define an optimization to replace two **add_to_array** calls next to each other, operating on the same array by one call with a combined constant. Compilers can perform this transformation easily, since it is based on the names of two functions, rather than the compiler identifying that a sequence of low-level instructions are actually implementing the functionality of adding a constant to an array!

Jumping outside the realm of toy examples, let's consider a real example. We are developing a MLIR IR for expressing DSP applications. We have defined the FIRFilterResponse() filter, which essentially calculates $y[n] = \sum_{i=0}^{L} h[i] \cdot x[n-i]$, for an input signal $x[]$, and a filter $h[]$. Now in most cases, the filter $h[]$ is a symmetric function. In that case $y[n]$, is also symmetric, and you only need to compute half of $y[n]$, and copy the first half onto the second half of $y[n]$. This transformation is hard to perform on a low-level IR, but at the DSP IR level, this can be performed as a simple compiler pass inside the implementation of the FIRFilterResponse() by checking first if $h[]$ is symmetric. That is the power of MLIR!, and that is why it is such a phenomenon, and all companies, including Google, Apple, Facebook are all now starting to use the Multi-Level Intermediate Representation (MLIR) compiler development framework.

Upcoming Conferences

MLCAD'24 - ACM/IEEE Workshop on Machine Learning for CAD
Snowbird, Utah
Sep. 9-11, 2024
https://mlcad-workshop.org/

ESWEEK'24 - Embedded Systems Week
Raleigh, NC
Sept. 29 - Oct. 4, 2024
http://www.esweek.org

VLSI-SoC'24 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Tanger, Morocco
Oct. 6-9, 2024
http://www.vlsi-soc.com

PACT'24 - Int'l Conference on Parallel Architectures and Compilation Techniques
Long Beach, CA
Oct. 13-16, 2024
http://www.pactconf.org

ICCAD'24 – IEEE/ACM Int'l Conference on Computer-Aided Design
New Jersey
Oct 27-31, 2024
https://iccad.com/

ICCD'24 – IEEE Int'l Conference on Computer Design
Milan, Italy
Nov. , 2024
http://www.iccd-conf.com

MICRO'24 – IEEE/ACM Int'l Symposium on Microarchitecture
Austin, Texas
Nov. 2-6, 2024

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems, TODAES, publishes innovative work documenting significant research and development advances on the specification, design, analysis, simulation, testing, and evaluation of electronic systems, emphasizing a computer science/engineering orientation. Design automation for machine learning/AI and machine learning/AI for design automation are very much welcomed.

If you are an active researcher in the design and design automation field and would like to be part of the TODAES review board, please fill out the following reviewer form. TODAES recognizes those reviewers that provide timely and high-quality reviews through the Distinguished Review Board. TODAES also recognizes papers and outstanding junior researchers through best paper and rookie of the year award. Authors can send their paper submissions on the manuscript portal.

TODAES welcomes special issue proposals from leading researchers and practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

TODAES 2024 BEST PAPER WEBINAR

Join us for a webinar showcasing the TODAES 2024 Best Paper Award entitled ***"Hardware-aware Quantization/Mapping Strategies for Compute-in-Memory Accelerators***" by Sanshi Huang, Hongwu Jiang, and Shimeng Yu.

When: September 20, 2024 10AM-11AM EST
Where: Online (https://zoom.us/j/93942637733)

Technical Activities

1. Hot Chips 2024 Takeaways
TIRIAS Research principal analysts Jim McGregor and Kevin Krewell discuss critical takeaways from Hot Chips 2024. AI was everywhere, as we have come to expect from most industry events, but a key theme emerged of designing these AI chips with upfront balanced design considerations to optimize chip utilization, remove bottlenecks, and minimize downtime from the beginning as opposed to later in the tape out and testing process…

2. World's First Quantum Microelectronics Park Lands in Chicago
The University of Illinois and the state government have unveiled the world's first Quantum and Microelectronics Park. Located on Chicago's South Side, the park is attracting startups like PsiQuantum in a project led by the Defense Advanced

http://www.microarch.org/micro57

FPT'24 - Int'l Conference on Field-Programmable Technology
Sydney
Dec. 10-12, 2024
http://icfpt.org

iSES'24 – IEEE Int'l Symposium on Smart Electronic Systems
Ahmedabad, India
Dec. 16-18, 2024
http://www.ieee-ises.org

HiPC'24 – IEEE Int'l Conference on High Performance Computing, Data, And Analytics
Bengaluru, India
Dec. 18-21, 2024
http://www.hipc.org

ISED'24 – Int'l Conference on Intelligent Systems and Embedded Design
NIT Rourkela, Odisha
Dec. 20-22, 2024
http://isedconf.org

VLSID'25 – International Conference on VLSI Design & International Conference on Embedded Systems
Bengaluru, India
Jan. 4 - 8, 2025
https://vlsid.org/

ASP-DAC'25 - Asia and South Pacific Design Automation Conference
Tokyo Odaiba Miraikan, Japan
Jan. 20-23, 2025
http://www.aspdac.com

Research Projects Agency (DARPA) to commercialize quantum computing and build a U.S. national-security advantage, project leaders told EE Times…

3. Nvidia Powering Supercomputers for Quantum Computing Research
Nvidia has become synonymous with the current AI boom by supporting it with various chips and network platforms. However, the company is also focusing efforts on accelerating quantum computing, which Nvidia sees as having a synergistic relationship with traditional high-performance computing (HPC)…

4. Reconfigurable Logic Circuit Opens Doors to New Computing Paradigms
Scientists from the Research Center for Materials Nanoarchitectonics (MANA) developed a reconfigurable logic circuit that switches functions with constant input voltages. This innovation opens doors to novel computing architectures…

Job Positions

University of California Santa Barbara, US

Job Title: Assistant Professor of Computer Engineering

Description: The Department of Electrical and Computer Engineering invites applications for an Associate Specialist position with Prof. Nina Miolane. Candidates will lead the development of the Python package 'Geomstats' co-developed by Dr. Miolane's Laboratory, and assist researchers as they apply methods from 'Geomstats' to their projects. Associate Specialists normally provide considerable independent input into the planning and execution of the research, have a record of academic accomplishments, and include contributions to published research in the field. Appointees to the Specialist series engage in specialized research, professional activity, and University and/or public service. Specialists use their professional expertise to make scientific and scholarly contributions to the research enterprise of the University and to achieve recognition in the professional and scientific community. Specialists may participate in University and/or public service depending upon funding source and duties of the position. The Department is especially interested in candidates who can contribute to the diversity and excellence of the academic community through research, teaching, and service as appropriate to the position. For more information, please refer to https://facultyvacancies.com/assistant-professor-of-computer-engineering,i39706.html.

University College Cork, Ireland

Job Title: Researcher in Electronic Engineering

Description: Applications are invited for the whole-time post in the School of Engineering and Architecture for a fixed term of 2 years, dedicated to the Discipline of Electrical & Electronic Engineering. The post-holder will support the delivery of School teaching and research activities in Engineering, including maintenance and

operability of teaching laboratories, planning, preparing, developing, delivering and assisting the running of undergraduate and postgraduate laboratory classes; support to research activities; supervision, training and routine maintenance of laboratory equipment in the School; implementation of and monitoring of safety procedures and risk assessments within the School; and operation of advanced equipment.
The Electrical and Electronic Engineering facilities of the School include a variety of teaching and research laboratories that serve a very research-intensive Discipline. Supporting and operationalising the recent development of bespoke teaching facilities in power electronics is a particular requirement for this post, as well as support to requirements for Portable Appliances Testing, implying that experience in the operation of systems used in the transmission and use of electrical power is essential for this post. For example: power electronic equipment, electrical power systems, 3-phase systems and/or electrical machines. For more information, please refer to https://facultyvacancies.com/researcher-in-electronic-engineering,i39663.html.

The NHR Graduate School, Germany

Job Title: PhD Fellowships for HPC, Numerical Simulations, and AI / ML projects

Description: The NHR Graduate School seeks qualified international and national applicants interested in pursuing a PhD project in HPC, numerical simulation, and AI/ML (for a complete overview of topics, please click here). Fellows will receive a three-year full-time fellowship and excellent supervision at one university of the NHR Alliance in Germany. For more information, please refer to https://facultyvacancies.com/9-phd-fellowships-for-hpc-numerical-simulations-and-aiml-projects,i39372.html.

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