Association for Computing Machinery

Special Interest Group Design Automation
The resource for EDA Professionals

**Special Interest Group on Design Automation**
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**SIGDA - The Resource for EDA Professionals**

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# Welcoming 2024 with Innovation and Collaboration - A New Year Message from SIGDA

Dear SIGDA Community,

As we bid adieu to 2023 and embrace the dawn of 2024, I find it essential to pause for a moment and reflect on our collective accomplishments while expressing my heartfelt gratitude to each one of you for your unwavering support throughout the past year.
In the realm of electronic design automation (EDA), SIGDA continues to play an active role in sponsoring and co-sponsoring a multitude of conferences. It brings me immense joy to witness a remarkable surge in conference participants, indicative of a robust recovery and growth within our community in the post-pandemic era. Many of these conferences have set record-breaking numbers for paper submissions. Additionally, we've witnessed strong representation from EDA and semiconductor companies in exhibitions and conference attendance.

# Messages from the EiCs

Dear ACM/SIGDA members,

We are excited to present to you January E-Newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter.

The newsletter covers a wide range of information from the upcoming conferences to technical news and activities of our community. Get involved and contact us if you want to contribute articles or announcements.

The newsletter is evolving. Please let us know what you think.

Happy reading!

*Debjit Sinha, Keni Qiu*,
Editors-in-Chief,
SIGDA E-News

In the spirit of growth, SIGDA has welcomed several new conferences into our fold. For instance, the ACM International Conference on Neuromorphic Systems (ICONS) 2023 was successfully held in Santa Fe, New Mexico, enhancing SIGDA's technical portfolio in the realm of neuromorphic computing.

Furthermore, SIGDA remains committed to actively sponsoring and co-sponsoring various educational activities, including student research demonstrations, competitions, research contests, Ph.D. forums, summer schools, workshops, webinars, and lectures. These activities have attracted thousands of attendees from around the globe, with invaluable support from our industrial partners, including Synopsys, our Global Educational Partner.

We also take pride in extending our congratulations to all the deserving recipients of SIGDA awards, recognizing their outstanding technical contributions and service. Our heartfelt gratitude goes out to the dedicated volunteers who tirelessly contribute to our global community; it is your unwavering support that makes SIGDA thrive.

One significant development that marked 2023 and is poised to have a substantial impact on the EDA community is the emergence of ChatGPT. As a powerful AI-powered language and multimodal model, ChatGPT has showcased remarkable potential in various facets of the EDA toolchain, potentially revolutionizing research and development in EDA.

Looking forward, 2024 marks the final year of the current SIGDA Executive Committee (EC) term. We will be conducting a new election this Spring to form the new EC, and I strongly encourage you to nominate both your colleagues and yourself for these pivotal roles. For more information, please reach out to our Nomination Chair, Prof. Sharon Hu (hu@nd.edu).

As we stand on the threshold of 2024, I am brimming with optimism about the opportunities, challenges, and untapped potential that lie ahead. Let us embrace this new year with renewed enthusiasm and an unwavering commitment to advancing the field of EDA.

Wishing you and your loved ones a joyful, prosperous, and healthy New Year!

Warmest regards,

Yiran Chen
Chair, ACM SIGDA (The ACM Special Interest Group on Design Automation)

# SIGDA EC

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AE for Awards

# SIGDA News

**1. Intel Breaks into Foundry Top Ten in 3Q23 Ranking**

Intel Foundry Services (IFS) achieved strong percentage quarterly revenue growth in 3Q23 and broke into a top ten ranking prepared by TrendForce.

**2. IBM, Meta Launch Alliance for Open, Safe, Responsible AI**

IBM and Meta, formerly Facebook, have launched the AI Alliance with over 50 founding members to create guidelines and opportunities for open, safe, and responsible artificial intelligence development.

**3. AMD Launches MI300, Claims AI Performance over Nvidia**

Advanced Micro Devices Inc. has launched the Instinct MI300 series data center AI accelerators together with the ROCm 6 software stack supporting large language models (LLMs).

**4. TSMC's Chairman Mark Liu Gives Notice of Retirement**

Leading foundry TSMC has announced that its chairman Mark Liu, has decided to retire from the company in June 2024.

**5. TSMC's November Sales Show Return to Downward Trend**

Leading foundry TSMC (Hsinchu, Taiwan) has reported November sales that declined on both a monthly and annual basis.

**6. Intel Shows Gaudi 3 alongside Core Ultra, Xeon Processors**

Intel CEO Pat Gelsinger showed off an early sample of the Gaudi 3 AI accelerator at an event in New York used to launch Intel Core Ultra and 5th generation Xeon processors.

**7. China's SpinQ Ships Quantum Computing Chip to Middle East**

Shenzhen SpinQ Technology Co. Ltd. has delivered samples of its superconducting quantum chip known as Shaowei to an unnamed research institute in the Middle East.

**8.Foxconn Selects Porotech for microLED Displays**

MicroLED technology developer Poro Technologies Ltd. (Cambridge, England) is working with Hon Hai Technology Group (Foxconn) on developing microLED displays for augmented reality (AR) and other applications.

***Xun Jiao***,
AE for What is

***Muhammad Shafique***,
AE for What is

***Rajsaktish Sankaranarayanan***,
AE for Researcher spotlight

***Xin Zhao***,
AE for Paper submission

***Ying Wang***,
AE for Technical activities

***Jiaqi Zhang***,
AE for Technical activities

# Paper Deadlines

**DAC'24 – Design Automation Conference**
San Francisco, CA
Engineering Tracks Deadline: Jan. 16, 2024
June 23-27, 2024
http://www.dac.com/

**FCCM' 24 - IEEE International Symposium On Field-Programmable Custom Computing Machines**
Orlando, FL
Deadline: Jan. 15, 2024 (Abstracts due: Jan. 9, 2024)
May 5-8, 2024
https://www.fccm.org/

**MDTS'24 – IEEE Microelectronics Design & Test Symposium**
Albany, NY
Deadline: Feb. 15, 2023
Tentative Date: May 13-15, 2024
http://natw.ieee.org

# What is ML for EDA?

**Contributing author: Dr. Nan Wu**, Assistant Professor, Electrical and Computer Engineering Department, George Washington University <nan.wu@email.gwu.edu>

**AE: Dr. Xun Jiao**, Villanova University <xjiao@villanova.edu>

With the ever-increasing applications comes the realization that efforts and complexity for developing hardware to keep pace with such compute demands are growing at an even faster rate. As the target cadence of Moore's law is already slipping, more burden is placed on the design methodology to achieve “equivalent scaling”. Given the superiority of machine learning (ML) in many domains, it emerges as a pivotal catalyst to more agile, flexible, and scalable electronic design automation (EDA). The general roles of ML applied for EDA can be summarized as (1) fast and accurate design evaluation, (2) efficient and scalable design optimization, and (3) high-quality and productive design verification [1].

Evaluating hardware design quality quickly and accurately is essential for rapid optimization iterations. However, traditional EDA tools usually provide either accurate yet time-consuming or fast yet inaccurate estimations. In contrast, ML holds the promise of delivering accurate and timely performance predictions from early design stages. When supplied with sufficient design data, ML-based techniques can construct surrogate models to approximate the intricate heuristics and rules employed in EDA tools, and thus predict design performance accurately and promptly [2][3].

From a single processing unit to warehouse-scale computing infrastructures, from application mapping to hardware development, optimization is a pillar stone to achieve various trade-offs among different design specifications, such as performance, energy/power efficiency, and resource utilization. Considering the expanding design spaces that pose challenges for human experts to thoroughly explore, reinforcement learning (RL) has showcased its efficacy in addressing constrained optimization problems, such as resource allocation. By carefully formulate optimization problems and reward functions, RL can easily surpass EDA tools and meta-heuristics [4-6].

Hardware design verification has been a bottleneck in chip development, whose scalability is not immune from design complexity, complicated system integration, etc. The execution of verification processes is often very time/memory-consuming, failing to fully harness the capabilities of modern computing resources. Recent efforts strive to imitate conventional verification problems using ML, thereby markedly enhancing efficiency and scalability as well as leveraging GPU acceleration [7].

**GLSVLSI’24 – ACM Great Lakes Symposium on VLSI**
Tampa Bay Area, FL
Deadline: Feb. 9, 2024
June, 2024
http://www.glsvlsi.org

**ISVLSI’24 – IEEE Computer Society Annual Symposium on VLSI**
Knoxville, TN
Deadline: Mar. 4, 2024
July 1-3, 2024
http://www.ieee-isvlsi.org

**ISLPED’24 – ACM/IEEE Int’l Symposium on Low Power Electronics and Design**
Newport Beach, CA
Deadline: Mar. 11, 2024 (Abstracts due: Mar. 4, 2024)
Aug. 5-7, 2024
http://www.islped.org

**IWLS'24 - International Workshop on Logic & Synthesis**
ETH Zurich, Zurich, Switzerland
Deadline: Apr. 5, 2024 (Abstracts due: Mar. 29, 2024)
June 6-7, 2024
https://www.iwls.org

**SAT’24 - 27th edition of the International Conference on Theory and Applications of Satisfiability Testing**
Pune, India
Deadline: March 15, 2024 AoE (Abstract due: March 8, 2024 AoE)
August 21-24, 2024
http://satisfiability.org/SAT24

In summary, ML is a powerful assistant for EDA, improving design evaluation, optimization, and verification, either independently or integrally. Standing on the current successes of ML for EDA, more future endeavors are anticipated to focus on areas such as data generation and collection, model interpretability and explainability, generalization capability to new hardware designs, and holistic solutions [1].

**References:**


[1] Wu, Nan, and Yuan Xie. "A survey of machine learning for computer architecture and systems." ACM Computing Surveys (CSUR) 55.3 (2022): 1-39.
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[6] Wu, Nan, Yuan Xie, and Cong Hao. "IronMan-Pro: Multiobjective Design Space Exploration in HLS via Reinforcement Learning and Graph Neural Network-Based Modeling." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 42, no. 3 (2022): 900-913.
[7] Wu, Nan, Yingjie Li, Cong Hao, Steve Dai, Cunxi Yu, and Yuan Xie. "Gamora: Graph Learning based Symbolic Reasoning for Large-Scale Boolean Networks." In Proceedings of the 60th ACM/IEEE Design Automation Conference, pp. 1-6. 2023.


# Who Is Who


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**Research interests:** EDA, Systems and Architectures for AI/DL

# Upcoming Conferences

**ASP-DAC'24 - Asia and South Pacific Design Automation Conference**
Incheon Songdo Convensia, South Korea
Jan. 22-25, 2024
http://www.aspdac.com

**VLSID'24 – International Conference on VLSI Design & International Conference on Embedded Systems**
ITC Royal Bengal, Kolkata, India
Jan. 6-10, 2024
https://vlsid.org/

**HiPEAC'24: Int'l Conference on High Performance Embedded Architectures & Compilers**
Munich, Germany
Jan. 17-19, 2024
https://www.hipeac.net/2024/munich/

**ISSCC'24 – IEEE Int'l Solid-State Circuits Conference**
San Francisco, CA
Feb. 18-22, 2024
http://isscc.org

**FPGA'24 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays**
Monterey, CA
Mar. 3 - 5, 2024
http://www.isfpga.org

**ISPD'24 – ACM Int'l Symposium on Physical Design**
Taipei, Taiwan
Mar. 12-15, 2024
http://www.ispd.cc

# SIGDA Partner Journal

**ACM Transactions on Design Automation of Electronic Systems, TODAES**, publishes innovative work documenting significant research and development advances on the specification, design, analysis, simulation, testing, and evaluation of electronic systems, emphasizing a computer science/engineering orientation. Design automation for machine learning/AI and machine learning/AI for design automation are very much welcomed.

If you are an active researcher in the design and design automation field and would like to be part of the TODAES review board, please fill out the following reviewer form. TODAES recognizes those reviewers that provide timely and high-quality reviews through the Distinguished Review Board. TODAES also recognizes papers and outstanding junior researchers through best paper and rookie of the year award. Authors can send their paper submissions on the manuscript portal.

TODAES welcomes special issue proposals from leading researchers/practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

**CALL FOR NOMINATIONS: BEST PAPER AWARD**

ACM Transactions on Design Automation of Electronic Systems (TODAES) is seeking nominations for the **2024 TODAES Best Paper Award**. The nomination **deadline is February 1, 2024**. All papers published in the ACM TODAES between January 2023 and December 2023 are eligible. The best paper will be selected based on originality, timeliness, potential impact and overall quality. Submit the nominations using this link: https://forms.gle/XEwb6vyrQuph5xtz5

**CALL FOR NOMINATIONS: ROOKIE OF THE YEAR AWARD**

ACM Transactions on Design Automation of Electronic Systems (TODAES) introduced a new award in 2023, i.e., **the TODAES Rookie Author of the Year (RAY) Award**. This newly introduced award aims to highlight the achievement of junior researchers in the Design and Design Automation of Electronic Systems field. Specifically, the award recognizes an author whose first-ever peer-reviewed journal paper as a lead author is published in ACM TODAES. The nomination **deadline is February 1, 2024**. Submit the nominations using this link: https://forms.gle/8NWbmTTNCW97DeKf6

**DATE'24 - Design Automation and Test in Europe**
Valencia, Spain
Mar. 25-27, 2024
http://www.date-conference.com

**ISQED'24 - Int'l Symposium on Quality Electronic Design**
San Francisco, CA
Apr. 3-5, 2023
http://www.isqed.org

**HOST'24 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust**
Washington DC
Deadline (winter submission): Dec. 18, 2023 ((Abstracts due: Dec. 11, 2023)
May , 2024
http://www.hostsymposium.org

**RTAS'24 - IEEE Real-Time and Embedded Technology and Applications Symposium**
Hong Kong, China
May 13-16, 2024
http://2024.rtas.org

**ISCAS'24 – IEEE Int'l Symposium on Circuits and Systems**
Singapore
May 19-22, 2024
http://iscas2024.org

The lead author of a paper refers to the author who contributed the most to the submission. Since people may adopt different ways to order the authors, any nomination for the RAY Award must make it clear that the nominee is the lead author. If two authors satisfy this requirement (meaning they made equal contributions and are both rookie authors), both can receive the RAY award.

# Technical Activities

1. **Could IBM's AI Chip Reinvent Deep Learning Inference?**

In August, a 30-strong team of IBM Research scientists revealed a radically new chip, designed to drastically raise the energy efficiency of power-hungry deep learning inference while maintaining operation precision. The analog in-memory chip, dubbed Hermes, merges digital circuits with phase-change memory (PCM) so neural network calculations can take place within the memory circuits…

2. **eMemory: Leading the NVM Technology Revolution**

One new-launched product from eMemory is NeoFlash, a scalable embedded non-volatile memory (NVM) solution that excels in size, cost-effectiveness, and seamless implementation across CMOS processes from 250nm to 22nm HKMG (High-k Metal Gate). With its simple process, robust design, and low cost, NeoFlash is an excellent embedded NVM solution for most system-on-chip applications…

3. **Next Up: Internet of Energy**

Watchers of energy developments will have heard of many proposed solutions, including the possibility of integrating cutting-edge technologies, such as machine-to-machine (M2M) communication and Internet of Things (IoT) devices to enable peer-to-peer (P2P) energy sharing in a distributed energy network. These technologies have the potential to revolutionize the way energy is produced, consumed, and shared—and they could pave the way for a functional "Internet of Energy" (IoE)…

4. **Makers Conquer Generative AI Bottlenecks**

Makers of generative AI hardware are focusing on bringing down the cost of using large language models (LLMs) along with optimizing efficiency and flexibility…

# Job Positions

**1. Harvard University, US**

**Job Title:** Tenure-track or Tenured Professor in Computer Science and Kempner Institute Investigator

**Description:** The Computer Science area of the John A. Paulson School of Engineering and Applied Sciences (SEAS) and the Kempner Institute for the Study of Natural and Artificial Intelligence at Harvard University are seeking applicants for a tenure-track or tenured position specializing in Machine Learning and Artificial Intelligence, with an expected start date of July 1, 2024. We are particularly interested in candidates with strong foundations in deep learning, generative AI, foundational models, and LLMs, with interest to apply these technologies to one or more domains including computational biology and the sciences, NLP, and computer vision. The successful candidate will be expected to lead an innovative research program that advances our understanding of and increases innovation in AI and ML, encompassing the development of new methodologies and models. Candidates will be welcomed into an interdisciplinary and highly collaborative environment where exploration into how principles of computation and learning in artificial systems can aid in understanding the brain and, reciprocally, how insights into brain computation can enhance artificial systems is encouraged. The successful candidate will hold a faculty position in SEAS and be appointed as an Institute Investigator within the Kempner Institute. Candidates are encouraged to apply by December 15, 2023; applications will be reviewed until the position is filled. For more information, please refer to https://facultyvacancies.com/professor-of-computer-science,i37223.html.

**2. Lund University, Sweden**

**Job Title:** PhD Positions in Electrical Engineering

**Description:** The security and networked systems division works broadly with research within cryptography, computer security, wireless, and fixed networks. The security group has around 15 members. The main research directions are cryptography and system security for connected systems. The division runs several research projects through different large research collaboration platforms and arranges extensive workshops and seminar series, making the research at the division visible to larger audiences. Cross-disciplinary projects are formed through our research collaboration platforms and national and international research networks, contributing to a dynamic research environment. Through the Swedish Research Council (https://www.vr.se/english.html) and the

Wallenberg AI, Autonomous Systems and Software Program (WASP) (https://wasp-sweden.org/sv/ai-autonoma-system-och-mjukvara/), we now offer four new PhD positions, two in the cryptographic area and two in the computer security area. Last application date: 14.Jan.2024 11:59 PM CET. For more information, please refer to https://facultyvacancies.com/phd-positions-in-electrical-engineering,i37401.html.

**3. ETH Zurich, Switzerland**

**Job Title:** PhD Positions in Electrical Engineering

**Description:** We are looking for outstanding, highly motivated people interested in pursuing PhD research on highly efficient drive systems for electric vehicles. For achieving high efficiency in a wide operating range, different 3-level inverter topologies and modulation schemes for drive systems should be modeled and optimized in this research project. Considering a wide operating range is important as the inverter is directly connected to the battery, which has a wide voltage range depending on the state of charge. Furthermore, the drive system is operated in many use cases only at a relatively low power level compared to nominal power, so that also partial load operation is also important to consider in the design phase. The efficiency increase should be achieved by using optimized 3-level inverter topologies, which also allow for reduction of the losses in the electrical machine due to lower ripple currents. Furthermore, new wide band gap depletion mode GaN HEMT devices in a direct-driven cascade configuration should be investigated, which allows reducing conduction as well as switching losses thus enabling a wider range of switching frequency at high-efficiency levels. A disadvantage of 3L inverters is the higher number of switches, which results in higher costs and which require more space. To still benefit from the 3L topology, a design trade-off between the inverter and the motor losses, which results in overall minimal losses, and an optimized PCB power module layout are necessary. The optimal design should be identified based on comprehensive models and an optimisation procedure considering the Worldwide Harmonised Light Vehicle Test Procedure (WLTP). In the optimization, different 3L topologies, modulation schemes, a wide switching frequency range, and different motor types as well as basic control strategies should be considered, for identifying the best topology and the optimal operating parameters for the different operating points. In the final step, you should validate the optimized design with a prototype system. For more information, please refer to https://facultyvacancies.com/phd-positions-in-electrical-engineering,i37168.html.

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