Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 53, No. 11

SIGDA - The Resource for EDA Professionals

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Call for SIGDA Newsletter Editor-in-Chief

ACM SIGDA announces the call for Editor-in-Chief for the SIGDA Newsletter, a monthly publication for news and event information in the design automation area. The Editor-in-Chief, along with the editorial board consisting of associate editors, is responsible for collecting and compiling information, as well as composing and disseminating the monthly newsletter to the SIGDA community. Please refer to the following URL for more information about the newsletter content: https://www.sigda.org/publications/newsletter/.

Responsibility: The Editor-in-Chief role requires the initial formation of the editorial board, and the assigning of roles to and close co-ordination with several Associate Editors in charge of the different newsletter sections, including headlines, "What is" column, recent events and awards, technical activities, upcoming submission deadlines, and job positions. The Editor-in-Chief will be appointed with effect from 1 January 2024 for an initial period of two years.

Qualifications: The candidate must be an active and respected member of the SIGDA community, as evidenced by participation in recent conferences, journals, and events associated with SIGDA. It is important that the candidate be willing to devote the time required for consistent and punctual publication of the newsletter every month, over years.

Application: Interested community members are requested to send an email to the ACM SIGDA Communications Chair, Preeti Ranjan Panda (panda@cse.iitd.ac.in), with a CV and 1-2 paragraphs indicating their interest in and willingness to devote the time required for successful operation of the newsletter activity. Applications are due by 15 November, 2023.

Messages from the EiCs

Dear ACM/SIGDA members,

We are excited to present to you November E-Newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter.

The newsletter covers a wide range of information from the upcoming conferences to technical news and activities of our community. Get involved and contact us if you want to contribute articles or announcements.

The newsletter is evolving. Please let us know what you think.

Happy reading!

Debjit Sinha, Keni Qiu,
Editors-in-Chief,
SIGDA E-News

SIGDA News

1. IBM's New Chip Architecture Points to Faster, More Energy-Efficient AI

A new chip prototype (NorthPole) from IBM Research's lab in California, long in the making, has the potential to upend how and where AI is used efficiently.

2. Cadence and Broadcom to Implement AI-Driven Design

Cadence Design Systems has announced a collaboration with Broadcom to implement new AI-driven design flows to accelerate the delivery of their innovative 3nm and 5nm designs.

3. Nvidia, AMD Set to Challenge Intel with ARM-based PC Processors

Both Nvidia Corp and Advanced Micro Devices Inc. are developing Arm-based processors for use in Windows personal computers that could appear in 2025.

4. Fully-Coherent RISC-V Tensor Unit Boosts AI Applications

Semidynamics has just announced a RISC-V Tensor Unit that is designed for ultra-fast AI and is based on its fully customisable 64-bit cores.

5. $35m for 200mm GaN-on-silicon at GlobalFoundries

GlobalFoundries has been awarded $35m to accelerate volume manufacturing of its gallium nitride (GaN) on silicon at Essex Junction, Vermont.

6. US Selects Four Semiconductor Tech Hubs

The US government has announced four tech hubs are aimed at regaining leadership in semiconductor manufacturing, none of which are anywhere near Silicon Valley or California.

7. €130m for 27 6G OProjects in Europe

The Smart Networks and Services Joint Undertaking (SNS JU) has announced the 27 projects in its second call for proposals with funding of €130m.

8. India Plans IMEC-Like Research Center with US$8 Billion Budget

India's Semiconductor R&D Committee has submitted a report recommending the creation of the India Semiconductor Research Center (ISRC) at a cost of US$8 billion over the next five years.

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AE for Local chapter news

Xunzhao Yin,
AE for Awards

What is

Contributing author: Giovanni Ansaloni, and David Atienza
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What is bitline computing?

For decades, the organization of computing architecture has followed the principles laid out by John Von Neumann in 1945[i]. Von Neumann's architecture, as it came to be known, enforced separation between the electronics employed to store data and to process it. Such separation has shaped the computing systems design industry, as nowadays, it is common for memories and processors to reside on different chips, employ other fabrication technologies, and be designed by various companies.

Nonetheless, the Von Neumann paradigm is being increasingly challenged. On the technology side, it faces the slowdown of Moore's law. Such law is indeed not a "law" per se, but the observation, made by Gordon Moore in 1965, that transistor size halves every 18 months, exponentially increasing the performance of integrated circuits. It has been proven to be remarkably accurate for 50 years, but it is projected not to be sustainable in the near future. At the same time, the increase in complexity of applications, especially machine learning (ML) ones, is continuous and unabated. In 2012, the foundational AlexNet network[ii] employed 0.7 GFLOPs (billions of floating-point operations) to process each input. Ten years later, ViT-G/14 requires almost 3 000 GFLOPs[iii].

Moore's law demise and the explosion in ML model sizes have forced computer architects to think out of the box, looking for solutions to increase computational performance and efficiency, which are **not** predicated on ever-smaller, ever-faster transistors. One such out-of-the-box idea is to break Von Neumann's separation between storing and processing data, devising ways to employ memory structures to support computational patterns. Memories are, by nature, highly parallel, and can therefore host many operations at once, as machine learning requires. Furthermore, the more computations are done in memory, the less costly and slow data transfers are needed. Many in- or near-memory approaches are being actively studied, targeting different technologies

Xun Jiao,
AE for What is

Muhammad Shafique,
AE for What is

Rajsaktish Sankaranarayanan,
AE for Researcher spotlight

Xin Zhao,
AE for Paper submission

Ying Wang,
AE for Technical activities

Jiaqi Zhang,
AE for Technical activities

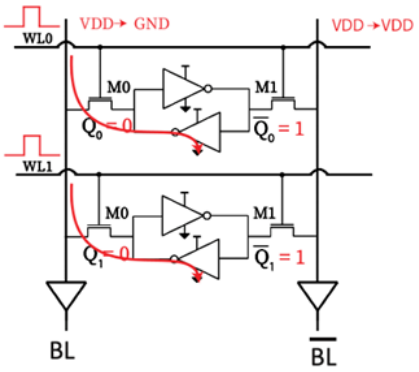
Paper Deadlines

ACM Transactions on Design Automation of Electronic Systems Special Issue on EMBEDDED SYSTEM SOFTWARE/TOOLS
Deadline: Nov. 31, 2023
https://todaes.acm.org

DAC'24 – Design Automation Conference
San Francisco, CA
Research Paper Deadline: Nov. 20, 2023
Abstracts due: Nov. 13, 2023
Engineering Tracks Deadline: Jan. 16, 2024
June 23-27, 2024
http://www.dac.com/

FCCM' 24 - IEEE International Symposium On Field-Programmable Custom Computing Machines
Orlando, FL
Deadline: Jan. 15, 2024
Abstracts due: Jan. 9, 2024

(DRAM, RRAM, SRAM), and operating in the digital or analog domain[iv]. Bitline computing is a particularly promising member of the compute memory family, as it requires few modifications to standard static RAMs (SRAMs) architectures to transform them into capable computing engines.



Q_0	Q_1	BL	$\overline{BL}$
0	0	0	1
0	1	0	0
1	0	0	0
1	1	1	0

BL: AND(Q0,Q1)

$\overline{BL}$: NOR(Q0,Q1)

Figure 1 In bitline computing memories, two memory cells are activated in the same clock cycle. The discharge of the bitlines computes AND and NOR values. The example highlights the case where $Q_0 = Q_1 = 0$.

Bitline compute memory exploits the memory read mechanism as an opportunity for computation[v].[vi]. To read a stored value in standard (non-compute) SRAMSs, wires called "bitlines" are pre-charged and then connected to a memory cell. If the memory contains a '0', the voltage of the bitlines discharges; otherwise, it retains its high value. A "bitline-negated" wire is also present, sensing the complemented value. Bitline-compute SRAMs slightly alter this mechanism by allowing **two** cells to be connected at the same time to the bitlines[vii]. Hence, two alternative discharge paths are possible through the first and the second cell. As shown in Figure 1, bitlines carry the AND and NOR of the two memory cell states. While this may not seem much at first sight, it is the key insight of bitline computing because it enables the combination of values stored at different memory locations within a single read operation (and with no processor involved!). Only a bit of additional logic is required to implement additions, multiplications, and ultimately entire layers composing neural network models.

Bitline computing architectures require a larger area than regular memories, but achieve much more energy efficient and high-performance computing solutions, particularly for the context of ML implementations. As example, in Rios et al.[viii] it is shown that an 82KB compute SRAM, occupying 0.15mm^2 in a 28 nm technology, can process up to 73 inputs per second while consuming only 71 mJ per input. Therefore, this new family

May 5-8, 2024
https://www.fccm.org/

HOST'24 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
Washington DC
Deadline (winter submission): Dec. 18, 2023
Abstracts due: Dec. 11, 2023
May , 2024
http://www.hostsymposium.org

Upcoming Conferences

MICRO'23 – IEEE/ACM Int'l Symposium on Microarchitecture
Toronto, Canada
Oct. 28 - Nov. 1, 2023
http://www.microarch.org/micro56

ICCAD'23 – IEEE/ACM Int'l Conference on Computer-Aided Design
San Francisco, CA
Oct 29 - Nov 2, 2023
https://iccad.com/

ICCD'23 – IEEE Int'l Conference on Computer Design
Washington DC, US
Nov. 6-8, 2023
http://www.iccd-conf.com

FPT'23 - Int'l Conference on Field-Programmable Technology
Yokohama, Japan
Dec. 11-14, 2023
http://icfpt.org

of bitline computing architectures beyond the Von Neumann paradigm is an up-and-coming solution for ML processing, which is getting very significant industrial support for latest technology nodes.

References

[i] John von Neumann, John “First Draft of a Report on the EDVAC”, 1945.
[ii] Krizhevsky, Alex, Ilya Sutskever, and Geoffrey E. Hinton. "Imagenet classification with deep convolutional neural networks." *Advances in neural information processing systems* 25 (2012).
[iii] Zhai, Xiaohua, et al. "Scaling vision transformers." *Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition*. 2022.
[iv] Gebregiorgis, Anteneh, et al. "A survey on memory-centric computer architectures." *ACM Journal on Emerging Technologies in Computing Systems (JETC)* 18.4 (2022): 1-50.
[v] Jeloka, Supreet, et al. "A 28 nm configurable memory (TCAM/BCAM/SRAM) using push-rule 6T bit cell enabling logic-in-memory." *IEEE Journal of Solid-State Circuits* 51.4 (2016): 1009-1021.
[vi] Ponzina, Flavio, et al. "A flexible in-memory computing architecture for heterogeneously quantized CNNs." *2021 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. IEEE, 2021.
[vii] Simon, William Andrew, et al. "BLADE: An in-cache computing architecture for edge devices." *IEEE Transactions on Computers* 69.9 (2020): 1349-1363.
[viii] Rios, Marco, et al. "Bit-Line Computing for CNN Accelerators Co-Design in Edge AI Inference." *IEEE Transactions on Emerging Topics in Computing* (2023).

SIGDA Awards

1. **Best Paper Award @ MEMOCODE 2023**

https://invasic.informatik.uni-erlangen.de/en/old_news.php

Hybrid Genetic Reinforcement Learning for Generating Run-Time Requirement Enforcers (nominated for MEMOCODE BPA)

Jan Spieck, Pierre-Louis Sixdenier, Khalil Esper, Stefan Wildermann and Jürgen Teich

Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU)

HiPC'23 – IEEE Int'l Conference on High Performance Computing, Data, And Analytics
Goa, India
Dec. 18-21, 2023
http://www.hipc.org

iSES’23 – IEEE Int’l Symposium on Smart Electronic Systems
Ahmedabad, India
Dec. 18-20, 2023
http://www.ieee-ises.org

ASP-DAC'24 - Asia and South Pacific Design Automation Conference
Incheon Songdo Convensia, South Korea
Jan. 22-25, 2024
http://www.aspdac.com

VLSID'24 – International Conference on VLSI Design & International Conference on Embedded Systems
ITC Royal Bengal, Kolkata, India
Jan. 6-10, 2024
https://vlsid.org/

HiPEAC'24: Int'l Conference on High Performance Embedded Architectures & Compilers
Munich, Germany
Jan. 17-19, 2024
https://www.hipeac.net/2024/munich/

ISSCC'24 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Feb. 18-22, 2024
http://isscc.org

FPGA’24 – ACM/SIGDA Int’l Symposium on Field-Programmable Gate Arrays
Monterey, CA
Mar. 3 - 5, 2024
http://www.isfpga.org

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems, TODAES, publishes innovative work documenting significant research and development advances on the specification, design, analysis, simulation, testing, and evaluation of electronic systems, emphasizing a computer science/engineering orientation. Design automation for machine learning/AI and machine learning/AI for design automation are very much welcomed.

If you are an active researcher in the design and design automation field and would like to be part of the TODAES review board, please fill out the following reviewer form. TODAES recognizes those reviewers that provide timely and high-quality reviews through the Distinguished Review Board. TODAES also recognizes papers and outstanding junior researchers through best paper and rookie of the year award. Authors can send their paper submissions on the manuscript portal.

TODAES welcomes special issue proposals from leading researchers/practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

CALL FOR PAPERS:

Special Issue on EMBEDDED SYSTEM SOFTWARE/TOOLS

TODAES special issue on embedded systems software/tools invites submissions focus on the following (nonexhaustive) topic areas:

- High level synthesis of embedded systems
- Electronic design automation tools
- Power, performance, area modeling tools
- Design space exploration
- Resource and thermal management for embedded systems
- Application-specific architectures
- Artificial intelligence on edge devices, IoT
- Hardware reliability and security

Submissions deadline: **November 31, 2023**

ISPD'24 – ACM Int'l Symposium on Physical Design
Taipei, Taiwan
Mar. 12-15, 2024
http://www.ispd.cc

DATE'24 - Design Automation and Test in Europe
Valencia, Spain
Mar. 25-27, 2024
http://www.date-conference.com

ISQED'24 - Int'l Symposium on Quality Electronic Design
San Francisco, CA
Apr. 3-5, 2023
http://www.isqed.org

RTAS'24 - IEEE Real-Time and Embedded Technology and Applications Symposium
Hong Kong, China
May 13-16, 2024
http://2024.rtas.org

ISCAS'24 – IEEE Int'l Symposium on Circuits and Systems
Singapore
May 19-22, 2024
http://iscas2024.org

Technical Activities

1. Qualcomm Takes On AMD, Apple, Intel With Snapdragon X Elite

At this year's Snapdragon Summit, Qualcomm released its most formidable PC processor yet. The Snapdragon X Elite, which is designed to run Windows, will provide real competition to AMD and Intel for notebook PCs…

2. Renesas Launches Induction Motor Position Sensing Technology

Utilizing non-contact coil sensors, Renesas' position sensing technology can replace expensive magnetic and optical encoders being used now in motor control systems…

3. SYSCOM Unveils 5G Private Network Cooperation, Generative AI Achievements at AIoT Exhibition 2023

SYSCOM has launched a domestic 5G enterprise private network to showcase its powerful integration strength. During the conference, SYSCOM also announced the research and application results of generative AI, making this year's AIoT Exhibition more attractive…

4. The Future of Medical Research: HPC, AI & HBM

CPUs and GPUs with high bandwidth performance and AI functionality deliver big benefits in HPC for advances in healthcare and medicine…

Job Positions

1. Portland State University, US

Job Title: ECE Assistant Professor

Description: The Department of Electrical & Computer Engineering (ECE) at Portland State University seeks outstanding candidates for one or several tenure-track faculty positions at the level of Assistant Professor, with research and teaching interests in two areas: (1) electric power systems or (2) computer engineering. The position will work closely with other members of the ECE Department and Maseeh College interdisciplinary research focused on areas of either electric power systems or computer engineering. These include (1) cyber-physical power

systems, power system data science, power systems cybersecurity, or power systems protection, or (2) beyond-Moore computing architectures, nanoscale computing architectures, neuromorphic engineering, biomolecular computing, future and emerging computing paradigms and architectures, design automation, or design verification and validation. Other power or computer engineering areas will also be considered. The position will build a research and teaching program through actions that contribute to the Department's aims to improve diversity, equity, and inclusion within the ECE Department. It will develop and maintain scholarly funded research; develop coursework relevant to the research field; teach undergraduate and graduate courses; advise students; and provide service to the university, professional societies, and the public. The position will initiate a research program that can be sponsored by external funding agencies. This program should expand, complement, and collaborate with the existing research activities in the ECE Department and/or build connections within the broader community. Research should also align with the strategic vision of the Maseeh College of Engineering and Computer Science and/or the strategic vision of the ECE Department. For more information, please refer to https://www.higheredjobs.com/faculty/details.cfm?JobCode=178584531&Title=ECE%20Assistant%20Professor%20%2D%20Power%20or%20Computer%20Engineering.

2. University of Washington, US

Job Title: Assistant Professor of Electrical Engineering

Description: The Engineering & Mathematics Division of the School of Science, Technology, Engineering & Mathematics (STEM) at the University of Washington Bothell (UWBothell) invites applications for a tenuretrack positionin Electrical Engineering at the rank of Assistant Professor. The successful candidate will join our faculty on a full-time basis for a nine-month academic year appointment beginning September 16, 2024.All University of Washington faculty engage in teaching, research/scholarship and service. Candidates will be consideredacross a wide range of research and teaching interests, including but not limited to,digital circuit design, FPGA implementation, embedded systems design, and VLSI and ASIC design.The successful candidate is also expected to teach other electrical engineering courses and develop an active research agenda, resulting in scholarly publications in reputable journals and conferences, along with securing external funding to support research endeavors. The successful candidate is strongly encouraged to engage in interdisciplinary collaboration, both in teaching and research, with a particular focus on opportunities that benefit undergraduate and master's students. The candidate is also expected to be actively engaged in service activities across the campus and the University, including membership in committees, student mentoring, curricular development and other activities that contribute to the University's mission and goals. The candidate is expected to be committed to supporting students from diverse backgrounds, actively enhancing their learning experience, and

creating an inclusive and supportive learning environment. For more information, please refer to https://facultyvacancies.com/assistant-professor-of-electrical-engineering,i36987.html.

3. RMIT University of Texas Austin, US

Job Title: Assistant Professor of Computer Engineering

Description: Candidates in the following areas of electrical and computer engineering will be considered, especially as they align with the strategic focus of the department (candidates are encouraged to view these areas of emphasis in the broadest sense in determining whether they match their research skills and interests): (i) 6G-era wireless communications, networking, and/or sensing (in this area, exceptional candidates at the associate or full professor level may be considered); (ii) Cyber-security and privacy, including network security, secure hardware, data anonymization, data privacy, and secure data storage, as well as topics that might have a tie into emerging areas in ML; (iii) Heterogeneous computer and communication systems, including, but not limited to computer architecture, computer networks, system software, accelerators, edge, rack, and data center system architecture, and opportunities in new multi-chip systems; and (iv) Electromagnetics and applications including EM theory and computation, antenna design and RF systems, quantum information processing and photonics, remote sensing and radar, and biomedical systems. Applicants should have received or expect to receive a doctoral degree in electrical engineering, computer engineering, computer science, or a related discipline prior to September 2024. Successful candidates are expected to mentor graduate students, teach our diverse undergraduate and graduate student populations, develop an externally sponsored research program, collaborate with other faculty from a wide range of backgrounds, and be involved in service to the university and profession. For more information, please refer to https://facultyvacancies.com/assistant-professor-of-computer-engineering,i36919.html.

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