



Special Interest Group on Design Automation **ACM/SIGDA E-NEWSLETTER**, Vol. 53, No. 5

SIGDA - The Resource for EDA Professionals

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SIGDA News

1. [U.S. Crawls Toward Rebuilding Frail PCB Industry](#)

Recent efforts by the U.S. government to rebuild the nation's nearly extinct printed circuit board (PCB) industry are tentative and inadequate steps toward one of the weakest links in the domestic electronics supply chain, experts told EE Times in exclusive interviews.

2. [Rapidus Secures US\\$2.3bn to Start 2nm Wafer Fab](#)

Japan's Ministry of Economy, Trade, and Industry (METI), is finalizing plans to provide Rapidus Co. Ltd. with 300 billion yen (about US\$2.3 billion) to build a wafer fab on the northern island of Hokkaido.

3. [Micron's \\$1bn Indian Chip Packaging Plant Close to Approval](#)

A budget of about US\$1 billion has been put on a chip assembly, testing, marking and packaging (ATMP) facility that memory maker Micron could soon receive approval for in India.

4. [TSMC Could Partner with Bosch for 28nm Fab in Germany](#)

Leading foundry TSMC could partner with Robert Bosch and two other automotive suppliers to create a joint-venture 300mm fab in Germany that will target a 28nm process technology.

5. [TSMC Says 2nm on Track for 2025 as It Broadens 3nm Offer](#)

TSMC's next-generation nominal '2nm' manufacturing process is making solid progress and is due to enter production in 2025, the leading foundry said at its North America Technology Symposium.

Messages from the EiCs

Dear ACM/SIGDA members,

We are excited to present to you May E-Newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter.

The newsletter covers a wide range of information from the upcoming conferences to technical news and activities of our community. Get involved and contact us if you want to contribute articles or announcements.

The newsletter is evolving. Please let us know what you think.

Happy reading!

Debjit Sinha, Keni Qiu,
Editors-in-Chief,
SIGDA E-News

6. [Top 25 Global and Chinese Chip Companies Ranked](#)

Market analyst Gartner Inc. has produced the ranking of the top 25 semiconductor manufacturers in the world and in mainland China by 2022 revenues.

What is

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AE: Xun Jiao <xjiao@villanova.edu>

What is Concolic Testing?

Yangdi Lyu
Assistant Professor,
Microelectronics Thrust,
The Hong Kong University of Science and Technology (Guangzhou)

Concolic testing is an automated test generation technique that combines CONcrete simulation and symbOLIC execution. Concolic testing was first proposed and successfully applied in the software domain [1-3]. The KLEE [3] tool is one of the open-source concolic testing tools widely used in academia and industry. In recent years, concolic testing has been successfully applied in the hardware domain [4-6] to cover branches, detect hardware Trojans, and generate counterexamples in RTL models.

During validation and verification, common industry practice runs millions of random or constrained-random tests to cover most functional scenarios quickly. However, it is not always possible to cover all scenarios using these tests. Verification engineers usually need to write test cases to cover the remaining hard-to-activate scenarios manually. Formal methods, such as model checking [7], can cover specific scenarios directly but suffer from state explosion for large designs. Concolic testing combines the advantages of simulation and formal methods to cover targets efficiently.

Concolic testing starts from a simulation and continuously explores alternate branches to cover a target. Based on different alternative branch selection strategies, concolic testing can be broadly classified into two categories. The first one is uniform test generation [8]. Uniform test generation techniques utilize depth-first search (DFS) or breadth-first search (BFS) in alternative branch selection to maximize the overall coverage. While theoretically uniform test generation can cover all branches given enough long time, it suffers from exponentially growing paths, making exhaustive searching impractical for large designs. The second is directed test generation, which can generate a test to activate

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specific targets. For example, Lyu et al. [4] applied concolic testing to cover target branches in RTL models by utilizing static analysis of distance metrics in control flow graphs (CFGs) to guide path exploration.

Compared to model checking, concolic testing explores one path at a time and can be applied in large designs. However, while it solves the state explosion problem in formal methods, a bad branch selection strategy may lead the simulation trace randomly or far away from the targets. The corresponding path exploration stage in concolic testing may take longer than the time budget but still never converge to the desired target, which is called the path explosion problem. As a result, designing a good heuristic in path exploration is one of the fundamental challenges in concolic testing.

In summary, concolic testing is a promising testing approach in both software and hardware. Compared to formal methods, concolic testing is suitable for large designs since it relies on concrete simulation and the symbolic execution of a single path. The main challenge of concolic testing is guiding the path exploration to cover specific targets.

References

- [1] Koushik Sen, Darko Marinov, and Gul Agha. “Cute: A concolic unit testing engine for C,” In ACM SIGSOFT Software Engineering Notes, vol. 30, no. 5, pp. 263–272, 2005.
- [2] Patrice Godefroid, Nils Klarlund, and Koushik Sen. “DART: Directed automated random testing,” In ACM Sigplan Notices, vol. 40, no. 6, pp. 213–223, 2005.
- [3] Cristian Cadar, Daniel Dunbar, and Dawson Engler. “KLEE: Unassisted and automatic generation of high-coverage tests for complex systems programs,” In USENIX Symposium on Operating Systems Design and Implementation (OSDI 2008), pp. 209–224, 2008.
- [4] Yangdi Lyu and Prabhat Mishra, “Scalable Concolic Testing of RTL Models” in IEEE Transactions on Computers (TC), 2021.
- [5] Yangdi Lyu, Alif Ahmed, and Prabhat Mishra, “Automated Activation of Multiple Targets in RTL Models using Concolic Testing” in 2019 Design, Automation and Test in Europe Conference & Exhibition (DATE), 2019.
- [6] Yangdi Lyu and Prabhat Mishra, “Automated Test Generation for Activation of Assertions in RTL Models” in Asia and South Pacific Design Automation Conference (ASPDAC), 2020.
- [7] Angelo Gargantini and Constance Heitmeyer, “Using model checking to generate tests from requirements specifications,” In ACM SIGSOFT Software Engineer Notes, vol. 24, no. 6, pp. 146–162, 1999.
- [8] Alif Ahmed and Prabhat Mishra, “QUEBS: Qualifying event based search in concolic testing for validation of RTL models,” In 2017 IEEE International Conference on Computer Design (ICCD), 2017.

SIGDA Awards

1. ISPD Best Paper Award @ ISPD 2023

<https://ispd.cc/ispd2023/index.php?page=awards>

Xun Jiao,

AE for What is

Muhammad Shafique,

AE for What is

Rajsaktish Sankaranarayanan,

AE for Researcher spotlight

Xin Zhao,

AE for Paper submission

Ying Wang,

AE for Technical activities

Jiaqi Zhang,

AE for Technical activities

Paper Deadlines

MEMOCODE'23 - IEEE/ACM Int'l Conference on Formal Methods and models for System Design (co-located with ESWEEK 2023)

Hamburg, Germany

Deadline: May 5, 2023

(Abstracts due: Apr 28, 2023)

Sept 21-22, 2023

<https://memocode2023.github.io>

OSCAR'23 - Second Workshop on Open-Source Computer Architecture Research

Orlando, FL

(co-located with ISCA 2023)

Abstract deadline: May 5, 2023

June 18, 2023

<https://oscar-workshop.github.io/>

ICCAD'23 – IEEE/ACM Int'l Conference on Computer-Aided Design

San Francisco, CA

Deadline: May 22, 2023

"FastPass: Fast Pin Access Analysis with Incremental SAT Solving",
Fangzhou Wang, Jinwei Liu, Evangeline F. Y. Young (The Chinese University
of Hong Kong)

2. Contest Winners @ ISPD 2023

<https://ispd.cc/ispd2023/index.php?page=home>

(1) FDUEA

Fudan University: Peng Zou, Min Wei, Xingyu Tong, Binggang Qiu, Zhijie
Cai, Guohao Chen, Benchao Zhu, Jiawei Li, Jun Yu, Jianli Chen

(2) NTHU-TCLAB

National Tsing Hua University: Chun-Wei Chiu, Min-Feng Hsieh, Chia-Hsiu
Ou, Ting-Chi Wang

(3) CUEDA

The Chinese University of Hong Kong: Bangqi Fu, Qijing Wang, Yang Sun,
Qin Luo, Anthony W. H. Lau, Fangzhou Wang, Evangeline F. Y. Young

(4) XDSecurity-II

XiDian University: Shunyang Bi, Guangxin Guo, Haonan Wu, Zhengguang
Tang, Hailong You, Cong Li

3. IEEE CEDA Service Award @ DATE 2023

<https://www.date-conference.com/>

Cristiana Bolchini, Politecnico di Milano, IT

4. ESDA / CEDA Phil Kaufman Award 2022 @ DATE 2023

<https://www.date-conference.com/>

Giovanni De Micheli, EPFL, CH

5. IEEE CS TTTC Outstanding Contribution Award @ DATE 2023

<https://www.date-conference.com/>

Ian O'Connor, École Centrale de Lyon, FR

6. ACM SIGDA/CEDA/EDAA PhD Forum Prize @ DATE 2023

<https://www.date-conference.com/>

Alessio Burrello, Politecnico di Torino and Università di Bologna, IT
Optimizing Ai: From Network Topology Design To Mcu Deployment

Jatin Arora, CISTER Research Centre, ISEP, IPP, PT
Shared Resource Contention Aware Schedulability Analysis For
Multiprocessor Real-Time Systems

(Abstracts due: May 15, 2023)

Oct 29 - Nov 2, 2023

<http://www.iccad.com>

VLSI-SoC'23 – IFIP/IEEE Int'l

**Conference on Very Large Scale
Integration**

Dubai, UAE

Deadline: May 23, 2023

(Abstracts due: May 16, 2023)

Oct 16-18, 2023

<http://www.vlsi-soc.com>

BioCAS'23 – Biomedical Circuits and Systems Conference

Toronto, Canada

Deadline: June 9, 2023

Oct 19-21, 2023

<https://2023.ieee-biocas.org/>

HiPC'23 – IEEE Int'l Conference on High Performance Computing, Data, And Analytics

Goa, India

Deadline: July 7, 2023

(Abstracts due: June 30, 2023)

Dec 18-21, 2023

<http://www.hipc.org>

Upcoming Conferences

HOST'23 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust

San Jose, CA

May 1-4, 2023

<http://www.hostsymposium.org>

7. EDAA Outstanding Dissertations Award 2023 @ DATE 2023

<https://www.date-conference.com/>

Topic 1:

Xiaochen Peng, Ph.D

Benchmark Framework for 2-D/3-D Integrated Compute-in-Memory based Machine Learning Accelerator

Topic 2:

Martin Rapp, Ph.D.

Machine Learning for Resource-Constrained Computing Systems

Topic 3:

Zhiyao Xie, Ph.D.

Intelligent Circuit Design and Implementation with Machine Learning

Topic 4:

Hasan Hassan, Ph.D.

Improving DRAM Performance, Reliability, and Security by Rigorously Understanding Intrinsic DRAM operations

8. DATE Fellow Award 2023 @ DATE 2023

<https://www.date-conference.com/>

Cristiana Bolchini, Politecnico di Milano, IT

9. DATE Best Paper Awards 2023 @ DATE 2023

<https://www.date-conference.com/>

D-Track:

Hardware Efficient Weight-Binarized Spiking Neural Networks

Chengcheng Tang and Jie Han, University of Alberta, CA

A-Track:

Automated Energy-Efficient DNN Compression under Fine-Grained Accuracy Constraints

Ourania Spantidi and Iraklis Anagnostopoulos

Southern Illinois University Carbondale, US

T-Track:

SAGERoute: Synergistic Analog Routing Considering Geometric and Electrical Constraints with Manual Design Compatibility

Haoyi Zhang, Xiaohan Gao, Haoyang Luo, Jiahao Song, Xiyuan Tang,

Junhua Liu, Yibo Lin, Runsheng Wang and Ru Huang

Peking University, CN

E-Track:

PRADA: Point Cloud Recognition Acceleration via Dynamic Approximation

Zhuoran Song, Heng Lu, Gang Li, Li Jiang, Naifeng Jing and Xiaoyao Liang

Shanghai Jiao Tong University, CN

MDTS'23 – IEEE Microelectronics Design & Test Symposium

Albany, NY

May 8-10, 2023

<http://natw.ieee.org>

FCCM' 23 - IEEE International Symposium On Field-Programmable Custom Computing Machines

Los Angeles, CA

May 8 - 11, 2023

<https://www.fccm.org/>

ISCAS'23 – IEEE Int'l Symposium on Circuits and Systems

Monterey, CA

May 21 - 25, 2023

<http://iscas2023.org>

RTAS'23 - IEEE Real-Time and Embedded Technology and Applications Symposium

San Antonio, Texas

May 9-12, 2023

<http://2023.rtas.org>

GLSVLSI'23 – ACM Great Lakes Symposium on VLSI

Knoxville, TN

June 5-7, 2023

<http://www.glsvlsi.org>

IWLS'23 - International Workshop on Logic & Synthesis

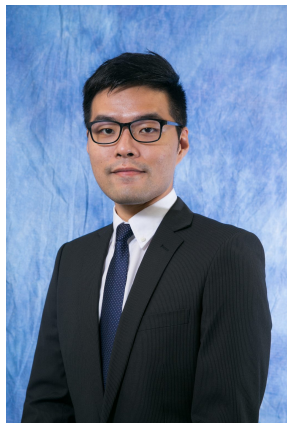
EPFL, Lausanne, Switzerland

June 5-6, 2023

<https://www.iwls.org>

ISVLSI'23 – IEEE Computer Society Annual Symposium on VLSI

Who's Who



Ming-Chang Yang

Associate Professor

Department of Computer Science and Engineering, The Chinese University of Hong Kong

Research interests: Emerging non-volatile memory and storage technologies, memory and storage systems, and the next-generation memory/storage architecture designs

Email: mcyang@cse.cuhk.edu.hk

Personal webpage: <http://www.cse.cuhk.edu.hk/~mcyang/>



Scott Beamer

Assistant Professor

Department of Computer Science & Engineering, University of California, Santa Cruz

Iguana Falls, Brazil

June 20 - 23, 2023

<http://www.ieee-isvlsi.org>

DAC'23 – Design Automation Conference

San Francisco, CA

July 9-13, 2023

<http://www.dac.com/>

ICDCS'23 – IEEE Int'l Conference on Distributed Computing Systems

Hong Kong, China

Jul 18 - 21, 2023

<https://www.icdcs.org/>

ISLPED'23 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design

Vienna, Austria

Aug 7-8, 2023

<http://www.islped.org>

ESWEEK'23 - Embedded Systems Week

Hamburg, Germany

Sept. 17-22, 2023

<http://www.esweek.org>

NOCS'23 – IEEE/ACM Int'l Symposium on Networks-on-Chip (co-located with ESWEEK 2023)

Hamburg, Germany

Sept 21-22, 2023

<https://nocs2023.github.io>

PACT'23 - Int'l Conference on Parallel Architectures and Compilation Techniques

Vienna, Austria

Oct 21-25, 2023

<http://www.pactconf.org>

Email: sbeamer@ucsc.edu

Personal webpage: <https://scottbeamer.net>

Research interests: Agile and open-source hardware design, computer architecture, graph processing, and data movement optimization

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems, TODAES, publishes innovative work documenting significant research and development advances on the specification, design, analysis, simulation, testing, and evaluation of electronic systems, emphasizing a computer science/engineering orientation. Design automation for machine learning/AI and machine learning/AI for design automation are very much welcomed.

If you are an active researcher in the design and design automation field and would like to be part of the TODAES review board, please fill out the following [reviewer form](#). TODAES recognizes those reviewers that provide timely and high-quality reviews through the [Distinguished Review Board](#). TODAES also recognizes papers and outstanding junior researchers through [best paper](#) and [rookie of the year](#) award. Authors can send their paper submissions on the [manuscript portal](#).

TODAES welcomes special issue proposals from leading researchers/practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

Technical Activities

1. [NexCOBOT Builds x86 Functional Safety Robot Control Solution](#)

NexCOBOT and its ecosystem partners is showcasing a new functional safety robot control solution in Hannover Messe 2023...

2. [Amazon Sidewalk Devices Can Now Be Built Using Nordic's Existing nRF Connect SDK](#)

Nordic Semiconductor's Bluetooth technology is once again at the forefront of one of the biggest industry developments in wireless IoT...

3. [‘Quantum Calculator’ Algorithm Tackles Optimization Problems](#)

Multiverse Computing has demonstrated how quantum computers with few qubits can already implement arbitrary multidimensional function calculus in a remarkably efficient way...

4. [Speakers at AICS Go In Depth on Green AI Computing](#)

The theme of the 5th IBM IEEE AI Compute Symposium (AICS), held at an IBM research center last fall in New York, was “scalability to sustainability.” Symposium presenters from industry and academia covered a range of topics, including device technology, circuits, architecture, algorithms and sustainability to make innovations for the cloud, with an emphasis on green artificial intelligence...

Job Positions

1. Royal Institute of Technology School of Engineering Sciences, Sweden

Job Title: Doctoral student in filtering techniques

Description: Filtering is a powerful tool in computational fluid dynamics that can aid in accurately and efficiently predicting the governing physics in simulations, leading to improved designs. Filters can enable data compression, damping unphysical oscillations, and revealing multi-scale physics such as in turbulence modelling. Smoothness-Increasing Accuracy-Conserving (SIAC) post-processing filters, are typically used to extract hidden information in certain numerical simulations, creating even more accurate representations of the data. They are flexible enough to incorporate information from experimental data. In the past, SIAC filtering has relied on B-splines and often has a tensor-product structure in multi-dimensions. This PhD project will focus on developing a multi-variate filtering framework for applications to general multi-dimensional geometries. The main application will be to data compression. The project will entail aspects from approximation theory, error estimation of simulation data, and contribution to the SIAC Magic ToolBox. The project will span theory, algorithms, and applications. No pre-requisite knowledge in filtering is required. Last application date 19.May.2023. For more information, please refer to <https://facultyvacancies.com/doctoral-position-in-filtering-techniques.i33920.html>.

2. Michigan State University College of Engineering, US

Job Title: Assistant/Associate/Full Professor in Electrical and Computer Engineering

Description: The College of Engineering at Michigan State University (MSU) invites applications in all areas related to semiconductor science and engineering for up to four open-rank, tenure-system faculty positions. Candidates must have a doctorate in engineering or a closely related science engineering discipline at the time of appointment, which will be available as of August 16, 2023. The candidate will be expected to develop a nationally recognized research program and teach courses within the College at both the undergraduate and graduate levels. All areas of research specialization will be considered, but the following areas have been identified as being of particular interest: Heterogeneous microsystem integration of semiconductors and associated radiation effects for space electronics applications. 6G/Millimeter-Wave RF devices and electronics and understanding of the mechanisms of radiation damage on device performance and lifetime for space electronics applications. RF devices and circuit design, testing, and radiation tolerant approaches for space electronics applications. Additive manufacturing of dielectric materials for high-performance, radiation-tolerant electronics for space applications. Development of semiconducting materials for radiation-tolerant electronics for space applications. For more information, please refer to <https://facultyvacancies.com/assistantassociatefull-professor-in-electrical-and-computer-engineering.i33839.html>.

3. Tokyo Institute of Technology School of Engineering, Japan

Job Title: Assistant Professor in Information and Communication

Description: Area of Specialization: Common underlying areas of information and communication fields and data science fields, e.g., mathematical models and algorithms for applications to signal processing, optimization and inverse problems, etc. The successful candidate will be responsible for lectures, exercises, and experiments related to information and communications for undergraduate and graduate students. The successful candidate will be required to supervise graduate and undergraduate students. The successful candidate will be required to conduct remarkable and international research in the specialized fields. The successful candidate will be responsible for managing the Department of Information and Communications Engineering and the Institute. Applicants must hold a PhD or have equivalent competence. Applications must be received by June 30, 2023. For more information, please refer to <https://facultyvacancies.com/assistant-professor-in-information-and-communication.i34011.html>.

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Aims of the Conference:

ASP-DAC 2024 is the 29th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design, CAD and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to design and Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC. ASP-DAC recognizes excellent contributions with the Best Paper Award and 10-Year Retrospective Most Influential Paper Award. Selected papers will be invited to submit the extended version of their work to a Special Issue of Integration, the VLSI Journal.

Areas of Interest:

Original papers in, but not limited to, the following areas are invited.

[1] System-Level Modeling and Design Methodology:

- 1.1. HW/SW co-design, co-simulation and co-verification
- 1.2. System-level design exploration, synthesis, and optimization
- 1.3. System-level formal verification
- 1.4. System-level modeling, simulation and validation
- 1.5. Networks-on-chip and NoC-based system design

[2] Embedded, Cyberphysical (CSP), IoT Systems and Software:

- 2.1. Many- and multi-core SoC architecture
- 2.2. IP/platform-based SoC design
- 2.3. Domain-specific architecture
- 2.4. Dependable architecture
- 2.5. Cyber physical system
- 2.6. Internet of things
- 2.7. Kernel, middleware, and virtual machine
- 2.8. Compiler and toolchain
- 2.9. Real-time system
- 2.10. Resource allocation for heterogeneous computing platform
- 2.11. Storage software and application
- 2.12. Human-computer interface

[3] Memory Architecture and Near/In Memory Computing:

- 3.1. Storage system and memory architecture
- 3.2. On-chip memory architectures and management: Scratchpads, compiler, controlled memories, etc.
- 3.3. Memory/storage hierarchies with emerging memory technologies
- 3.4. Near-memory and in-memory computing
- 3.5. Memory architecture and management for emerging memory technologies

[4] Tools and Design Methods with and for Artificial Intelligence (AI)

- 4.1. Design method for learning on a chip
- 4.2. Deep neural network for EDA
- 4.3. Tools and design methodologies for edge AI and TinyML
- 4.4. Efficient ML training and inference

[5] Hardware Systems and Architectures for AI:

- 5.1. Hardware, device, and architecture for deep neural networks
- 5.2. Systems-level design for (deep) neural computing
- 5.3. Neural network acceleration co-design techniques
- 5.4. Novel reconfigurable architectures including FPGAs for AI/MLs

[6] Photonic/RF/Analog-Mixed Signal Design:

- 6.1. Analog/mixed-signal/RF synthesis
- 6.2. Analog layout, verification, and simulation techniques
- 6.3. High-frequency electromagnetic simulation of circuit
- 6.4. Mixed-signal design consideration
- 6.5. Communication and computing using photonics

[7] Approximate, Bio-Inspired and Neuromorphic Computing:

- 7.1. Circuit and system techniques for approximate and stochastic computing
- 7.2. Neuromorphic computing
- 7.3. CAD for approximate and stochastic systems
- 7.4. CAD for bio-inspired and neuromorphic systems

ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals. The submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, references and bibliographic citations. While research papers with open-source software are highly encouraged where the software will be made publicly available (via GitHub or similar), the authors' identities need to be anonymized in the submitted paper for the double-blind review process. Issuing the paper as a technical report, posting the paper on a website, or presenting the paper at a workshop that does not publish formally reviewed proceedings, does not disqualify it from appearing in the proceedings. Note that each paper shall be accompanied by at least one different conference registration at the speaker's registration rate (e.g., two speaker registrations are needed for presenting two accepted papers). But any registered co-author can present the work at the conference. ACM and IEEE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by any author.

Submission of Papers:

Deadline for abstract submission:

5 PM AOE (Anywhere on earth) July 23 (Sun), 2023

Deadline for PDF uploading:

5 PM AOE (Anywhere on earth) July 28 (Fri), 2023

Announcement of accepted manuscript IDs:

Sept. 9 (Sat), 2023

Notification of acceptance:

Sept. 11 (Mon), 2023

Deadline for final version:

5 PM AOE (Anywhere on earth) Nov. 3 (Fri), 2023

For detailed instructions for submission, please refer to the "Authors' Guide" at: <http://www.aspdac.com/>

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Panels, Special Sessions, and Tutorials: Suggestions and proposals are welcome and have to be addressed to aspdac2024-ss@aspdac.com for special sessions & panels, aspdac2024-tutorial@aspdac.com for tutorials, no later than Aug 31 (Thu), 2023.

Contact: Conference Secretariat: aspdac2024-sec@aspdac.com TPC Secretariat: aspdac2024-tpc@aspdac.com