Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 53, No. 4

SIGDA - The Resource for EDA Professionals

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
Circulation: 2,700

Online archive: http://www.sigda.org/newsletter

SIGDA News

1. **Gordon Moore – In His Own Words**

Gordon Moore, co-founder of Fairchild Semiconductor and Intel, has died at the age of 94. Moore was one of the 'traitorous eight' who founded Fairchild Semiconductor in 1957, going on develop Moore's Law in 1965 predicting that the number of transistors on an integrated circuit would double every year.

2. **ChatGPT Gets Its "Wolfram Superpowers"**

In just two and a half months, the Wolfram team was able to connect ChatGPT with Wolfram|Alpha. Wolfram was the 'go to' place for those who worked and lived in mathematics, but the combination of ChatGPT and Wolfram opens up a complete new interaction. With Wolfram it means ChatGPT is able to do very specific calculations and maths, just by simply asking. Stephen Wolfram explains how Wolfram|Alpha can be seen as a Superpower for AI generators.

3. **ASML, TSMC, Synopsys join Nvidia for Computation Lithography**

Nvidia Corp. has partnered with ASML, Synopsys and TSMC to promote the use of its 'cuLitho' software library for computational lithography.

4. **TSMC Closes in on Intel for Brand Value**

According to a new report from brand valuation consultancy, Brand Finance, Intel has barely retained its title as the world's most valuable semiconductor brand, marginally ahead of TSMC. Intel's brand value is down 10% to US$22.9 billion while the brand value of TSMC rose 5% to US$21.6 billion. Intel has built a partially-consumer-facing brand based upon laptop and desktop computers, in addition to server and industrial

Messages from the EiCs

Dear ACM/SIGDA members,

We are excited to present to you April E-Newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter.

The newsletter covers a wide range of information from the upcoming conferences to technical news and activities of our community. Get involved and contact us if you want to contribute articles or announcements.

The newsletter is evolving. Please let us know what you think.

Happy reading!

Debjit Sinha, Keni Qiu,
Editors-in-Chief,
SIGDA E-News

markets, while TSMC is substantially a business-to-business brand dedicated to manufacturing semiconductors for Apple, AMD, Nvidia and mobile devices.

5. ARM Proposes Change to IP Royalty Model

Processor intellectual property licensor Arm Ltd. is looking to increase sales by changing in its royalty model from one based on chip value to one based on equipment value, according to the Financial Times.

6. South Korea's Chipmaking Spend to Overtake China's in 2024

Taiwan is expected to remain the top ranked region but US sanctions against the export of leading-edge chipmaking equipment to China is expected to keep China's spending flat while South Korea is expected to make a surge in spending so that it reclaims second place, SEMI said.

What is

Contributing author: Fengbin Tu <tufengbin@gmail.com>

AE: Xun Jiao <xjiao@villanova.edu>

What is Reconfigurable Digital Computing-In-Memory?

Fengbin Tu
Adjunct Assistant Professor,
Department of Electronic and Computer Engineering,
The Hong Kong University of Science and Technology

Reconfigurable digital Computing-In-Memory (CIM) is a new architecture paradigm for artificial intelligence (AI) chips, which fuses the spirits of digital CIM and reconfigurable computing. It can well balance efficiency, accuracy, and flexibility, just like human intelligence that flexibly solves intelligence tasks with high efficiency and high accuracy.

Conventional digital AI chips have discrete multiply-accumulation (MAC) units and memory. With the increasing size and computation of AI models, there exist frequent data movements between the MAC units and memory, which significantly affects the overall energy efficiency. Analog CIM is one mainstream technique that eliminates the above memory access bottleneck by implementing analog MAC in memory such as SRAM [1, 2] and Resistive RAM (ReRAM) [3, 4]. When processing an AI model, analog CIM converts inputs to analog signals, and then performs bitwise MAC operations with weights in the analog domain. Although analog CIM saves lots of data movements for higher energy efficiency, the two inherent

drawbacks limits analog CIM's accuracy and flexibility: (1) Analog computing's non-ideal issues cause accuracy loss. (2) The compact data path in memory is difficult to modify, so the CIM function is usually limited to only INT MAC.

In recent years, TSMC proposes digital CIM that embeds digital bitwise MAC logic in SRAM [5, 6]. In digital CIM, high efficiency is achieved by integrating compute into memory, while digital in-memory logic guarantees high accuracy by avoiding analog non-ideality. However, the fixed in-memory data path is still a limitation that makes digital CIM only support INT MAC operations.

Reconfigurable digital CIM is a new architecture paradigm that applies reconfigurable computing into digital CIM to achieve high efficiency, accuracy, and flexibility simultaneously. The in-memory reconfigurable logic greatly extends the functional flexibility of digital CIM by dynamically changing the data path for diverse workloads. Based on reconfigurable digital CIM, researchers have developed AI chips for cloud AI applications, Transformer models, and beyond-NN applications [7-10]: ReDCIM flexibly supports INT and FP MAC operations for cloud AI training and inference [7]. TranCIM and MulTCIM use reconfigurable pipeline/parallel modes for accelerating sparse Transformer models [8, 9]. TensorCIM reconfigures its CIM macros for sparse gathering and sparse algebra in beyond-NN applications with a multi-chip-module CIM system architecture [10]. This new architecture paradigm opens up a new dimension for AI chip design, offering unprecedented opportunities for future AI computing.

References

[1] Su, Jian-Wei, et al. “A 28nm 384kb 6T-SRAM Computation-in-Memory Macro with 8b Precision for AI Edge Chips.” 2021 IEEE International Solid-State Circuits Conference (ISSCC). Vol. 64. IEEE, 2021.

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[7] Tu, Fengbin, et al. “A 28nm 29.2TFLOPS/W BF16 and 36.5TOPS/W INT8 Reconfigurable Digital CIM Processor with Unified FP/INT Pipeline and Bitwise

Xun Jiao,
AE for What is

Muhammad Shafique,
AE for What is

Rajsaktish Sankaranarayanan,
AE for Researcher spotlight

Xin Zhao,
AE for Paper submission

Ying Wang,
AE for Technical activities

Jiaqi Zhang,
AE for Technical activities

Paper Deadlines

PACT'23 - Int'l Conference on Parallel Architectures and Compilation Techniques
Vienna, Austria
Deadline: Apr 15, 2023
(Abstracts due: Mar 25, 2023)
Oct 21-25, 2023
http://www.pactconf.org

IWLS'23 - International Workshop on Logic & Synthesis
EPFL, Lausanne, Switzerland
Deadline: Apr 17, 2023
(Abstracts due: Apr 10, 2023)
June 5-6, 2023
https://www.iwls.org

BioCAS'23 – Biomedical Circuits and Systems Conference
Toronto, Canada
Deadline: June 9, 2023
Oct 19-21, 2023
https://2023.ieee-biocas.org/

in-Memory Booth Multiplication for Cloud Deep Learning Acceleration." 2022 IEEE International Solid-State Circuits Conference (ISSCC). Vol. 65. IEEE, 2022.
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[10] Tu, Fengbin, et al. "TensorCIM: A 28nm 3.7nJ/Gather and 8.3TFLOPS/W FP32 Digital-CIM Tensor Processor for MCM-CIM-based Beyond-NN Acceleration." 2022 IEEE International Solid-State Circuits Conference (ISSCC). Vol. 66. IEEE, 2023.

SIGDA Awards

1. Best Paper Award @ FPGA 2023
https://www.isfpga.org/program/

DONGLE: Direct FPGA-Orchestrated NVMe Storage for HLS

Author : Linus Y. Wong, Jialiang Zhang and Jing "Jane" Li (University of Pennsylvania)

2. EDAA Achievement Award 2023 @ DATE 2023
https://www.date-conference.com/

Jason Cong, University of California, Los Angeles

Citation: He served as the chair of the UCLA Computer Science Department from 2005 to 2008. He is the author of more than 500 papers, including 17 Best Paper Awards. Dr. Cong's research publications have close to 35,000 citations, according to Google Scholar, and he is a frequent keynote speaker at major conferences in EDA and design automation.

3. ISPD Lifetime Achievement Award @ ISPD 2022
https://ispd.cc/ispd2023/index.php?page=awards

Malgorzata Marek-Sadowska, University of California, Santa Barbara

Citation: Professor Marek-Sadowska was a member of numerous technical committees, including the Technical Committee of the International Conference on Computer Aided Design, the Technical Committee of the Design Automation Conference, and the Technical Committee of the International Symposium on Physical Design. From 1989 to 1993, she was Associate Editor of IEEE Transactions on Computer-Aided

NOCS'23 – IEEE/ACM Int'l Symposium on Networks-on-Chip (co-located with ESWEEK 2023)
Hamburg, Germany
Deadline: Apr 21, 2023
(Abstracts due: Apr 14, 2023)
Sept 21-22, 2023
https://nocs2023.github.io

MEMOCODE'23 - IEEE/ACM Int'l Conference on Formal Methods and models for System Design (co-located with ESWEEK 2023)
Hamburg, Germany
Deadline: May 5, 2023
(Abstracts due: Apr 28, 2023)
Sept 21-22, 2023
https://memocode2023.github.io

OSCAR'23 - Second Workshop on Open-Source Computer Architecture Research
Orlando, FL (co-located with ISCA 2023)
Abstract deadline: May 5, 2023
June 18, 2023
https://oscar-workshop.github.io/

ICCAD'23 – IEEE/ACM Int'l Conference on Computer-Aided Design
San Francisco, CA
Deadline: May 22, 2023
(Abstracts due: May 15, 2023)
Oct 29 - Nov 2, 2023
http://www.iccad.com

VLSI-SoC'23 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Dubai, UAE
Deadline: May 23, 2023
(Abstracts due: May 16, 2023)
Oct 16-18, 2023
http://www.vlsi-soc.com

HiPC'23 – IEEE Int'l Conference on High Performance Computing, Data, And Analytics
Goa, India

Design of Integrated Circuits and Systems, and from 1993 to 1995, Editor-In- Chief. From 2007 to 2015 she was Associate Editor of IEEE Transactions on VLSI Design of Circuits and Systems.

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems, TODAES, publishes innovative work documenting significant research and development advances on the specification, design, analysis, simulation, testing, and evaluation of electronic systems, emphasizing a computer science/engineering orientation. Design automation for machine learning/AI and machine learning/AI for design automation are very much welcomed.

If you are an active researcher in the design and design automation field and would like to be part of the TODAES review board, please fill out the following reviewer form. TODAES recognizes those reviewers that provide timely and high-quality reviews through the Distinguished Review Board. TODAES also recognizes papers and outstanding junior researchers through best paper and rookie of the year award. Authors can send their paper submissions on the manuscript portal.

TODAES welcomes special issue proposals from leading researchers/practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

Technical Activities

1. The Status of Room-Temperature Quantum Computers

Quantum computers promise to master problems that would take classical computers trillions of years to solve. Standing in the way of broad deployment, however, is that most quantum computer designs depend on cooling the hardware to extreme temperatures—well below –200°C. In recent years, the technology for room-temperature quantum computing has advanced. How close are developers to leveraging these achievements to bring quantum compute power to the desktop, displacing classical computing hardware?

Deadline: July 7, 2023
(Abstracts due: June 30, 2023)
Dec 18-21, 2023
http://www.hipc.org

Upcoming Conferences

ISQED'23 - Int'l Symposium on Quality Electronic Design
San Francisco, CA
April 5-7, 2023
http://www.isqed.org

HOST'23 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
San Jose, CA
May 1-4, 2023
http://www.hostsymposium.org

MDTS'23 – IEEE Microelectronics Design & Test Symposium
Albany, NY
May 8-10, 2023
http://natw.ieee.org

FCCM' 23 - IEEE International Symposium On Field-Programmable Custom Computing Machines
Los Angeles, CA
May 8 - 11, 2023
https://www.fccm.org/

ISCAS'23 – IEEE Int'l Symposium on Circuits and Systems
Monterey, CA
May 21 - 25, 2023
http://iscas2023.org

2. Open RAN, Private 5G Dominate Cellular Industry

At Mobile World Congress 2023 (MWC23), Open RAN and private 5G were two of the biggest topics dictating cellular industry discussion. Technologists involved in hardware and software for telecoms were betting on Open RAN to grab a slice of the 5G market. At the same time, traditional infrastructure providers were not impressed, expressing their continued interest in the lucrative private wireless market…

3. Synopsys Launches Full-Stack, AI-Driven EDA Suite

At its annual Synopsys Users Group (SNUG) Silicon Valley Conference, Synopsys Inc. has launched Synopsys.ai, a suite of AI-driven solutions for the design, verification, testing, and manufacturing of the most advanced digital and analog chips…

4. Codasip Takes Up the Cause of RISC-V Processor Security

RISC-V has gathered considerable momentum in recent years, aided by companies like Google, which has announced its Android mobile operating system's support for the open-source instruction set architecture. Companies are using the architecture for a variety of processing applications, and Codasip, a founding member of RISC-V International, aims to provide customers with tools to develop processor cores tailored to their needs…

Job Positions

1. University of Surrey, UK

Job Title: Professor in Computer Science

Description: We are particularly keen to attract applications in areas including: Data Science, Practical Security, Machine Learning, Data Analytics, Data Engineering, NLP, HCI and Usability, Digital Security and Resilience, Autonomous Systems and Robotics, Complex Systems, and Software Engineering. What we are looking for is: A higher professional qualification, normally a doctoral degree or equivalent; Outstanding qualities and achievements in scholarship and research at a national and international level which have made a significant contribution to the advancement of their subject; Significant academic publication record; Evidence of driving the research agenda, including postgraduate research supervision; Teaching programmes, and/or internationally recognised

RTAS'23 - IEEE Real-Time and Embedded Technology and Applications Symposium
San Antonio, Texas
May 9-12, 2023
http://2023.rtas.org

GLSVLSI'23 – ACM Great Lakes Symposium on VLSI
Knoxville, TN
June 5-7, 2023
http://www.glsvlsi.org

ISVLSI'23 – IEEE Computer Society Annual Symposium on VLSI
Iguana Falls, Brazil
June 20 - 23, 2023
http://www.ieee-isvlsi.org

DAC'23 – Design Automation Conference
San Francisco, CA
July 9-13, 2023
http://www.dac.com/

ICDCS'23 – IEEE Int'l Conference on Distributed Computing Systems
Hong Kong, China
Jul 18 - 21, 2023
https://www.icdcs.org/

ISLPED'23 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
Vienna, Austria
Aug 7-8, 2023
http://www.islped.org

ESWEEK'23 - Embedded Systems Week
Hamburg, Germany
Sept. 17-22, 2023
http://www.esweek.org

textbooks; Evidence of securing a significant amount of sustained research funding; Proven management and leadership qualities at a senior level; Evidence of contributions to conferences, professional meetings and societies at an international level and evidence of achievements in other external activities at an international level; Evidence of high quality teaching at undergraduate and postgraduate level. For more information, please refer to https://jobs.surrey.ac.uk/vacancy.aspx?ref=014523.

2. Royal Institute of Technology School of Electrical Engineering and Computer Science, Sweden

Job Title: Postdocs in Foundations of Data Science

Description: We are looking for 2 postdoctoral researchers in the area of foundations of data science. The positions are in a research team in KTH led by professor Aristides Gionis (https://www.kth.se/profile/argioni/). The research team focuses on developing novel methods to extract knowledge from data, modeling large-scale complex systems, and exploring new application areas in data science. Areas of interest include but are not limited to models and algorithms for knowledge discovery, novel algorithmic and statistical techniques for big data management, optimization for machine learning, analysis of information and social networks, fairness, accountability, and transparency in learning systems. Applicants must have a strong interest in the development of the underlying theory, applications, and methods to distill knowledge from large complex datasets. The advertised positions are funded by Wallenberg AI, Autonomous Systems and Software Program (WASP), Sweden's largest individual research program, and by an ambitious 5-year European Research Council (ERC) Advanced Grant titled REBOUND, which aims to study the phenomena of polarization and echo chambers in online media, and develop methods to mitigate these phenomena. Funding is also provided by H2020 European project SoBigData++. The postdoc positions involve individual and collaborative research, participation in research projects, and interaction with faculty, postdocs, and students. Opportunities to enhance important skills, such as research leadership, teaching, and grant-proposal writing, will also be given. For more information, please refer to https://facultyvacancies.com/post-doc-in-foundations-of-data-science,i33411.html.

3. Harvard University, US

Job Title: Postdoctoral Fellow in Resilient Multi-Robot Systems

Description: Postdoctoral fellow will conduct research in multi-agent coordination with a particular focus on cases where malicious agents in the network disrupt optimal or nominal coordination between agents. We are interested in developing the theory and accompanying analysis to characterize and mitigate the impact of adversarial agents on multi-agent coordination schemes. Some particular areas of interest are consensus

systems, distributed optimization (and federated learning), and game theory. Postdoctoral fellow will be expected to publish results in top tier control and robotics journals (such as but not limited to, Transactions on Automatic Control, Automatica, Transactions on Robotics, International Journal on Robotics Research, and Science Robotics), mentor and collaborate with PhD students in the lab, and contribute to related research proposals. Developed algorithms and derived results may be deployed and validated on actual multi-robot system platforms in the REACT Lab. For more information, please refer to https://academicpositions.harvard.edu/postings/12307.

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