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SIGDA - The Resource for EDA Professionals

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SIGDA News

1. Apple, AMD Back TSMC's Tripled Investment, Tech Upgrade in Arizona

Taiwan Semiconductor Manufacturing Co. (TSMC) has more than tripled its overall investment in Arizona to about $40 billion for two chip facilities with the support of customers like Apple and AMD, stoking a U.S. effort to revive domestic chip production.

2. Nvidia Shows Off Hopper MLPerf Training Benchmarks

In the MLPerf training round, Nvidia exhibited training benchmarks for its new H100 GPU for the first time. There were also strong results from Intel, Habana Labs, and MosaicML in this latest round, but nothing from Nvidia challengers Graphcore or Google.

3. U.S. Blacklists YMTC, 21 Chinese Companies on AI Threat

The U.S. Commerce Department is blacklisting Yangtze Memory Technologies Co. (YMTC) and more than 20 other Chinese chipmakers suspected of an AI threat to U.S. national security.

4. YMTC's Lead Over Samsung, Micron in 3D NAND Challenged

The new lead of China's Yangtze Memory Technologies Co. (YMTC) over larger rivals like Samsung and Micron with the world's first 200-layer–plus 3D NAND flash is likely to crumble, according to industry analysts.

Messages from the EiCs

Dear ACM/SIGDA members,

Wish you a very happy new year 2023! We are excited to present to you the January E-Newsletter and encourage you to invite your students and colleagues to be a part of the SIGDA newsletter.

The newsletter covers a wide range of information from the upcoming conferences to technical news and activities of our community. Get involved and contact us if you want to contribute articles or announcements.

The newsletter is evolving. Please let us know what you think.

Happy reading!

Debjit Sinha, Keni Qiu,
Editors-in-Chief,
SIGDA E-News

5. 10 Years After Start, FHE in Commercial Use

The flexible hybrid electronics (FHE) industry is less than 10 years old, and there are commercial products on the market in health care, wearables and medical diagnostics. GE, for example, has announced several FHE-containing products in health care and medical diagnostics.

6. Synaptics CEO Aims for AI on Edge Devices

Synaptics CEO Michael Hurlston rescued the chip designer from the collapse of a billion-dollar–plus business when it lost Apple as a customer a few years ago. Now, Synaptics has assembled a new tech portfolio aimed at design wins that add AI to edge IoT devices.

7. National Ignition Facility Hits Fusion Milestone

The results of the discovery at the U.S. National Ignition Facility (NIF) of the Lawrence Livermore National Laboratory (LLNL) in California, conducted on Dec. 5, were announced a few days ago by the administration of U.S. President Joe Biden. That research aims to harness nuclear fusion—the phenomenon that powers the sun—to provide an almost unlimited source of clean energy on Earth.

8. Flexible Cryogenic Cables Simplify Quantum Computer Design

Delft Circuits announced its inclusion in the BICEP project in Antarctica, supporting NASA's Jet Propulsion Laboratory (JPL) at the California Institute of Technology and other project partners. The team at JPL determined that advanced cables made by Delft Circuits will be installed in the telescope's cryostat, as part of its new camera.

What is a CGRA?

Henk Corporaal(1) & Barry de Bruin(1,2)

(1) Eindhoven University of Technology

(2) Tampere University

Certainly, many of us heard about Coarse-Grained Reconfigurable Arrays (CGRA). They are flexible and highly parallel processing platforms, used for a wide variety of computing tasks where energy-efficiency is a primary concern. Various CGRA variations have been proposed for several decades [1]. Although most efforts remain research platforms, there have been commercial products which include a CGRA, such as an audio processor in

a Samsung mobile System-on-Chip (SoC) [2], a flexible accelerator for embedded multimedia applications [3], and a SoC for large-scale acceleration of deep learning workloads [4].

What distinguishes CGRAs from other computing platforms like FPGAs, CPUs, GPUs, and DSPs? A precise definition turns out to be rather difficult. Let's look at the keywords: 'coarse grain', 'reconfigurable', and 'array'. The array aspect is easy to understand; a CGRA consists of a grid (array) of processing elements (PEs) that are interconnected through a configurable switching fabric, or network-on-chip (NoC). However, what about coarse grain and reconfigurable? Most processors are coarse grain (having 'big' units); even FPGAs, typically supporting fine grain (single bit-level) configuration, are adding coarse grain units like DSPs, and recently even complete SIMD units (e.g., in the Xilinx Versal architectures [12]). Most processors are in fact highly reconfigurable; e.g., a CPU can change the performed operations every cycle! Of course, this is not the most energy efficient; flexibility has its price!

A recent survey proposed a CGRA classification based on the temporal and spatial reconfiguration granularity [1]. The temporal granularity specifies how often the CGRA reconfigures, while the spatial granularity specifies the minimum unit of reconfiguration. The authors propose that part of the CGRA should remain static for at least a part of a program (e.g., a loop-nest or kernel), which excludes CPUs that exploit cycle-level reconfiguration, and that the spatial granularity should be well above the bit-level of an FPGA, i.e., the minimum unit of reconfiguration could be the arithmetic or memory operation of PEs.

Many proposed CGRAs fit into this classification. One recent architecture is the IPA CGRA [10], which consists of a homogeneous grid of programmable PEs and a static torus network that can pass data to neighboring PEs. Every PE essentially operates as a small independent RISC core, and has its own instruction memory and decoding stage, ALU and register file. Some PEs have a load-store unit to access the memory that is shared with the host core. The IPA CGRA operates standalone and accelerates complete kernels, including required control flow. Another interesting CGRA is Blocks [6], which consists of a heterogeneous grid of programmable PEs and a static reconfigurable instruction and data network. On top of exploiting Instruction-Level-Parallelism (ILP), its instruction network allows the CGRA to combine multiple PEs into a virtual SIMD-unit to exploit data-level parallelism (DLP). The Blocks CGRA operates standalone and accelerates different kernels between every reconfiguration sequence, as was demonstrated in [8] for a seizure detection application, by 24/7 EEG analysis.

Xun Jiao,
AE for What is

Muhammad Shafique,
AE for What is

Rajsaktish Sankaranarayanan,
AE for Researcher spotlight

Xin Zhao,
AE for Paper submission

Ying Wang,
AE for Technical activities

Paper Deadlines

HOST'23 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
San Jose, CA
Deadline: Jan 16, 2023 (Winter Submission, Abstracts due: Jan 9, 2023)
May 1-4, 2023
http://www.hostsymposium.org

DAC'23 – Design Automation Conference
San Francisco, CA
Engineering Tracks Deadline: Jan. 17, 2023
July 9-13, 2023
http://www.dac.com/

FCCM' 23 - IEEE International Symposium On Field-Programmable Custom Computing Machines
Los Angeles, CA
Deadline: Jan 16, 2023
(Abstracts due: Jan 9, 2023)
TBD
https://www.fccm.org/

CGRAs have several advantages: 1) They are highly parallel (containing many units), supporting parallelism at various levels (data-, instruction-/operation- and often even task-level). 2) They have a high area efficiency, due to its coarseness (as compared to e.g., FPGAs); 3) Energy efficiency is also good, due to spatial computation using static configuration of the communication; also, the computation itself can often be statically mapped. 4) Finally, they are very flexible, supporting all kinds of computation (unless they are very specialized for a certain domain). This wide applicability gives them the potential advantage of high-volume production with resulting low cost.

Note that a quantitative definition of flexibility does not exist, and scientists often disagree. E.g., some find FPGAs extremely flexible, since they can be reconfigured to implement any hardware, while others find them far less flexible due to their large overhead (in area, delay and energy). [11] provides an in-depth discussion and proposes a first quantitative definition of flexibility of processing platforms, including CPUs, GPUs and FPGAs. You may be surprised to read where they end up on the scale of flexibility.

CGRAs also have major challenges: 1) Typically, the switching fabric is expensive. Here we can learn from FPGA interconnect, with e.g., short and long wires, and avoiding full crossbar switchboxes. 2) Another challenge is to determine the right architecture for CGRAs. Some recent efforts focus on automated design-space-exploration (DSE) to find a good CGRA architecture for a given set of applications [7]. 3) Perhaps the biggest challenge in CGRA research has been to find a suitable programming model and accompanying highly optimizing compiler for application acceleration while exploiting all hardware features of the CGRA. One well-explored, although restricted, approach is to map a static dataflow graph to the CGRA, while executing the application control flow on a tightly coupled host processor [9]. Another promising approach is to model the CGRA as an exposed data-path architecture (EDPA) to reuse existing compiler developments for VLIW/TTA processors [5]. All these areas require further research.

In summary, CGRAs are extremely interesting, with high potential. Providing good solutions for above challenges, in particular excellent programming support, they can become the flexible and energy efficient processing 'workhorse' of the near future.

References

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ICDCS'23 – IEEE Int'l Conference on Distributed Computing Systems
Hong Kong, China
Deadline: Jan 21, 2023
(Abstracts due: Jan 14, 2023)
Jul 18 - 21, 2023
https://www.icdcs.org/

GLSVLSI'23 – ACM Great Lakes Symposium on VLSI
Knoxville, TN
Deadline: Feb. 6, 2023
June 5-7, 2023
http://www.glsvlsi.org

ISVLSI'23 – IEEE Computer Society Annual Symposium on VLSI
Iguana Falls, Brazil
Deadline: Feb 23, 2023
June 20 - 23, 2023
http://www.ieee-isvlsi.org

MDTS'23 – IEEE Microelectronics Design & Test Symposium
Albany, NY
Deadline: Feb 26, 2023
Tentative Date: May 8-10, 2023
http://natw.ieee.org

ISLPED'23 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
Vienna, Austria
Deadline: March 13, 2023
(Abstracts due: March 6, 2023)
Aug 7-8, 2023
http://www.islped.org

ESWEEK'23 - Embedded System Week
Hamburg, Germany
Deadline: March 23, 2023
(Abstracts due: March 16, 2023)
September 17-22, 2023
http://esweek.org

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An update in: Mark Wijtvliet, Henk Corporaal and Akash Kumar, CGRAs and Related Work, chapter in Blocks, Towards Energy-efficient, Coarse-grained Reconfigurable Architectures, Springer, June 2021.

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IWLS'23 - International Workshop on Logic & Synthesis
EPFL, Lausanne, Switzerland
Deadline: April 10, 2023
(Abstracts due: April 3, 2023)
June 5-6, 2023
https://www.iwls.org

Upcoming Conferences

VLSID'23 – International Conference on VLSI Design & International Conference on Embedded Systems
Novotel, HICC, Hyderabad
Jan 8 - 12, 2023
http://embeddedandvlsidesignconference.org/

ASP-DAC'23 - Asia and South Pacific Design Automation Conference
Miraikan, Tokyo, Japan
Jan 16-19, 2023
http://www.aspdac.com

HiPEAC'23: Int'l Conference on High Performance Embedded Architectures & Compilers
Toulouse, France
Jan 16-18, 2022
https://www.hipeac.net/2023/toulouse/

FPGA’23 – ACM/SIGDA Int’l Symposium on Field-Programmable Gate Arrays
Monterey, CA
Feb 12 - 14, 2023
http://www.isfpga.org

SIGDA Awards

1. **ACM/IEEE A. Richard Newton Technical Impact Award in Electronic Design Automation @ 2022**

https://www.sigda.org/awards/newton/

Ricardo Telichevesky, Kenneth S. Kundert, and Jacob K. White, "Efficient Steady-State Analysis based on Matrix-Free Krylov-Subspace Methods", In Proc. of the 32nd Design Automation Conference, 1995.

2. **ACM Outstanding Ph.D. Dissertation Award in Electronic Design Automation @ 2022**

https://www.sigda.org/awards/opda/

Ganapati Bhat, for the dissertation "Design, Optimization, and Applications of Wearable IoT Devices", Arizona State University, Advisor: Umit Y. Ogras

3. **SIGDA Outstanding New Faculty Award @ 2022**

https://www.sigda.org/awards/onfa/

Yingyan (Celine) Lin, Rice University

SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems, TODAES, publishes innovative work documenting significant research and development advances on the specification, design, analysis, simulation, testing, and evaluation of electronic systems, emphasizing a computer science/engineering orientation. Design automation for machine learning/AI and machine learning/AI for design automation are very much welcomed.

If you are an active researcher in the design and design automation field and would like to be part of the TODAES review board, please fill out the following reviewer form. TODAES recognizes those reviewers that provide

ISSCC'23 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Feb 19-23, 2023
http://isscc.org

DATE'23 - Design Automation and Test in Europe
Antwerp, Belgium
Mar 17-19, 2023
http://www.date-conference.com

ISPD'23 – ACM Int'l Symposium on Physical Design
Virtual Conference
Mar 26 - 29, 2023
http://www.ispd.cc

ISQED'23 - Int'l Symposium on Quality Electronic Design
San Francisco, CA
April 5-7, 2023
http://www.isqed.org

ISCAS'23 – IEEE Int'l Symposium on Circuits and Systems
Monterey, CA
May 21 - 25, 2023
http://iscas2023.org

RTAS'23 - IEEE Real-Time and Embedded Technology and Applications Symposium
San Antonio, Texas
May 9-12, 2023
http://2023.rtas.org

timely and high-quality reviews through the Distinguished Review Board. TODAES also recognizes papers and outstanding junior researchers through best paper and rookie of the year award. Authors can send their paper submissions on the manuscript portal.

TODAES welcomes special issue proposals from leading researchers/practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

MOST DOWNLOADED PAPERS OF 2022

Here are the top 5 most downloaded paper for TODAES 2022

- Han Cai, Ji Lin, Yujun Lin, Zhijian Liu, Haotian Tang, Hanrui Wang, Ligeng Zhu, and Song Han. 2022. **Enable Deep Learning on Mobile Devices: Methods, Systems, and Applications**. ACM Trans. Des. Autom. Electron. Syst. 27, 3, Article 20 (May 2022), 50 pages. https://doi.org/10.1145/3486618
- Atefeh Sohrabizadeh, Cody Hao Yu, Min Gao, and Jason Cong. 2022. **AutoDSE: Enabling Software Programmers to Design Efficient FPGA Accelerators**. ACM Trans. Des. Autom. Electron. Syst. 27, 4, Article 32 (July 2022), 27 pages. https://doi.org/10.1145/3494534
- Sunjung Lee, Jaewan Choi, Wonkyung Jung, Byeongho Kim, Jaehyun Park, Hweesoo Kim, and Jung Ho Ahn. 2022. **MVP: An Efficient CNN Accelerator with Matrix, Vector, and Processing-Near-Memory Units**. ACM Trans. Des. Autom. Electron. Syst. 27, 5, Article 42 (September 2022), 25 pages. https://doi.org/10.1145/3497745
- Quentin Gautier, Alric Althoff, Christopher L. Crutchfield, and Ryan Kastner. 2022. **Sherlock: A Multi-Objective Design Space Exploration Framework**. ACM Trans. Des. Autom. Electron. Syst. 27, 4, Article 33 (July 2022), 20 pages. https://doi.org/10.1145/3511472
- Monzurul Islam Dewan and Dae Hyun Kim. 2022. **Design Automation Algorithms for the NP-Separate VLSI Design Methodology**. ACM Trans. Des. Autom. Electron. Syst. 27, 5, Article 53 (September 2022), 20 pages. https://doi.org/10.1145/3508375

CALL FOR PAPERS

TODAES welcomes submission on Special Issue on Design for Testability and Reliability of Security-Aware Hardware. Topics of interest include, but are not limited to the following:

- Functional Testing for Security-Aware Hardware

- Design Time Testing of Hardware-Intrinsic Security Primitives
- Security in Scan Testing
- Testing for PUF Resistant to Machine Learning Attacks
- Environmental Variation Tolerance in PUF and TRNG
- Aging-Resistance of Hardware-Intrinsic Security Primitives
- Early-Stage Design for Testability and Reliability for Security-awareness

Deadline: **15 February 2023**.
Tentative Publication Date: August 2023.

CALL FOR NOMINATIONS: BEST PAPER AWARD

ACM Transactions on Design Automation of Electronic Systems (TODAES) is seeking nominations for the **2023 TODAES Best Paper Award**. The nomination **deadline is February 15, 2023**. All papers published in the ACM TODAES between January 2022 and December 2022 are eligible. The best paper will be selected based on originality, timeliness, potential impact and overall quality. Submit the nominations using this link: https://forms.gle/8NWbmTTNCW97DeKf6

CALL FOR NOMINATIONS: ROOKIE OF THE YEAR AWARD

ACM Transactions on Design Automation of Electronic Systems (TODAES) introduced a new award in 2022, i.e., **the TODAES Rookie Author of the Year (RAY) Award**. This newly introduced award aims to highlight the achievement of junior researchers in the Design and Design Automation of Electronic Systems field. Specifically, the award recognizes an author whose first-ever peer-reviewed journal paper as a lead author is published in ACM TODAES.

The lead author of a paper refers to the author who contributed the most to the submission. Since people may adopt different ways to order the authors, any nomination for the RAY Award must make it clear that the nominee is the lead author. If two authors satisfy this requirement (meaning they made equal contributions and are both rookie authors), both can receive the RAY award.

The nomination deadline is February 15, 2023. All papers published in the ACM TODAES between January 2022 and December 2022 are eligible. The RAY award will be selected based on originality, timeliness, potential impact, and overall quality. Submit the nominations using this link: https://forms.gle/wd6xGMSEgZmT1SSP8

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