



## Special Interest Group on Design Automation **ACM/SIGDA E-NEWSLETTER**, Vol. 53, No. 2

### **SIGDA - The Resource for EDA Professionals**

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# SIGDA News

### **1. [Exploring the Industrial Relevance of QNLP](#)**

One of the most demanding—yet fascinating—challenges that researchers, scientists and academics are facing is understanding the mathematics of language. In this context, the discipline that deals with defining and applying models and tools to the treatment of natural language is called computational linguistics (CL). By nature, CL is interdisciplinary, as it combines methods and techniques of linguistics with those of computer science, artificial intelligence (AI) and statistics.

### **2. [Micron Pushes DRAM Node for Mobile First](#)**

Micron Technology has been setting the pace for DRAM advancement of late. Its 1-beta DRAM technology continues the trend, but other major vendors are keeping up, even as it looks like DRAM prices will be lower in 2023.

### **3. [Samsung, Micron Battle for NAND Supremacy](#)**

The memory industry has always gone through a predictable boom-and-bust cycle, but the pandemic and geopolitical instability has introduced new twists to the market over the course of 2022, and uncertainty will continue to play a role in 2023.

### **4. [AV Radar Moves to Domain Controller for First Time](#)**

At CES 2023, Ambarella demonstrated its centralized architecture for radar processing in autonomous vehicles (AVs), which allows fewer radar sensors to be used in each AV. Ambarella's offering is a combination of its

# Messages from the EiCs

Dear ACM/SIGDA members,

We are excited to present to you February E-Newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter.

The newsletter covers a wide range of information from the upcoming conferences to technical news and activities of our community. Get involved and contact us if you want to contribute articles or announcements.

The newsletter is evolving. Please let us know what you think.

Happy reading!

*Debjit Sinha, Keni Qiu,*  
Editors-in-Chief,  
SIGDA E-News

CV3 family of domain controller chips with AI algorithms and software from Oculii, which Ambarella acquired in 2021.

#### 5. [Experts: U.S. Military Chip Supply Is Dangerously Low](#)

The U.S. Department of Defense (DoD) will probably take years to wean itself from Asian chip supplies because of a dearth of investments in domestic production capacity, according to industry insiders and government observers.

# What is

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## What is Hyperdimensional Computing?

The human brain remains the most sophisticated processing component that has ever existed. The ever-growing research in biological vision, cognitive psychology, and neuroscience has given rise to many concepts that have led to prolific advancement in artificial intelligent accomplishing cognitive task. HyperDimensional (HD) Computing is introduced as an alternative paradigm that mimics important brain functionalities towards high-efficiency and noise-tolerant computation [1]. HD computing is motivated by the observation that the human brain operates on high-dimensional data representations. In HD computing, objects are thereby encoded with high-dimensional vectors, called hypervectors, which have thousands of elements [2, 3]. HD computing incorporates learning capability along with typical memory functions of storing/loading information. It mimics important functionalities of the human memory model with vector operations, which are computationally tractable and mathematically rigorous in describing human cognition [4, 5]. HD computing relies on the algebraic properties of their key operations to incorporate the advantages of structured symbolic and vector distributed representations. It operates over a well-defined and hardware-friendly set of mathematics: Binding is well suited for associating two hypervectors and used for variable-value association. Bundling is a memorization function that keeps the information of input data into a bundled vector. Permutation is an operation to represent sequences by creating a near-orthogonal but reversible hypervector. Reasoning is done by measuring the similarity of hypervectors.

HD computing has shown several advantages as the next generation of cognitive machines. First, its training capability in one or few shots, where

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partial data are learned from one or few examples as opposed to many iterations [6, 7]. Second, HD operations are highly parallel and do not require frequent weight updates, thus empowering online learning on processing in-memory [8]. Third, HD computing has natural robustness to noise and bit errors provided by the high-dimensional distributed representations. This enables greater tolerance for device variability and unreliable emerging technologies, such as non-volatile memory or nanoscale devices with low signal-to-noise ratio [8-10]. Finally, HD computing has been shown great potential to enable lightweight privacy and security [11-14].

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**Muhammad Shafique,**

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AE for Researcher spotlight

**Xin Zhao,**

AE for Paper submission

**Ying Wang,**

AE for Technical activities

**Jiaqi Zhang,**

AE for Technical activities

# Paper Deadlines

## **GLSVLSI'23 – ACM Great Lakes Symposium on VLSI**

Knoxville, TN

Deadline: Feb. 6, 2023

June 5-7, 2023

<http://www.glsvlsi.org>

## **ISVLSI'23 – IEEE Computer Society Annual Symposium on VLSI**

Iguana Falls, Brazil

Deadline: Feb 23, 2023

June 20 - 23, 2023

<http://www.ieee-isvlsi.org>

## **MDTS'23 – IEEE Microelectronics Design & Test Symposium**

Albany, NY

Deadline: Feb 26, 2023

Tentative Date: May 8-10, 2023

<http://natw.ieee.org>

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# SIGDA Awards

## 1. IEEE Gustav Robert Kirchhoff Award @ ASP-DAC 2023

**28th Asia and South Pacific Design Automation Conference (ASP-DAC 2023) ([aspdac.com](http://aspdac.com))**

**Yoshisuke Ueda**

## 2. Best Paper Award @ ASP-DAC 2023

**ASP-DAC 2023 Technical Program ([tsys.jp](http://tsys.jp))**

**2C-2: Approximate Floating-Point FFT Design with Wide Precision-Range and High Energy Efficiency**

**Author: Chenyi Wen, Ying Wu, Xunzhao Yin, Cheng Zhuo (Zhejiang Univ., China)**

**3D-1: Rethink before Releasing your Model: ML Model Extraction Attack in EDA**

**Author: Chen-Chia Chang, Jingyu Pan (Duke Univ., USA), Zhiyao Xie (Hong Kong Univ. of Science and Tech., Hong Kong), Jiang Hu (Texas A&M Univ., USA), Yiran Chen (Duke Univ., USA)**

## **ISLPED'23 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design**

Vienna, Austria

Deadline: March 13, 2023

(Abstracts due: March 6, 2023)

Aug 7-8, 2023

<http://www.islped.org>

## **ESWEEK'23 - Embedded Systems Week**

Hamburg, Germany

Deadline: March 23, 2023

(Abstracts due: March 16, 2023)

Sept. 17-22, 2023

<http://www.esweek.org>

## **IWLS'23 - International Workshop on Logic & Synthesis**

EPFL, Lausanne, Switzerland

Deadline: April 10, 2023

(Abstracts due: April 3, 2023)

June 5-6, 2023

<https://www.iwls.org>

## **ICCAD'23 – IEEE/ACM Int'l Conference on Computer-Aided Design**

San Francisco, CA

Deadline: May 22, 2023

(Abstracts due: May 15, 2023)

Oct 29 - Nov 2, 2023

<http://www.iccad.com>

## **VLSI-SoC'23 – IFIP/IEEE Int'l Conference on Very Large Scale Integration**

Dubai, UAE

Deadline: May 23, 2023

(Abstracts due: May 16, 2023)

Oct 16-18, 2023

<http://www.vlsi-soc.com>

### 3. Special Feature Award @ ASP-DAC 2023

#### [ASP-DAC 2023 Technical Program \(tsys.jp\)](#)

##### **2E-1 : ViraEye: An Energy-Efficient Stereo Vision Accelerator with Binary Neural Network in 55 nm CMOS**

**Author :** Yu Zhang, Gang Chen, Tao He, Qian Huang, Kai Huang  
(Sun Yat-sen Univ., China)

### 4. Best Design Award @ ASP-DAC 2023

#### [ASP-DAC 2023 Technical Program \(tsys.jp\)](#)

##### **2E-5 : A fully synchronous digital LDO with built-in adaptive frequency modulation and implicit dead-zone control**

**Author :** Shun Yamaguchi, Mahfuzul Islam, Takashi Hisakado, Osami Wada (Kyoto Univ., Japan)

## Who's Who



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## Upcoming Conferences

### **FPGA'23 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays**

Monterey, CA  
Feb 12 - 14, 2023  
<http://www.isfpga.org>

### **ISSCC'23 – IEEE Int'l Solid-State Circuits Conference**

San Francisco, CA  
Feb 19-23, 2023  
<http://isscc.org>

### **DATE'23 - Design Automation and Test in Europe**

Antwerp, Belgium  
Mar 17-19, 2023  
<http://www.date-conference.com>

### **ISPD'23 – ACM Int'l Symposium on Physical Design**

Virtual Conference  
Mar 26 - 29, 2023  
<http://www.ispd.cc>

### **ISQED'23 - Int'l Symposium on Quality Electronic Design**

San Francisco, CA  
April 5-7, 2023  
<http://www.isqed.org>

### **HOST'23 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust**

San Jose, CA  
May 1-4, 2023  
<http://www.hostsymposium.org>

### **FCCM' 23 - IEEE International Symposium On Field-Programmable Custom Computing Machines**

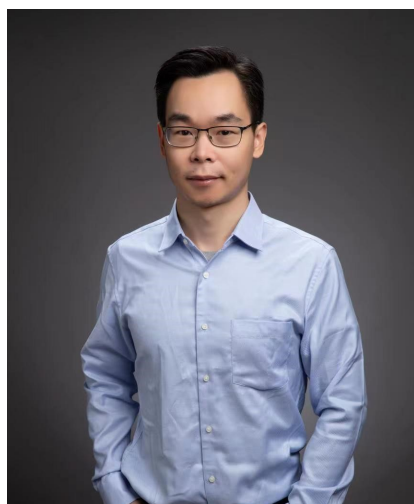
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Los Angeles, CA

May 8 - 11, 2023

<https://www.fccm.org/>

**ISCAS'23 – IEEE Int'l Symposium on Circuits and Systems**

Monterey, CA

May 21 - 25, 2023

<http://iscas2023.org>

**RTAS'23 - IEEE Real-Time and Embedded Technology and Applications Symposium**

San Antonio, Texas

May 9-12, 2023

<http://2023.rtas.org>

**DAC'23 – Design Automation Conference**

San Francisco, CA

July 9-13, 2023

<http://www.dac.com/>

**ICDCS'23 – IEEE Int'l Conference on Distributed Computing Systems**

Hong Kong, China

Jul 18 - 21, 2023

<https://www.icdcs.org/>

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