



Special Interest Group on Design Automation ACM/SIGDA E-NEWSLETTER, Vol. 52, No.11

SIGDA - The Resource for EDA Professionals

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SIGDA News

1. How the CHIPS Act Will Impact Engineers

The \$52 billion spending plan outlined in the CHIPS and Science Act that has been signed into law has significant implications for the semiconductor ecosystem—from chip manufacturers to engineers and production teams.

2. TSMC Cuts Expansion Plan to \$36B as Outlook Sours

Taiwan Semiconductor Manufacturing Co. (TSMC) is cutting its 2022 capacity expansion budget to \$36 billion from the original \$40 billion announced in July, as outlook for demand from smartphone and other consumer electronics makers dims.

3. Samsung Roadmap Includes 1.4-nm Production by 2027

Samsung Electronics is planning for 1.4-nm production by 2027, according to a roadmap it publicized for its chip foundry business. The company is raising the ante with top rival Taiwan Semiconductor Manufacturing Co. (TSMC) as demand for advanced semiconductors has soared.

4. Intel Foundry's 'No. 1' Customer—U.S. DoD—Targets GAA

The U.S. Department of Defense (DoD) is Intel Foundry Services' (IFS's) "No. 1" customer. IFS plans to be part of the DoD state-of-the-art heterogeneous integrated packaging (SHIP) program. That program will necessitate deep knowledge of gate-all-around (GAA) technology facilitating high-transistor-density 3D chips.

Messages from the EiCs

Dear ACM/SIGDA members,

We are excited to present to you November E-Newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter.

The newsletter covers a wide range of information from the upcoming conferences to technical news and activities of our community. Get involved and contact us if you want to contribute articles or announcements.

The newsletter is evolving. Please let us know what you think.

Happy reading!

Debjit Sinha, Keni Qiu, Editors-in-Chief, SIGDA E-News

5. Nvidia DPU Tackles Zero Trust

The remote-work era spawned by the pandemic shone a light on the need for robust security when endpoints exponentially proliferate and workloads become more distributed. Nvidia's latest data processing unit (DPU) reflects that these distributed-computing environments are here to stay—and that hardware has a key role to play in implementing zero-trust security, whether it's in the data center or at the edge.

6. <u>Direct Satellite-to-Mobile Services Emerge</u>

Apple and T-Mobile are separately rolling out schemes with Globalstar and SpaceX, respectively, to enable customers to connect to signals delivered from space. Amazon is preparing for multiple launches of its low earth orbit (LEO) Project Kuiper satellite constellation.

What is

What is Hardware Trust Verification?

Contributing author: Prabhat Mishra

Professor, Department of Computer & Information Science & Engineering, University of Florida

Design of secure systems rely on the hardware root-of-trust. While there are many design-for-security solutions (such as encryption, authentication, obfuscation, etc.), securing hardware is still difficult in the face of supply chain vulnerabilities [1]. Specifically, growing reliance on third-party hardware modules, severely affects the security and trustworthiness of computing platforms. These third-party IPs may come with deliberate malicious implants (e.g., hardware Trojan), undocumented test/debug interfaces working as hidden backdoors, or other integrity issues. Therefore, it is critical to verify that the hardware is trustworthy before deployment.

There are three major components in hardware trust verification: (i) threat model, (ii) trust metrics and benchmarks, and (iii) trust verification techniques [2]. While functional verification checks for expected behaviors based on error (bug) models, hardware trust verification needs to check for anomalies based on specific threat (vulnerability) models. There are a wide variety of vulnerabilities that an attacker can exploit, including hardware Trojans, information leakage, illegal states and transitions, permissions and privileges, fault injection, and side-channel

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AE for Awards

vulnerabilities. The metrics and benchmarks are crucial to evaluate the quality of the trust verification methods. It is expected that the metrics will have a natural alignment with the vulnerabilities. For example, we need to have hardware Trojan coverage metric corresponding to malicious implants vulnerability [3]. Similarly, the Trust-Hub website provides diverse hardware Trojan benchmarks. There are also tools that can provide dynamic benchmarks by inserting the required number and types of hardware Trojans in a design [4].

Hardware security verification techniques can be broadly divided into four categories: (i) formal verification, (ii) simulation-based security validation, (iii) side-channel analysis, and (iv) machine learning. If you have a golden specification (e.g., RTL design), you can perform equivalence checking to ensure that the implementation (e.g., gate-level design) is trustworthy [5]. Similarly, we can define specific security properties (assertions) and perform property checking or assertion-based validation on the target implementation [6]. When formal verification fails due to state-space explosion, we can rely on efficient test generation methods to activate specific vulnerabilities or improve the specific trust metrics [7,8]. While simulation-based security validation compares functional outputs, side-channel analysis compares side-channel signatures, such as dynamic power, path delay, and electromagnetic emanation [9]. Finally, machine learning based solutions are useful when we want to verify known as well as unknown vulnerabilities without a golden specification [10].

References

- [1] Prabhat Mishra, Swarup Bhunia and Mark Tehranipoor (Editors), Hardware IP Security and Trust, ISBN: 978-3-319-49024-3, Springer, 2017.
- [2] Farimah Farahmandi, Yuanwen Huang and Prabhat Mishra, System-on-Chip Security Validation and Verification, ISBN: 978-3-030-30596-3, Springer, 2019.
- [3] Jonathan Cruz, Prabhat Mishra and Swarup Bhunia, The Metric Matters: The Art of Measuring Trust in Electronics, Design Automation Conference (DAC), 2019.
- [4] Jonathan Cruz, Yuanwen Huang, Prabhat Mishra and Swarup Bhunia, An Automated Configurable Trojan Insertion Framework for Dynamic Trust Benchmarks, Design Automation and Test in Europe (DATE), pages 1598-1603, 2018.
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- [6] Hasini Witharana, Aruna Jayasena, Andrew Whigham and Prabhat Mishra, Automated Generation of Security Assertions for RTL Models, ACM Journal on Emerging Technologies in Computing Systems, 2022.
- [7] Yangdi Lyu and Prabhat Mishra, Scalable Concolic Testing of RTL Models, IEEE Transactions on Computers, 70(7), pages 979-991, 2021.
- [8] Yangdi Lyu and Prabhat Mishra, Scalable Activation of Rare Triggers in Hardware Trojans by Repeated Maximal Clique Sampling, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 40(7), pages 1287-1300, 2021.

Xun Jiao.

AE for What is

Muhammad Shafique,

AE for What is

Rajsaktish Sankaranarayanan,

AE for Researcher spotlight

Xin Zhao,

AE for Paper submission

Ying Wang,

AE for Technical activities

Upcoming Conferences

ISQED'23 - Int'l Symposium on Quality Electronic Design

San Francisco, CA Deadline: Nov 11, 2022 April 5-7, 2023 http://www.isqed.org

HOST'23 – IEEE Int'l Symposium on Hardware-Oriented Security

San Jose, CA

and Trust

Deadline: Oct 17, 2022 (Fall Submission), Jan 16, 2023 (Winter Submission)

May 1-4, 2023

http://www.hostsymposium.org

DAC'23 – Design Automation Conference

San Francisco, CA Research Paper Deadline: Nov. 21, 2022 (Abstracts due: Nov. 14, 2022) Engineering Tracks Deadline: Jan. 17, 2023 July 19-13, 2023

http://www.dac.com/

FCCM' 23 - IEEE International Symposium On

[9] Yuanwen Huang, Swarup Bhunia and Prabhat Mishra, Scalable Test Generation for Trojan Detection using Side Channel Analysis, IEEE Transactions on Information Forensics & Security, 13(11), pages 2746-2760, May 2018.

[10] Zhixin Pan and Prabhat Mishra, A Survey on Hardware Vulnerability Analysis using Machine Learning, IEEE Access, Volume 10, pages 49508 – 49527, 2022.

SIGDA Awards

1. Test-of-Time Award @ ESWEEK 2022 https://esweek.org/awards/

- CASES: Scalable Custom Instructions Identification for Instruction-set Extensible Processors (2004)
 Advisor: Pan Yu and Tulika Mitra, National University of Singapore
- CODES+ISSS: A Framework for Rapid System-level Exploration, Synthesis, and Programming of Multimedia MP-SoCs (2007) Advisor: Mark Thompson, Hristo Nikolov, Todor Stefanov, Andy D. Pimentel, Cagkan Erbas, Simon Polstra, and Ed. F. Deprettere, University of Amsterdam and Leiden University, NL
- EMSOFT: Real-time Interfaces for Composing Real-time Systems (2006)
 Advisor: Lether Thiolo, Ernocto Wandeler, and Nikeley Steimeney

Advisor: Lothar Thiele, Ernesto Wandeler, and Nikolay Stoimenov, ETH Zurich, CH

2. IEEE CEDA Service Award @ ESWEEK 2022

https://www.youtube.com/watch?v=su7wPNJquhE

Prof. Andreas Gerstlauer, In recognition of outstanding service as General Chair of ESWEEK 2021, Contact: Gi-Joon Nam (President)

3. SIGBED Distinguished Leadership Award @ ESWEEK

https://www.youtube.com/watch?v=su7wPNJquhE

Insup Lee, University of Pennsylvania

Citation: For leadership in promoting cross-fertilization of ACM and IEEE communities in Cyber- Physical Systems, Real-Time Systems, and Embedded Systems

4. SIGBED Technical Achievement Award @ ESWEEK 2022 https://www.youtube.com/watch?v=su7wPNJquhE

Edward A. Lee, University of California Berkeley
Citation: For foundational contributions on modeling a

Citation: For foundational contributions on modeling and design of embedded real-time, and cyber-physical systems

5. SIGBED SRC 2022 Awards @ ESWEEK 2022 https://www.youtube.com/watch?v=su7wPNJquhE Graduate Category:

Champion: Zishen Wan, Georgia Institute of Technology (to represent SIGBED in ACM Finals)

First Runner-up: Shail Dave, Arizona State University

Field-Programmable Custom Computing Machines

Los Angeles, CA Deadline: Jan 16, 2023 (Abstracts due: Jan 9, 2023) TBD

https://www.fccm.org/

ICDCS'23 – IEEE Int'l Conference on Distributed Computing Systems

Hong Kong, China Deadline: Jan 21, 2023 (Abstracts due: Jan 14, 2023) Jul 18 - 21, 2023 https://www.icdcs.org/

ISVLSI'22 – IEEE Computer Society Annual Symposium on VLSI

Iguana Falls, Brazil Deadline: Feb 23, 2023 June 20 - 23, 2023 http://www.ieee-isvlsi.org

Paper Deadlines

ICCAD'22 - IEEE/ACM Int'l Conference on Computer-Aided Design

Hybrid in-person and virtual conference Oct 30 - Nov 3, 2022 http://www.iccad.com

WOSET'22 - Workshop on Open-Source EDA Technology (virtually co-located with ICCAD 2022)

San Diego, CA Nov 3, 2022 https://woset-workshop.github.io Second Runner-up: Nurani Saoda, University of Virginia

Undergraduate Category:

Champion: Yuankai Xu, Shanghai Jiao Tong University (to represent SIGBED in ACM Finals)

First Runner-up: Yuiie Chen, Nanchang University Second Runner-up: Chamika Sudusinghe, University of Moratuwa

6. ESWEEK 2022 Outstanding Reviewer Awards @ ESWEEK 2022

https://www.youtube.com/watch?v=su7wPNJquhE

- CASES: Lars Bauer, Karlsruhe Institute of Technology; Janardhan Rao Doppa, Washington State University
- **EMSOFT**: Alain Girault, INRIA, Grenoble Ichiro Hasuo, National Institute of Informatics, Tokyo
- **CODES+ISSS**: Wanli Chang, Hunan University Ishan Thakkar, University of Kentucky

7. ESWEEK 2022 Best Paper Awards @ ESWEEK 2022 https://esweek.org/awards/

- CASES: SWAP: A Server-Scale Communication-Aware
 Chiplet-Based Manycore PIM Accelerator
 Advisor: Harsh Sharma (Washington State University), Sumit K.
 Mandal (University of Wisconsin, Madison), Janardhan Rao Doppa
 (Washington State University), Umit K. Ogras (University of
 Wisconsin, Madison), Partha Pratim Pande (Washington State
 University)
- CODES+ISSS: Exploring Synchronous Page Fault Handling Advisor: Yin-Chiuan Chen (National Taiwan University), Chun-Feng Wu (Harvard University), Yuan-Hao Chang (Academia Sinica), Tei-Wei Kuo (Academia Sinica and National Taiwan University)
- EMSOFT: Tinkertoy: Build your own operating systems for loT devices
 Advisor: Bingyao Wang and Margo Seltzer(University of British

8. ACM TECS Best Paper Award 2022 @ ESWEEK 2022 https://www.youtube.com/watch?v=su7wPNJquhE

Verifying the safety of autonomous systems with neural network controllers, Radoslav Ivanov, Taylor Carpenter, James Weimer, Rajeev Alur, George J. Pappas, Insup Lee (University of Pennsylvania)

9. Best Paper Award @ NOCS 2022 https://nocs2022.github.io/index.html

Columbia)

Traversal Packets: Opportunistic Bypass Packets for Deadlock Recovery

Zhiqiang Chen, Rangyu Deng, Kun Zeng, Xiaoqiang Ni, and Hongwei Zhou, National University of Defense Technology, China

FPT'22 - Int'l Conference on Field-Programmable Technology

Hybrid: Hong Kong, China Dec 5-9, 2022

http://icfpt.org

HiPC'22 – IEEE Int'l Conference on High Performance Computing, Data, And Analytics

Deadline: June 24, 2022 (Abstracts due: June 10, 2022) Dec 18-21, 2022 http://www.hipc.org

iSES'22 – IEEE Int'l Symposium on Smart Electronic Systems

Warangal, India
Dec 19-21, 2022

http://www.ieee-ises.org

VLSID'23 – International Conference on VLSI Design & International Conference on Embedded Systems

Novotel, HICC, Hyderabad Jan 8 - 12, 2023 <u>http://embeddedandvlsidesignconf</u>

<u>http://embeddedandvlsidesignconf</u> <u>erence.org/</u>

ASP-DAC'23 - Asia and South Pacific Design Automation Conference

Miraikan, Tokyo, Japan Jan 16-19, 2023 http://www.aspdac.com

FPGA'23 – ACM/SIGDA Int'l Symposium on

Field-Programmable Gate Arrays
Monterey, CA

Feb 12 - 14, 2023 http://www.isfpga.org

nttp://www.isipga.org

ISSCC'23 – IEEE Int'l Solid-State Circuits Conference

San Francisco, CA Feb 19-23, 2023 http://isscc.org

Who's Who

Xun Jiao

Assistant Professor, Villanova University

Research interests: Robust Computing, Efficient Computing, Al/Machine Learning, Brain-inspired Computing, Fuzz Testing

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SIGDA Partner Journal

ACM Transactions on Design Automation of Electronic Systems,

TODAES, publishes innovative work documenting significant research and development advances on the specification, design, analysis, simulation, testing, and evaluation of electronic systems, emphasizing a computer science/engineering orientation. Design automation for machine learning/AI and machine learning/AI for design automation are very much welcomed.

If you are an active researcher in the design and design automation field and would like to be part of the TODAES review board, please fill out the following reviewer form. TODAES recognizes those reviewers that provide timely and high-quality reviews through the Distinguished Review Board. For the second and third quarter of 2022, we would like to commend the following reviewers for their outstanding service.

- Ahn Jung Ho (Seoul National University)
- Benjamin Carrion Schafer (University of Texas at Dallas),
- Chung Ki-Seok (Hanyang University)
- Lorenzo Ferretti (University of California Los Angeles),
- Bharat Garg (Thapar Institute of Engineering)
- Huang Tsung-Wei (University of Illinois at Urbana-Champaign)
- Lin Xijiang (Mentor Graphics)
- Irith Pomeranz (Purdue University)
- Muhammad Shafique (New York University Abu Dhabi)
- Zhiyao Xie (Duke University)
- Xue Chun (City University of Hong Kong).

DATE'23 - Design Automation and Test in Europe

Antwerp, Belgium Mar 17-19, 2023

http://www.date-conference.com

ISPD'23 – ACM Int'l Symposium on Physical Design

Virtual Conference Mar 26 - 29, 2023 http://www.ispd.cc

ISCAS'23 – IEEE Int'l Symposium on Circuits and Systems

Monterey, CA May 21 - 25, 2023 http://iscas2023.org

RTAS'23 - IEEE Real-Time and Embedded Technology and Applications Symposium

San Antonio, Texas May 9-12, 2023 http://2023.rtas.org TODAES also recognizes papers and outstanding junior researchers through <u>best paper</u> and <u>rookie of the year</u> award. Authors can send their paper submissions on the <u>manuscript portal</u>.

TODAES also welcomes special issue proposals from leading researchers/practitioners. Such proposals should be emailed to Joerg Henkel, Senior Associate Editor, at joerg.henkel@kit.edu.

TODAES welcomes submission on <u>Special Issue on Design for Testability</u> <u>and Reliability of Security-Aware Hardware</u>. Topics of interest include, but are not limited to the following:

- Functional Testing for Security-Aware Hardware
- Design Time Testing of Hardware-Intrinsic Security Primitives
- Security in Scan Testing
- Testing for PUF Resistant to Machine Learning Attacks
- Environmental Variation Tolerance in PUF and TRNG
- Aging-Resistance of Hardware-Intrinsic Security Primitives
- Early-Stage Design for Testability and Reliability for Security-awareness

Deadline: 15 February 2023.

Tentative Publication Date: August 2023.

Technical Activities

1. <u>TSMC Expands OIP Ecosystem with Launch of 3DFabric</u> Alliance

TSMC is expanding its OIP ecosystem with the launch of the 3DFabric Alliance at the 2022 Open Innovation Platform Ecosystem Forum...

2. <u>V2X Communication Paves Pathway Toward Zero-Accident</u> Future

Hagai Zyss, CEO of Autotalks, explained how the company's recently launched V2X chipsets contribute to improving urban road traffic safety and how V2X communication paves the way toward a zero-accident, zero-death future...

3. <u>Cadence's Certus</u>, a new approach to speeding up full-chip optimization and signoff

Based on a parallel architecture and a 'distributed optimization engine', the new automated environment builds on Cadence's implementation system (Innovus) and timing signoff solution (Tempus), and promises up to 10X faster closure for designs greater than ten million cells...

Job Openings

1. Shanghai American School, China

Job Title: Lecturer in Interdisciplinary Design

Description: Teachers within Shanghai American School are recognized, along with students, as the schools most valuable resource. Faculty members are recruited and offered employment based upon prior exemplary teaching performance. Teachers must be fully credentialed / certified for their respective assignments and must maintain both teaching excellence and credentials throughout employment. PERFORMANCE RESPONSIBILITIES: Serve as one of four core teachers in The Innovation Institute, a two-year, cohort-based interdisciplinary program for ninth and tenth graders. The four core teachers - Design, Asian History, English, Physics/Chemistry - work collaboratively to teach their curriculum through shared themes and projects that connect all four disciplines allowing students to explore the topics in an applied, real-world manner. Provide day-to-day instructional excellence to each student. Actively support and promote the school's philosophy, mission, and goals. Work cooperatively with fellow-staff members and administrators in curriculum design, assessment and implementation as it pertains to specific grade levels and programs. Work cooperatively with parents to meet the needs of students and to promote the philosophy and goals of the school. Assist fellow teachers and administrators in the ordering of educational supplies and materials. Ø Coordinate and implement at the classroom level appropriate student assessments and to utilize assessment results in a prescriptive, constructive manner to promote student learning. Be knowledgeable and utilize standardized testing and other assessment data to deliver appropriate instruction to each student. Actively participate in school sponsored events & activities. Actively support the School through participation in the after school activities program, advisory program, and faculty

2. Singapore University of Technology and Design Singapore

Job Title: Research Assistant in Cybersecurity

Description: Work type: Contract, full-time Location: Singapore Categories: Bachelor Degree, Masters, iTrust, Others, IT -Network/Systems/Database, IT - Software, Others iTrust is looking for Research Assistants to design and conduct experiments on the maritime testbed MariOT and assist the RFs to develop prototypes and tools. Job Requirements: A bachelor's degree in any area of engineering. Demonstrated expertise in C/C++ or Python programming. Working knowledge of computer networks. Working knowledge of applied cryptography and/or applied machine learning is preferred. Working knowledge in software testing is preferred. Familiar with shipboard OT systems is preferred. Applications close: Standard Time. Apply Singapore Nov 2022 https://secure.dc5.pageuppeople.com/apply/799/aw/applicationFor m/initApplication.asp?lJobID=495224&sLanguage=en&sSourcePointe r=aw&lJobSourceTypeID=804.

3. Hong Kong University of Science and Technology (Guangzhou), China

Job Title: Faculty Positions in Internet of Things (IoT) Thrust

Description: The IoT Thrust has multiple tenured/tenure-track positions at the ranks of Assistant Professor, Associate Professor, and Professor. The IoT Thrust is interested in candidates who can create a multi-disciplinary IoT curriculum and pursue high impact research in a science, technology and engineering oriented environment. We offer a dynamic and collaborative academic environment within the culturally rich city of Guangzhou. Our faculty is highly diverse, joining us from world-leading institutes around the globe. Candidates should hold a Ph.D. degree and work in one or more areas related to the Thrust. Example research topics include embedded systems, data science, machine learning, optimization, computer networking, distributed computation and systems, security and privacy-enhancing technologies, human-factors in design, metaverse technologies, and next-generation applications. As a highly internationalized campus, English is the medium of instruction at HKUST(GZ) - candidates should therefore have a good command of written and spoken English. Applicants for tenure-track Assistant Professor should demonstrate strong research and teaching potentials. Applicants for Associate Professor should have a proven record in research, teaching, student supervision, and funding. Applicants for Professor

should have world-class academic achievements, international academic leadership, and an established track record in teaching, student supervision and funding. In your application, please refer to Professorpositions.com.

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