



Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 52, No.12

SIGDA - The Resource for EDA Professionals

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Circulation: 2,700

Online archive: <http://www.sigda.org/newsletter>

SIGDA News

1. [TSMC Expansion in Arizona to Target 3-nm Node](#)

Taiwan Semiconductor Manufacturing Co. (TSMC) announced this week that it's building the factory shell for a possible second fab at its Arizona site. The world's top chipmaker has already committed to a \$12 billion investment for its 5-nm fab in Arizona.

2. [With RFAB2, TI Bumping Up Analog Chip Production](#)

TI announced it began initial chip production at RFAB2, a new 300-mm analog wafer fab in Richardson, TX, that is connected to RFAB1, its 13-year-old 300-mm analog wafer fab. A few years from now, the pair will be able to produce more than 100 million analog chips per day, TI asserts.

3. [SSDs Get Smarter](#)

Today, the endurance of NAND flash—now 3D—is rarely a concern, and the now-very-mature Non-Volatile Memory express protocol (NVMe) has unlocked the full capabilities of SSDs. There's also no shortage of form factors serving different purposes in a wide array of use cases.

4. [How Graphene Is Innovating the Medical Device Sector](#)

Graphene is penetrating many commercial sectors. Despite the higher regulatory barriers enforced within the medical industry, a range of medical devices are being created using graphene for the general public.

Messages from the EICs

Dear ACM/SIGDA members,

We are excited to present to you December E-Newsletter.

We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter.

The newsletter covers a wide range of information from the upcoming conferences to technical news and activities of our community. Get involved and contact us if you want to contribute articles or announcements.

The newsletter is evolving. Please let us know what you think.

Happy reading!

Debjit Sinha, Keni Qiu,
Editors-in-Chief,
SIGDA E-News

5. [Accelerating the Transition to a Renewable-Energy Economy](#)

Scientific progress has made available a series of technologies capable of supplying the energy necessary to carry out daily activities without compromising the ecosystem. Thanks to a growing awareness of the importance of protecting the environment, these technologies are now spreading all over the world.

What is Analog Design Automation?

Sachin S. Sapatnekar
University of Minnesota

Modern computing systems increasingly interact with the inherently analog real world, and thus require analog data from sensors, cameras, antennas, etc. to be sensed and processed. Empowering these capabilities requires the design of increasingly complex analog/mixed-signal (AMS) chips. Although the analog segment of an AMS chip is typically a small portion by area, it is the part that requires the most design effort (since analog circuits are traditionally manually designed) and experiences the most post-silicon failures, requiring expensive design respins. Automating analog design is a key step in making designs reliable and enhancing design productivity.

However, despite outstanding research over several decades [1–8], this field has stubbornly resisted automation. A systematic method for building analog designs faces several difficulties: (a) each circuit type has many variants they must be comprehended by an automated algorithm (e.g., there are hundreds of variants of simple blocks such as operational transconductance amplifiers (OTAs)), and (b) unlike digital circuits, where circuit performance can be measured across different circuit families in terms of power, performance, and area (PPA), different analog circuits have performance specifications (e.g., gain/bandwidth/offset for OTAs; tuning range/phase noise for voltage-controlled oscillators (VCOs); efficiency/ripple for voltage regulators).

In addition to the greater proliferation of AMS circuits, in the last few years, several factors have provided a fillip to analog EDA. First, design rules in

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FinFET technology have become more complex than older spacing-based “lambda-rules” and are hard for the manual designer to comprehend (e.g., allowable via rules are best captured by a set of Boolean relationships). Second, design rules enforce same-direction routing in a metal layer due to lithographic constraints, reducing the design search space for EDA solutions. Third, high metal/via resistances imply that circuit performance is increasingly constrained, and standard-cell-like structures with fixed height are encouraged to keep straight metal stripes and reduce IR drops to avoid incurring via resistance costs [9]. Fourth, process variation and reliability/electromigration have become very important in determining the ability of a circuit to meet specifications. Fifth, machine learning (ML) methods have enabled new ways of emulating the expert designer within an automated flow [10–17]. Last, but not least, significant funding investments have incentivized new groups of researchers to enter the area, and the field has seen a resurgence of energy [18–30].

The ALIGN open-source analog layout automation flow [18–20] is a joint university-industry effort for automatically generating analog layouts from a netlist (SPICE file) description. ALIGN uses a mix of algorithmic techniques, template-driven design, and ML to create layouts that are at the level of sophistication of the expert designer. The solution proceeds through a compositional approach. Initially, it identifies hierarchies in the netlist using algorithmic and ML methods, also identifying constraints on symmetry and matching, including the design of arrays of transistor and passives [24–29]. Based on the process design rules from the PDK, captured using a simple yet effective abstraction, the layout is hierarchically constructed, starting from the lowest level of hierarchical blocks called primitives (e.g., differential pairs, current mirrors), and then progressing up the hierarchy, constructing a performance-optimal placement and routing at each stage.

ALIGN has been applied to a wide range of design types: low-frequency components (analog-to-digital converters (ADCs), amplifiers, and filters); wireline components (e.g., VCOs, equalizers), RF components (e.g., mixers, filters, receivers); and power delivery circuits (e.g., capacitor- and inductor-based DC-to-DC converters). It is demonstrated to perform design commercial FinFET (e.g., 16nm, 12nm, 5nm) and bulk nodes (e.g., 130nm, 65nm, 40nm). The layout capabilities of ALIGN have been leveraged in other efforts for automatically generating VCO layouts [30] and to build memory arrays in collaboration with the FASoC project [31,32]. On a recent 65nm chip tapeout of a MIMO receiver, the ALIGN-generated layout was demonstrated to be 39% smaller than a manually-generated layout, with similar performance.

Xun Jiao,
AE for What is

Muhammad Shafique,
AE for What is

Rajsaktish Sankaranarayanan,
AE for Researcher spotlight

Xin Zhao,
AE for Paper submission

Ying Wang,
AE for Technical activities

Paper Deadlines

HOST'23 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust

San Jose, CA
Deadline: Jan 16, 2023
(Winter Submission)
May 1-4, 2023
<http://www.hostsymposium.org>

FCCM' 23 - IEEE International Symposium On Field-Programmable Custom Computing Machines

Los Angeles, CA
Deadline: Jan 16, 2023
(Abstracts due: Jan 9, 2023)
<https://www.fccm.org/>

DAC'23 – Design Automation Conference

San Francisco, CA
Engineering Tracks Deadline:
Jan. 17, 2023
July 19-13, 2023
<http://www.dac.com/>

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ICDCS'23 – IEEE Int'l Conference on Distributed Computing Systems

Hong Kong, China
Deadline: Jan 21, 2023
(Abstracts due: Jan 14, 2023)
Jul 18 - 21, 2023
<https://www.icdcs.org/>

GLSVLSI'23 – ACM Great Lakes Symposium on VLSI

Knoxville, TN
Deadline: Feb. 6, 2023
June 5-7, 2023
<http://www.glsvlsi.org>

ISVLSI'22 – IEEE Computer Society Annual Symposium on VLSI

Iguana Falls, Brazil
Deadline: Feb 23, 2023
June 20 - 23, 2023
<http://www.ieee-isvlsi.org>

Upcoming Conferences

FPT'22 - Int'l Conference on Field-Programmable Technology

Hybrid: Hong Kong, China
Dec 5-9, 2022
<http://icfpt.org>

HiPC'22 – IEEE Int'l Conference on High Performance Computing, Data, And Analytics

Bangalore, India
Dec 18-21, 2022
<http://www.hipc.org>

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SIGDA Awards

1. **IEEE/ACM William J. McCalla ICCAD Best Paper Awards @ ICCAD 2022**

https://iccad.com/wp-content/uploads/sites/72/2022/11/ICCAD_2022_Virtual-Program_V11.pdf

- **Back-end:** Session 1D: SpecPart: A Supervised Spectral Framework for Hypergraph Partitioning Solution Improvement

Awardee: Ismail Bustany (AMD), Andrew Kahng (UCSD), Ioannis Koutis (New Jersey Institute of Technology), Bodhisatta Pramanik (Iowa State University), Zhiang Wang (University of California San Diego)

- **Front-end:** Session 5D: Attack Directories on ARM big.LITTLE Processors

iSES'22 – IEEE Int'l Symposium on Smart Electronic Systems

Warangal, India

Dec 19-21, 2022

<http://www.ieee-ises.org>

VLSID'23 – International Conference on VLSI Design & International Conference on Embedded Systems

Novotel, HICC, Hyderabad

Jan 8 - 12, 2023

<https://vlsid.org/>

ASP-DAC'23 - Asia and South Pacific Design Automation Conference

Miraikan, Tokyo, Japan

Jan 16-19, 2023

<http://www.aspdac.com>

HiPEAC'23: Int'l Conference on High Performance Embedded Architectures & Compilers

Toulouse, France

Jan 16-18, 2022

<https://www.hipeac.net/2023/toulouse/>

FPGA'23 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays

Monterey, CA

Feb 12 - 14, 2023

<http://www.isfpnga.org>

ISSCC'23 – IEEE Int'l Solid-State Circuits Conference

San Francisco, CA

Feb 19-23, 2023

<http://isscc.org>

DATE'23 - Design Automation and Test in Europe

Antwerp, Belgium

Mar 17-19, 2023

<http://www.date-conference.com>

ISPD'23 – ACM Int'l Symposium on

Awardee: Zili Kou (Hong Kong University of Science and Technology), Sharad Sinha (Indian Institute of Technology Goa), Wenjian He (Hong Kong University of Science and Technology), Wei Zhang (Hong Kong University of Science and Technology)

2. **IEEE/ACM William J. McCalla ICCAD Best Paper Award Nominations @ ICCAD 2022**

https://iccad.com/wp-content/uploads/sites/72/2022/11/ICCAD_2022_Virtual-Program_V11.pdf

- **Front-end:** Session 8D: Logic Synthesis for Digital In-Memory Computing

Awardee: Muhammad Rashedul Haq Rashed (University of Central Florida), Sumit Kumar Jha (University of Texas at San Antonio), Rickard Ewetz (University of Central Florida)
- **Front-end:** Session 7D: ObfuNAS: A Neural Architecture Search-based DNN Obfuscation Approach

Awardee: Tong Zhou (Northeastern University), Shaolei Ren (UC Riverside), Xiaolin Xu (Northeastern University)
- **Back-end:** Session 11B: DeePEB: A Neural Partial Differential Equation Solver for Post Exposure Baking Simulation in Lithography

Awardee: Qipan Wang (Peking University), Xiaohan Gao (Peking University), Yibo Lin (Peking University), Runsheng Wang (Peking University), Ru Huang (Peking University)
- **Back-end:** Session 7A: TransSizer: A Novel Transformer-Based Fast Gate Sizer

Awardee: Siddhartha Nath (NVIDIA Corp), Geraldo Pradipta (NVIDIA Corp), Corey Hu (NVIDIA Corp), Tian Yang (NVIDIA Corp), Bruce Khailany (NVIDIA), Haoxing Ren (NVIDIA Corporation)

3. **William J. McCalla ICCAD Ten Year Retrospective Most Influential Paper Award @ ICCAD 2022**

https://iccad.com/wp-content/uploads/sites/72/2022/11/ICCAD_2022_Virtual-Program_V11.pdf

On reconfiguration-oriented approximate adder design and its application

Awardee: Rong Ye (The Chinese University of Hong Kong), Ting Wang (The Chinese University of Hong Kong), Feng Yuan (The Chinese

Physical Design

Virtual Conference
Mar 26 - 29, 2023
<http://www.ispd.cc>

ISQED'23 - Int'l Symposium on Quality Electronic Design

San Francisco, CA
April 5-7, 2023
<http://www.isqed.org>

ISCAS'23 - IEEE Int'l Symposium on Circuits and Systems

Monterey, CA
May 21 - 25, 2023
<http://iscas2023.org>

RTAS'23 - IEEE Real-Time and Embedded Technology and Applications Symposium

San Antonio, Texas
May 9-12, 2023
<http://2023.rtas.org>

University of Hong Kong), Rakesh Kumar (University of Illinois at Urbana-Champaign), Qiang Xu (The Chinese University of Hong Kong)

In 2013 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 48-54. IEEE, 2013. The award is given to the paper judged to be the most influential on research and industry practice in computeraided design of integrated circuits over the ten years since its original appearance at ICCAD. The awards are jointly sponsored by IEEE Council on Electronic Design Automation (IEEE CEDA) and the ACM Special Interest Group on Design Automation (ACM SIGDA).

4. 2022 IEEE CEDA Ernest S. Kuh Early Career Award @ ICCAD 2022

https://iccad.com/wp-content/uploads/sites/72/2022/11/ICCAD_2022_Virtual-Program_V11.pdf

Bei Yu (The Chinese University of Hong Kong) For contributions to machine learning in physical design and Design for Manufacturability

5. 2022 IEEE CEDA Outstanding Service Recognition @ ICCAD 2022

https://iccad.com/wp-content/uploads/sites/72/2022/11/ICCAD_2022_Virtual-Program_V11.pdf

Rolf Drechsler (University of Bremen) For outstanding service to the EDA community as ICCAD General Chair in 2021

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