



Special Interest Group on Design Automation ACM/SIGDA E-NEWSLETTER, Vol. 52, No. 7

SIGDA - The Resource for EDA Professionals

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
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SIGDA News

1. U.S. Announces World's First Exascale Computer

The U.S. announced the world's first exascale computer this week, Frontier, powered by AMD chips. Oak Ridge National Laboratory's Frontier system led the Top500 list at 1.1 exaflops, making it the first to break the exascale barrier.

2. Supercharging Hyperscale and HPC with Superchips

Nvidia launched the concept of superchips at its GTC conference. "Superchip" is what the company calls its modules with two computing dies; the Grace Superchip has two Grace CPUs, and the Grace Hopper superchip has one Grace CPU and one Hopper GPU.

3. TSMC Creates Design Options for New 3nm Node

Taiwan Semiconductor Manufacturing Co. (TSMC) has created versions of its upcoming 3nm FinFET node, allowing chip designers to enhance performance, power efficiency, and transistor density — or select a balance of those options.

4. Micron Readies for Level 5 Autonomy with LPDDR5 DRAM

The journey to Level 5 autonomy is taking longer than initially expected, but Micron Technology is opting to be well prepared so that any memory content meets tomorrow's reliability requirements today. Micron announced that its LPDDR5 memory is now Automotive Safety Integrity Level (ASIL) D certified, under ISO

Messages from the EiCs

Dear ACM/SIGDA members,

We are excited to present to you July E-Newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter.

The newsletter covers a wide range of information from the upcoming conferences to technical news and activities of our community. Get involved and contact us if you want to contribute articles or announcements.

The newsletter is evolving. Please let us know what you think.

Happy reading!

Debjit Sinha, Keni Qiu,
Editors-in-Chief,
SIGDA E-News

26262, which is considered one of the most stringent safety integrity levels for automotive safety.

5. [OpenLight Announces New Open Silicon Photonics Platform](#)

OpenLight, a newly launched, independent company formed by investments from Synopsys and Juniper, announced yesterday the world's first open silicon photonics platform with integrated lasers. The California-based company seeks to provide chip manufacturers with a means to create photonic integrated circuits (PICs) that offer the highest performance possible. Applications will include datacom, telecom, and LiDAR markets, to name a few, all while operating at low power.

6. [Purdue Starts Comprehensive Semiconductor Degree Programs in U.S.](#)

Purdue University is ramping up what it calls the first "comprehensive" degree program in the U.S. in semiconductor engineering as America aims to rebuild its chip industry.

What Is

What is Runtime Verification?

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Column Editor: Xun Jiao <xun.jiao@villanova.edu>

Runtime verification is an approach for systems to monitor the system events or the surrounding environments, check specific properties, and probably take the appropriate actions [1]. One representative example is an autonomous vehicle: no matter how the autonomous vehicle is designed or how complex it is, one can require the autonomous vehicle to stop if it is going to collide with an object or an obstacle in front of it, which can be implemented as a runtime monitor.

The essential pieces of runtime verification include a system, a property, and a runtime monitor. A property in runtime verification is defined by a property specification language (e.g., regular

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AE for Local chapter news

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AE for Awards

Xun Jiao,
AE for What is

expression, linear temporal logic) or an equivalent automation (e.g., finite-state machine, Büchi automation). From the property, a runtime monitor can be synthesized, usually in an automatic way, and instrumented to the target system. When the system is executing, the runtime monitor observes the system events and checks (verdicts) if the corresponding property is satisfied or violated. If the runtime monitor can provide the verdict to the system, the system can take the corresponding actions, depending on satisfaction or violation of the property.

There are several features of runtime verification. First, for complex systems and complex properties which are difficult to perform formal verification (e.g., model checking, theorem proving) due to the high computational complexity, runtime verification can at least provide some alternative guarantees to the systems. Second, these properties and the corresponding runtime monitors are usually lightweight so that they can be verified in real-time. Third, runtime verification can play the "last line of defense" in system design to prevent systems from entering unsafe states, which is crucial for systems having probabilistic behaviors. Moreover, for a system with an assume-guarantee contract under an uncertain environment, runtime verification can also be used to monitor if the assumption is violated, implying that the guarantee may be violated. In this case, the system should be switched to a special mode (e.g., a safe mode) [2,3].

In summary, runtime verification is a lightweight solution to systems requiring guarantees with limited resources. It can be applied to various domains, such as software engineering, cyber-physical systems, and general safety-critical systems.

References

- [1] E. Bartocci, Y. Falcone, A. Francalanza, and G. Reger, "Introduction to runtime verification," in Lectures on Runtime Verification, Lecture Notes in Computer Science, vol. 10457, Springer, Cham, 2018.
- [2] S. Raghavan, K. Watanabe, E. Kang, C.-W. Lin, Z. Jiang, and S. Shiraishi, "Property-driven runtime resolution of feature interactions," in International Conference on Runtime Verification (RV), pp. 316--333, Limassol, Cyprus, Nov. 2018.
- [3] S.-L. Wu, C.-Y. Bai, K.-C. Chang, Y.-T. Hsieh, C. Huang, C.-W. Lin, E. Kang, and Q. Zhu, "Efficient system verification with multiple weakly-hard constraints for runtime monitoring," in International Conference on Runtime Verification, pp. 497--516, Los Angeles (Virtual), CA, 2020.

Muhammad Shafique,

AE for What is

Rajsaktish Sankaranarayanan,

AE for Researcher spotlight

Xin Zhao,

AE for Paper submission

Ying Wang,

AE for Technical activities

Paper Deadlines

MLCAD'22 - ACM/IEEE Workshop on Machine Learning for CAD

Snowbird, Utah

Deadline: Jul 10, 2022

Sep 12 - 13, 2022

<https://mlcad-workshop.org/>

VLSID'23 - International Conference on VLSI Design & International Conference on Embedded Systems

Novotel, HICC, Hyderabad

Deadline: Jul 10, 2022

Jan 8 - 12, 2023

<http://embeddedandvlsidesignconference.org/>

FPT'22 - Int'l Conference on Field-Programmable Technology

Hybrid: Hong Kong, China

Deadline: Jul 15, 2022

(Abstracts due: Jul 8, 2022)

Dec 5-9, 2021

<http://icfpt.org>

IWBDA'22 - Int'l Workshop on Bio-Design Automation

Online

Abstract deadline: Jul 22, 2022

Oct 24-26, 2022

<http://www.iwbdaconf.org/2022>

SIGDA Awards

1. Best Paper Award @ GLSVLSI 2022

<http://www.gslvlsi.org/>

- **1st place:** Fast Parallel High-Level Synthesis Design Space Explorer: Targeting FPGAs to accelerate ASIC Exploration

Md Imtiaz Rashid and Benjamin Carrion Schafer

- **2nd place:** Protected ECC Still Leaks: A Novel Differential-Bit Side-channel Power Attack on ECDH and Countermeasures

Tianhong Xu, Gongye Cheng and Yunsi Fei

- **3rd place:** Thermal and Power-Aware Run-time Performance Management of 3D MPSoCs with Integrated Flow Cell Arrays

Halima Najibi, Alexandre Levisse, Giovanni Ansaloni, Marina Zapater and David Atienza

ASP-DAC'23 - Asia and South Pacific Design Automation Conference

Miraikan, Tokyo, Japan

Deadline: Jul 29, 2022

(Abstracts due: Jul 24, 2022)

Jan 16-19, 2023

<http://www.aspdac.com>

iSES'22 – IEEE Int'l Symposium on Smart Electronic Systems

Warangal, India

Deadline: Aug 1, 2022

Dec 19-21, 2022

<http://www.ieee-ises.org>

WOSET'22 - Workshop on Open-Source EDA Technology (virtually co-located with ICCAD 2022)

San Diego, CA

Deadline: Sept. 1, 2022

Nov 3, 2022

<https://woset-workshop.github.io>

ISSCC'23 – IEEE Int'l Solid-State Circuits Conference

San Francisco, CA

Deadline: Sept 7, 2022

Feb 19-23, 2023

<http://isscc.org>

FPGA'23 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays

Monterey, CA

Deadline: Sept 23, 2022

(Abstracts due: Sept 16, 2022)

Feb 12 - 14, 2023

<http://www.isfpga.org>

DATE'23 - Design Automation and Test in Europe

Antwerp, Belgium

Deadline: Sept 25, 2022

(Abstracts due: Sept 18, 2022)

Mar 17-19, 2023

<http://www.date-conference.com>

Who's Who

Fan Chen

Assistant Professor, Indiana University Bloomington

Research interests: Beyond-CMOS Computing, Quantum Machine Learning, Accelerator Architecture for Emerging Applications, Emerging Nonvolatile Memory

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SIGDA Partner Journal

The ACM Transactions on Design Automation of Electronic Systems (TODAES) is a premier ACM journal in design and automation of electronic systems.

1. Special Issue on Advances in Physical Design Automation

Guest Editors

- Iris Hui-Ru Jiang, National Taiwan University
- David Chinnery, Siemens Digital Industries Software
- Gracieli Posser, Cadence Design Systems
- Jens Lienig, Dresden University of Technology

The special issue seeks recent advances and innovations for More Moore and More-than-Moore in a physical design context. In addition to submissions from academia, submissions from industry are also welcome. Research papers with emphasis on the following topics are of particular interest: placement, routing, and ECO; advances towards analog design automation; physical design for heterogeneous integration; physical design for advanced lithography technology; hardware security-related physical design; and physical design for emerging technologies.

[Click here for the full Call for Papers and submission instructions.](#)

Important Dates

- Open for submissions: May 1st, 2022
- Submissions deadline: July 31st, 2022
- First-round review decisions: September 16th, 2022
- Deadline for revision submissions: October 14th, 2022
- Notification of final decisions: November 30th, 2022
- Tentative publication: Spring 2023

For questions and further information, please contact guest editors:

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- Gracieli Posser, gposser@cadence.com
- Jens Lienig, jens.lienig@tu-dresden.de

ISPD'23 – ACM Int'l Symposium on Physical Design

Virtual Conference
Deadline: Oct 7, 2022
(Abstracts due: Sept. 30, 2022)
Mar 26 - 29, 2023
<http://www.ispd.cc>

ISCAS'23 – IEEE Int'l Symposium on Circuits and Systems

Monterey, CA
Deadline: Oct. 24, 2022
May 21 - 25, 2023
<http://iscas2023.org>

Upcoming Conferences

ISVLSI'22 – IEEE Computer Society Annual Symposium on VLSI

Cyprus
July 4-6, 2022
<http://www.ieee-isvlsi.org>

ICDCS'22 – IEEE Int'l Conference on Distributed Computing Systems

Bologna, Italy
Jul 10 - 13, 2022
<https://www.icdcs.org/>

DAC'22 – Design Automation Conference

San Francisco, CA
July 10-14, 2022
<http://www.dac.com/>

IWLS'22 - International Workshop on Logic & Synthesis

Virtual conference
Jul 18-21, 2022
<https://www.iwls.org>

2. TODAES Rookie of the Year Award

The ACM Transactions on Design Automation is proud to announce the winner of the 2021 “Rookie of the Year” Award. This newly introduced award aims to highlight the achievement of junior researchers in the Design and Design Automation of Electronic Systems field. Specifically, the award recognizes an author whose first-ever peer-reviewed journal paper as a lead author is published in ACM TODAES.

The winner for 2022 is **Yukui Luo** for the research article, “FPGAPRO: A Defense Framework Against Crosstalk-Induced Secret Leakage in FPGA”.

Readers may review this paper on the ACM TODAES Proceedings website at <https://dl.acm.org/doi/abs/10.1145/3491214>.

3. Distinguished Reviewer Board

As a premier journal in the EDA area, TODAES has continued to strive for shorter submission-to-first-review and accept-to-publication time.

Through the Distinguished Reviewer Board, TODAES recognizes those reviewers whose outstanding contributions have provided an invaluable service to TODAES as well as to the community. To be recognized as a member of the Distinguished Reviewer Board, a reviewer must have

- reviewed 3 or more papers in a 12 month period,
- submitted reviews that have been rated of the highest quality by the inviting Associate Editors, and
- returned all reviews on time.

If you are interested in becoming a member of the Distinguished Reviewer Board, please fill the form at <https://lnkd.in/dGPM2aV>

The current Distinguished Reviewer Board is updated every 3 months, and can be found on page at the following link: <https://dl.acm.org/journal/todaes/distinguished-reviewers-board>

ISLPED'21 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design

Boston University, Boston, MA
(Hybrid)

Aug 1-3, 2022

<http://www.islped.org>

VLSI-SoC'22 – IFIP/IEEE Int'l Conference on Very Large Scale Integration

Patras, Greece

Oct 3-5, 2022

<http://www.vlsi-soc.com>

NOCS'22 – IEEE/ACM Int'l Symposium on Networks-on-Chip (co-located with ESWEEK 2022)

Hybrid Conference. Shanghai, China

Oct 7-14, 2022

<https://nocs2022.github.io>

ESWEEK'22 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)

Hybrid Conference. Shanghai, China

Oct 7-14, 2022

<http://www.esweek.org>

PACT'22 - Int'l Conference on Parallel Architectures and Compilation Techniques

Chicago, IL

Oct 10-12, 2022

<http://www.pactconf.org>

BioCAS'22 – Biomedical Circuits and Systems Conference

Taipei, Taiwan

Oct 13-15, 2022

<https://2022.ieee-biocas.org/>

MEMOCODE'22 - IEEE/ACM Int'l Conference on Formal Methods and models for System Design (co-located with ESWEEK 2022)

Hybrid Conference. Shanghai,

China
Oct 13-14, 2022
<https://memocode2022.github.io>

**MICRO'22 – IEEE/ACM Int'l
Symposium on
Microarchitecture**

Chicago, IL
October, 2022
<http://www.microarch.org/micro55>

**ICCD'22 – IEEE Int'l Conference
on Computer Design**

Lake Tahoe
Oct 23-26, 2022
<http://www.iccd-conf.com>

**ICCAD'22 – IEEE/ACM Int'l
Conference on Computer-Aided
Design**

Hybrid in-person and virtual
conference
Oct 30 - Nov 3, 2022
<http://www.iccad.com>

**HiPC'22 – IEEE Int'l Conference
on High Performance
Computing, Data, And Analytics**

Deadline: June 24, 2022
(Abstracts due: June 10, 2022)
Dec 18-21, 2022
<http://www.hipc.org>

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