Special Interest Group on Design Automation
ACM/SIGDA E-NEWSLETTER, Vol. 51, No. 11

SIGDA - The Resource for EDA Professionals

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
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Newsletter format poll

Dear readers,

We are in the process of updating the E-newsletter and would like to have your feedback on which format you would like to receive and read it. Here is a tiny poll and your feedback will be very helpful for us as we move forward. Thank you for your time to take the poll, this should not take more than a few seconds.
Poll link: https://www.surveymonkey.com/r/3J6G6FG.

Best regards,
Debjit Sinha and Keni Qiu

SIGDA News

1. Intel Unveils Second-Generation Neuromorphic Chip
Intel has unveiled its second-generation neuromorphic computing chip, Loihi 2, the first chip to be built on its Intel 4 process technology. Designed for research into cutting-edge neuromorphic neural networks, Loihi 2 brings a range of improvements. They include a new instruction set for neurons that provides more programmability, allowing spikes to have integer values beyond just 1 and 0, and the ability to scale into three-dimensional meshes of chips for larger systems.

2. Moore's Law Could Ride EUV for 10 More Years
ASML plans to introduce new extreme ultraviolet (EUV) lithography equipment that will extend the longevity of Moore's

Dear ACM/SIGDA members,

We are excited to present to you November E-Newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from the upcoming conferences and hot research topics to technical news and activities from our community. Get involved and contact us if you want to contribute an article or announcement. Please take a minute of your time and complete the format poll in this newsletter - We value your feedback.
Happy reading!

Debjit Sinha, *Keni Qiu*,
SigDA E-News
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Law for at least ten years, according to executives at the world's only supplier of the tools, which are crucial for the world's most advanced silicon.

3. SiC and GaN: A Tale of Two Semiconductors
Over the last several decades, advances in silicon carbide and gallium nitride technologies has been characterized by development, growing industry acceptance and the promise of billion-dollar revenues. The first commercial SiC device arrived in 2001 in the form of a Schottky diode from Germany's Infineon. Rapid development has followed, and the industry sector is now poised to exceed $4 billion by 2026.

4. GaN Emerges for Next-Gen Power Electronics
Applications such as power conversion in automotive, consumer and aerospace applications are leveraging the advantages of gallium nitride (GaN) technology, according to participants in the recent industry event sponsored by Dutch chipmaker Nexperia.

5. TI Rolls 3D Hall Sensor for Real-Time Control
Texas Instruments has introduced TMAG5170, the first device in a new family of 3D Hall-effect position sensors for real-time control in factory automation and motor-drive applications. The sensor is promoted as providing integrated functions and diagnostics to maximize design flexibility and system safety while saving energy.

6. Foxconn Enters Chip Production with Macronix Deal
Foxconn, the world's largest assembler of consumer devices such as Apple's iPhone, is entering semiconductor production as part of a plan to expand into electric vehicles.

7. Qualcomm Takes on Nvidia for MLPerf Inference Title
Foxconn, the world's largest assembler of consumer devices such as Apple's iPhone, is entering semiconductor production as part of a plan to expand into electric vehicles.

8. European IC Effort Doubles Down on Tech Sovereignty
The pursuit of technology sovereignty from China to the U.S. to Europe has moved to the forefront as semiconductors emerge as the coin of the realm.

Paper deadlines

ISCAS'22 – IEEE Int'l Symposium on Circuits and Systems
Austin, TX
Deadline: Nov. 1, 2021 (Special Sessions: Nov. 22, 2022)
May 28 - June 1, 2022
http://iscas2022.org

What Is column

What is Customizable Computing?

Zhenman Fang,
Assistant Professor,
School of Engineering Science
Simon Fraser University, Canada

With the end of Moore's law for general-purpose CPU scaling, new computing paradigms have been actively explored to meet the ever-increasing computing demands and energy efficiency requirements of future applications, such as machine learning, personalized healthcare, and big data applications. As one of the most promising paradigms, customizable computing tailors the computer architecture (known as hardware accelerators) for these important application domains to improve their performance and energy efficiency by orders-of-magnitude [1]. Such improvements are usually achieved by three major types of customizations: custom compute engines, custom memory hierarchy, and custom data representations [2].

Custom compute engines typically explore the following pipeline and parallelization techniques to execute more operations concurrently to improve their throughput: 1) accelerator-unique fine-grained custom pipeline, which is often deeply pipelined and tightly coupled with fine-grained operator-level parallelization, different from CPUs and GPUs, 2) coarse-grained parallelization that further parallelizes multiple fine-grained pipelines, which can be both homogeneous (i.e., data parallelism) and heterogeneous (i.e., task parallelism) parallelization, similar to multicore processors, and/or 3) accelerator-unique coarse-grained pipeline that is composed of multiple fine-grained pipelines. Such compute engines can be implemented as fixed-function accelerators (i.e., ASICs, such as Google TPU [3]), coarse-grained composable accelerators, as well as fine-grained programmable fabric (i.e., FPGA) [1].

Moreover, the memory hierarchy can also be customized using 1) custom on-chip buffering, caching, and their mix, to improve data reuse and exploit much higher on-chip bandwidth, 2) streaming

DAC'22 – Design Automation Conference
San Francisco, CA
Research Paper Deadline: Nov. 22, 2021 (Abstracts due: Nov. 15, 2021)
Engineering Tracks Deadline: Jan. 17, 2022
July 10-14, 2022
http://www.dac.com/

ISCA'22 – Int'l Symposium on Computer Architecture
New York City, USA
Deadline: Nov 23, 2021 (Abstracts due: Nov 16, 2021)
June 11-15, 2022
https://iscaconf.org/isca2022/

FCCM'22 - IEEE International Symposium On Field-Programmable Custom Computing Machines
New York
Deadline: Jan 10, 2022 (Abstracts due: Jan 3, 2022)
May 15–18, 2022
https://www.fccm.org/

MDTS'22 – IEEE Microelectronics Design & Test Symposium
Albany, NY
Deadline: Feb 28, 2022
May 23-25, 2022
http://natw.ieee.org

ISVLSI'22 – IEEE Computer Society Annual Symposium on VLSI
Cyprus
Deadline: TBD
July 6-8, 2022
http://www.ieee-isvlsi.org

optimization and/or custom network-on-chip (NoC) to enable direct communication between multiple computing engines on-chip and/or bypass off-chip memory access, and 3) off-chip memory optimizations that aims to either fully utilize the off-chip bandwidth through memory access reorganization and/or hide the off-chip access latency from the compute engines through coarse-grained pipeline or data prefetching. Finally, custom data representations with a reduced (or widened) bit width can play a vital and unique role in further improving the accelerator performance in synergy with custom compute engines and memory hierarchy.

One good example that enables most of these customization techniques is the recent Xilinx Adaptive Compute Acceleration Platform, which incorporates AI Engines (ASIC) and FPGA fabric, caches and buffers, as well as a hardened NoC, all on the same chip [4]. It provides users ample opportunities to accelerate their applications through various customization techniques.

While very promising, there are still several major challenges remaining to enable a much wider adoption of customizable computing. First, it is nontrivial to find the right balance between customization for better performance and general-purpose for better flexibility [5][6]. Second, it is nontrivial to figure out at which levels of the compute hierarchy---on the processor-side, memory-side, storage-side, and/or network-side---to integrate custom accelerators, and how to efficiently integrate and coordinate them to achieve the optimal system-level performance [7]. Finally, it remains a challenge to productively program custom accelerators to achieve efficient application performance, which calls for higher-level programming abstractions (at both the hardware and software levels), more automated and faster synthesis and compilation support, as well as faster and easier-to-use debugging tools [2].

References
[1] Jason Cong, Zhenman Fang, Muhuan Huang, Peng Wei, Di Wu, Cody Hao Yu. Customizable Computing: From Single-Chip to Datacenters. Proceedings of the IEEE (PIEEE 2019), Volume 107, Issue 1, Pages 185 - 203, Jan. 2019.
[2] Yi-Hsiang Lai, Ecenur Ustun, Shaojie Xiang, Zhenman Fang, Hongbo Rong, Zhiru Zhang. Programming and Synthesis for Software-defined FPGA Acceleration: Status and Future Prospects. ACM Transactions on Reconfigurable Technology and Systems (TRETS 2021), Volume 14, Issue 4, December 2021, Article No.: 17, pp 1–39.
[3] Norman P. Jouppi, Cliff Young, et al. In-Datacenter Performance Analysis of a Tensor Processing Unit. In Proceedings of the 44th Annual International Symposium on Computer Architecture (ISCA 2017), New York, NY, USA, 1–12.

Upcoming conferences

ICCAD'21 – IEEE/ACM Int'l Conference on Computer-Aided Design Virtual Conference
Nov 1-4, 2021
http://www.iccad.com

WOSET'21 - Workshop on Open-Source EDA Technology (virtually co-located with ICCAD 2021)
San Diego, CA
Nov 4, 2021
https://woset-workshop.github.io

2nd ROAD4NN Workshop: Research Open Automatic Design for Neural Networks (Co-located with DAC 2021)
San Francisco, CA
Dec 5, 2021
https://easychair.org/cfp/ROAD4NN2021

DAC'21 – Design Automation Conference
San Francisco
Dec 5–9, 2021
http://www.dac.com/

FPT'21 - Int'l Conference on Field-Programmable Technology
Auckland, New Zealand
Dec 6-10, 2021
http://icfpt.org

[4] Brian Gaide, Dinesh Gaitonde, Chirag Ravishankar, Trevor Bauer. 2019. Xilinx Adaptive Compute Acceleration Platform: VersalTM Architecture. In Proceedings of the 2019 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2019), New York, NY, USA, 84–93.

[5] Jason Cong, Zhenman Fang, Michael Lo, Hanrui Wang, Jingxian Xu, Shaochong Zhang. Understanding Performance Differences of FPGAs and GPUs. The 26th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2018 short paper), Boulder CO, May 2018, pp. 172-175.

[6] Vidushi Dadu, Jian Weng, Sihao Liu, and Tony Nowatzki. 2019. Towards General Purpose Acceleration by Exploiting Common Data-Dependence Forms. In Proceedings of the 52nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO 2019), New York, NY, USA, 924–939.

[7] Nazanin Farahpour, Yuchen Hao, Zhenman Fang, Glenn Reinman. Reconfigurable Accelerator Compute Hierarchy: A Case Study Using Content-Based Image Retrieval. The 2020 IEEE International Symposium on Workload Characterization (IISWC 2020), Virtual Conference, Oct 2020, pp. 276-287.

Call for Award Nominations

1. ACM Outstanding Ph.D. Dissertation Award in Electronic Design Automation

Deadline Nov. 30, 2021

Design automation has gained widespread acceptance by the VLSI circuits and systems design community. Advancement in computer-aided design (CAD) methodologies, algorithms, and tools has become increasingly important to cope with the rapidly growing design complexity, higher performance and low-power requirements, and shorter time-to-market demands. To encourage innovative, ground-breaking research in the area of electronic design automation, the ACM's Special Interest Group on Design Automation (SIGDA) has established an ACM award to be given each year to an outstanding Ph.D. dissertation that makes the most substantial contribution to the theory and/or application in the field of electronic design automation.

The award consists of a certificate and a check for $1,000 and is presented at the Design Automation Conference, which is held in June/July of each year. The award is selected by a committee of

DAForum'21 - SIGDA/IEEE CEDA Ph.D. Forum at DAC 2021
San Francisco, CA
Dec 6, 2021
https://easychair.org/cfp/daforum21

HOST'21 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
Washington DC
Dec 12-15, 2021
http://www.hostsymposium.org

HiPC'21 – IEEE Int'l Conference on High Performance Computing, Data, And Analytics
Bangalore, India
Dec 17-20, 2021
http://www.hipc.org

VLSID'22 – International Conference on VLSI Design & International Conference on Embedded Systems
Virtual Conference
Feb 19-23, 2022
http://embeddedandvlsidesignconference.org/

iSES'21 – IEEE Int'l Symposium on Smart Electronic Systems
Jaipur, India
Dec 20-22, 2021
http://www.ieee-ises.org

ASP-DAC'22 - Asia and South Pacific Design Automation Conference
Virtual Conference
Jan 17-20, 2022
http://www.aspdac.com

ISSCC'22 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Feb 20-24, 2022
http://isscc.org

experts from academia and industry in the field and appointed by ACM in consultation with the SIGDA Chair.

Deadline: November 30th of each year

Nomination requirements: Each department of any university may nominate at most two Ph.D. dissertations whose final submission date is between July 1st of the previous year and June 30th of the current year. Each nomination package must be emailed by November 30 and should consist of:

1) The PDF file of the Ph.D. dissertation. If the nominated Ph.D. dissertation is not written in English, an English translation of the entire dissertation must be included in the nomination package.
2) A statement (up to two pages) from the nominee explaining the significance and major contributions of the work.
3) A nomination letter from nominee's department chair or dean of the school endorsing the application.
4) Optionally, up to three letters of recommendation from experts in the field. These letters may be included in the nomination package or sent separately to the address below.

The nomination materials should be emailed to SIGDA-Award@acm.org (Subject: ACM Outstanding Ph.D. Dissertation Award in EDA).

All standard conflict of interest regulations as stated in ACM policy will be applied (see https://awards.acm.org/conflict-of-interest). Any awards committee members will recuse themselves from consideration of any candidates where a conflict of interest may exist.

2. SIGDA Outstanding New Faculty Award

Deadline: Nov. 30, 2021

The SIGDA Outstanding New Faculty Award recognizes a junior faculty member early in her or his academic career who demonstrates outstanding potential as an educator and/or researcher in the field of electronic design automation. While prior research and/or teaching accomplishments are important, the selection committee will especially consider the impact that the candidate has had on her or his department and on the EDA field during the initial years of their academic appointment. The award is presented annually at Design Automation Conference, and

FPGA'22 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Monterey, CA
Feb 27 - Mar 1, 2022
http://www.isfpga.org

DATE'22 - Design Automation and Test in Europe
Antwerp, Belgium, and online
Mar 14-23, 2022
http://www.date-conference.com

ISPD'22 – ACM Int'l Symposium on Physical Design
Banff, Alberta, Canada
Mar 27 - 30, 2022
http://www.ispd.cc

ISQED'22 - Int'l Symposium on Quality Electronic Design
California
April 6-8, 2022
http://www.isqed.org

RTAS'22 - IEEE Real-Time and Embedded Technology and Applications Symposium
Milano, Italy
May 4-6, 2022
http://2022.rtas.org

currently consists of a $1,000 award to the faculty member, along with a citation.

Eligibility: SIGDA Outstanding new faculty who are developing academic careers in areas in or related to electronic design automation are encouraged to apply for this award. Note that this award is not intended for senior or highly experienced investigators who have already established independent research careers, even if they are new to academia. Candidates must have recently completed at least one full academic year and no more than four full academic years in a tenure-track position. Applications will also be considered from people whose appointments are continuing (non-visiting) positions with substantial educational responsibilities regardless whether or not they are tenure track. Persons holding research-only positions are not eligible. Exceptions to the timing requirements will be made for persons who have interrupted their academic careers for substantive reasons, such as family or medical leave. The presence of such reasons must be attested by the sponsoring institution, but no explanation is needed.

Application: Candidates applying for the award must submit the following to the selection committee no later than November 30 of the current year:
1) a 2-page statement summarizing the candidate's teaching and research accomplishments since beginning their current academic position, as well as an indication of plans for further development over the next five years;
2) a copy of a current curriculum vitae;
3) a letter from either the candidate's department chair or dean endorsing the application.

The nomination materials should be emailed by the deadline to SIGDA-Award@acm.org (Subject: ACM/SIGDA Outstanding New Faculty Award).

All standard conflict of interest regulations as stated in ACM policy will be applied (see https://awards.acm.org/conflict-of-interest). Any awards committee members will recuse themselves from consideration of any candidates where a conflict of interest may exist.

Technical activities

1. [AI Has Unlocked a Secret of Human Biology](#)
The knowledge bank shared by DeepMind is no small gift to the scientific community...

2. [Authenticating Batteries Before Rapid and Fast Charging](#)
With little room left to differentiate smartphones in terms of fit, form, and function, battery life and charging speed have become the new killer features...

3. [Space Jam: Efforts Launched to Corral Orbital Junk](#)
Calls grow to deploy precision navigation and life extension technologies...

Job Openings

1. University of Colorado Boulder Department of Electrical and Computer Engineering, United States
Job Title: Faculty Position in Electrical, Computer and Energy Engineering

Description: The University of Colorado offers excellent benefits, including medical, dental, retirement, paid time off, tuition benefit and ECO Pass. The University of Colorado Boulder is one of the largest employers in Boulder County and offers an inspiring higher education environment. Learn more about the University of Colorado Boulder. The University of Colorado does not discriminate on the basis of race, color, national origin, sex, age, pregnancy, disability, creed, religion, sexual orientation, gender identity, gender expression, veteran status, political affiliation, or political philosophy. All qualified individuals are encouraged to apply. Click here for a list of ADA and Title IX coordinators. Posting Contact Information Posting Contact Name: Prof. Dejan S. Filipovic Posting Contact Email: dejan@colorado.edu.

2. DTU Denmark Professor in Real-Time Computer Architecture
Job Title: Professor in Real-Time Computer Architecture

Description: If you are ambitious and internationally renowned for your research on Real-Time Computer Architecture, you might be our new professor at our Section for Embedded Systems Engineering. DTU Compute invites applications for an appointment as Professor in Real-Time Computer Architecture conducting research on real-time and time-predictable systems. As the position is part of the department's capacity building related to DIREC, the National Digital Research Centre, you must appreciate close professional relations with colleagues both inside and outside of DTU. The appointment will be based on the collective agreement with the Danish Confederation of Professional Associations. The salary for the position will be determined by the applicant's qualifications and in agreement with the relevant union. Further information on qualification requirements and job content may be found in the Ministerial Order on Job Structure for Academic Staff at Universities. Further information may be obtained from Head of Department Per B. Brockhoff, tel.: +45 2044 1711 or Head of Section, Professor Jan Madsen, tel.: +45 4525 3751. You can read more about DTU Compute at compute.dtu.dk/english.

3. Hong Kong University of Science and Technology
Job Title: Faculty Positions in Electronic and Computer Engineering

Description: The Department of Electronic and Computer Engineering (ECE) at the Hong Kong University of Science and Technology invites applications for tenure-track faculty positions at Professor, Associate Professor and Assistant Professor ranks. The department consists of a large number of faculty conducting research in cutting-edge technologies such as biomedical data science, biomedical imaging/devices, quantum technology, smart cities, big data, autonomous systems, Internet of Things, and beyond 5G wireless networks in a wide scope of fields including biomedical engineering, solid-state electronics and photonics; integrated circuits and systems; control and robotic systems; data science and AI; and wireless communications and networking. Applications including 1) a cover letter, 2) full curriculum vitae and a list of publications, 3) names of five referees, and 4) a summary of research proposal and teaching statement should be submitted via the HKUST recruitment system: https://facrecruit.hkust.edu.hk/. The applicants should first sign up to create a personal account. Applications are accepted at any time and considered on a rolling basis.

4. University of California, Santa Cruz

Job Title: Faculty Positions in Computer Science and Engineering, and Electronic and Computer Engineering

The UCSC Department of Computer Science and Engineering and Department of Electrical and Computer Engineering are each hiring an Assistant Professor to start in Fall 2022. The Baskin School of Engineering at UC Santa Cruz is a member of the AAU, an association of the top research universities in the U.S. Our school has nationally and internationally known researchers in many areas, including theoretical computer science, programming languages, security, distributed systems, storage systems, computer architectures, machine learning, natural language processing, AI, data science, vision, and networking. UCSC is home to many centers and research institutes including the UCSC Genomics Institute, the W.M. Keck Center for Nanoscale Optofluidics, the Center for Molecular Biology of RNA, and the Cyber-Physical Systems Research Center. Nestled in a redwood forest above the city of Santa Cruz, our beautiful campus has a long history of embracing groundbreaking interdisciplinary work. Of the ten UC campuses, our campus is the nearest to Silicon Valley and has close research ties with the local computer industry. Our proximity to Silicon Valley, and our satellite campus there, afford opportunities and avenues for collaboration with researchers working in the many research and development labs in Silicon Valley, as well as with the other San Francisco Bay Area universities.

CSE: Hardware design, computer architecture, and embedded systems
https://recruit.ucsc.edu/JPF01163

ECE: Digital Hardware Electronics
https://recruit.ucsc.edu/JPF01166

If you have any questions, please contact mrg@ucsc.edu.

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