Association for Computing Machinery

Special Interest Group Design Automation
The resource for EDA Professionals

Special Interest Group on Design Automation

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SIGDA - The Resource for EDA Professionals

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Chair's New Year's Greetings

Dear Members of ACM SIGDA,

After two years of the COVID-19 pandemic, the world is slowly returning to a new normal. In the Design Automation Conference (DAC) held in San Francisco last month, more than a thousand engineers, scholars, and students gathered in person for the first time in the last two and half years. They presented research ideas, exchanged industrial and societal information, and discussed collaboration opportunities. The only notable difference was probably that everyone was wearing a mask.

As the world reopened from the pandemic, SIGDA elected its new executive committee (EC) in the summer of 2021. Like its predecessors, the new EC is responsible for all regular operations of SIGDA, including conferences, publications and media, educational and technical activities, awards, and members' benefits. Understandably, the COVID-19 pandemic has brought numerous unprecedented challenges that the current EC, and the whole SIGDA in general, are facing: disrupted international travels, unpredictable outbreaks of local epidemics, and lack of efficient and effective communications among our members, to name a few. Fortunately, the volunteers of SIGDA and the whole society at large have accumulated extensive experience in overcoming these challenges: the successful in-person DAC last month was just a

Messages from the EiCs

Dear ACM/SIGDA members,

Happy New Year! We are excited to present to you January E-Newsletter on the first day of 2022. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from the upcoming conferences and hot research topics to technical news and activities from our community. Get involved and contact us if you want to contribute an article or announcement.

Debjit Sinha, Keni Qiu,
Editors-in-Chief,
SIGDA E-News

SIGDA EC

Yiran Chen,
Chair

Sudeep Pasricha,
Vice Chair and Conference Chair

X. Sharon Hu
Past chair

perfect example.

Building on these experiences, the new EC has been working tirelessly with our volunteers and the whole society to meet these challenges and prepare for the era after the pandemic. A new "Who's Who" column of the SIGDA website (https://www.sigda.org/whos-who/) has been launched so that we'd still be able to learn about those active young researchers and scholars all over the world. A new version of ACM/SIGDA E-Newsletter is in the works, among many initiatives that are being planned. I am very proud of how our members, volunteers, and SIGDA leadership team have persevered through the challenging times and have also been delighted to witness the remarkable progress and achievements we have made in the past year. With this message we not only celebrate a successful 2021 with you, but also look forward to sharing some big goals and ideas soon! Our fellows will get in touch with you in the new year about our new plans and initiatives.

My warmest wishes to all the SIGDA members and their families for a healthy, restorative and productive 2022!

Yiran Chen

Chair of ACM SIGDA

SIGDA News

1. TSMC, Sony to Partner in $7B Fab in Japan
Taiwan Semiconductor Manufacturing Co. (TSMC) and Sony will join as investors in a chip facility in Japan to address strong demand for specialty technologies at the 28nm and 22nm process nodes, the companies said in a joint statement.
2. IBM, Samsung Unveil VTFET to Extend Moore's Law
IBM and Samsung Electronics claimed a breakthrough in semiconductor design based on a new IBM's architecture touted as enabling an 85-percent reduction in power consumption.
3. Advanced Cellular ASIC To Enable Satellite to Mobile Network
U.K. custom design house Ensilica has announced it is developing the cellular ASIC that will enable AST SpaceMobile's planned space-based cellular broadband network.
4. Synthetic Quantum Systems Help Solve Complex Real-World Applications

Simulation using synthetic quantum systems is a potential tool for addressing challenging NP-Hard problems (non-deterministic polynomial-time hardness), which is a task where traditional numerical approaches frequently fail.

5. Startup Mimics Human Eye By Adding Processing to Pixels

An early-stage company spun out of Johns Hopkins University wants to make machine vision more like human vision by adding memory and computing to each sensor pixel. Oculi is developing products for gesture recognition and eye tracking in consumer AR/VR systems. Other applications include smart city infrastructure and eventually, automotive vision sensing.

6. Neuromorphic Developers Partner to Integrate Sensor, Processor

SynSense and Prophesee are partnering to develop a single-chip, event-based image sensor integrating Prophesee's Metavision image sensor with Synsense's DYNAP-CNN neuromorphic processor. The companies will collaborate on design, development, manufacture and commercialization of the combined sensor-processor, aiming to produce ultra-low power sensors that are both small and inexpensive.

7. Optical Chip Solves Hardest Math Problems Faster than GPUs

Optical computing startup Lightelligence has demonstrated a silicon photonics accelerator running the Ising problem more than 100 times faster than a typical GPU setup.

8. DoD Shifts Gears, Goes Multi-Cloud

A growing list of large companies have adopted a "multi-cloud" strategy as a way of avoiding vendor lock-in. After years of legal maneuvering and procurement shenanigans, the Pentagon has at last settled on a similar approach as it seeks to drag its sprawling enterprise into the 21st century.

What Is

What is Logic Locking

Ozgur Sinanoglu
Professor, Engineering Division, New York University (NYU) Abu Dhabi
Director, Center of Cyber Security, NYU Abu Dhabi

Logic locking is a chip design netlist modification operation performed in software to enable certain features in hardware [1].

Ying Wang,
AE for Technical activities

Paper Deadlines

DAC'22 – Design Automation Conference
San Francisco, CA
Engineering Tracks Deadline: Jan. 17, 2022
July 10 - 14, 2022
http://www.dac.com/

FCCM' 22 - IEEE International Symposium On Field-Programmable Custom Computing Machines
New York
Deadline: Jan 10, 2022
(Abstracts due: Jan 3, 2022)
May 15 – 18, 2022
https://www.fccm.org/

MDTS'22 – IEEE Microelectronics Design & Test Symposium
Albany, NY
Deadline: Feb 28, 2022
May 23 - 25, 2022
http://natw.ieee.org

ISVLSI'22 – IEEE Computer Society Annual Symposium on VLSI
Cyprus
Deadline: Mar 4, 2022
July 6 - 8, 2022
http://www.ieee-isvlsi.org

VLSI-SoC'22 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Patras, Greece

Specifically, the design is modified to add new inputs that expect a "logic locking key" to be applied. Only when the correct key, which is the designer's secret, is applied from these new inputs, the logic-locked design becomes functionally equivalent to the design prior to locking. Post-fabrication, the secret key that drives these new inputs must be loaded on every chip which stores it in a non-volatile secure memory, a step referred to as the "chip activation step;" any chip that circumvents this step ends up remaining locked, i.e., non-functional.

There is apparently an implementation cost (increased area and power consumption; and performance penalty if critical paths are touched) for logic locking, so why do it? With more and more chip design companies going fabless, i.e., outsourcing fabrication to third party chip foundries [2], there is an increasing concern about the trustworthiness of the chip supply chain. A reverse engineer who analyzes the chip blueprint that the fab has full access to understand the chip's functionality and/or copy and pirate the chip or one of its critical blocks (aka intellectual property (IP) piracy), a rogue person in the chip fab tampering with the chip design to inject stealthy circuitry to launch some malicious attack when the chips are functional in the field (aka hardware Trojans), a fab running extra shifts to overproduce chips and make extra profits by selling them in gray market (overproduction) are concerns for chip design companies or government agencies today [3]. Logic locking enforces the authorized use of chips, preventing overproduction. Furthermore, without the knowledge of the secret key, anyone who tries to reverse engineer the logic-locked chip blueprint fails to fully understand the functionality of the chip or one of its security-critical blocks, incapable of pirating the design or inserting meaningful Trojans.

Depending on the application where the chips are to be used, or the critical blocks that require IP protection, and the power-performance-area impact that can be tolerated, logic locking can be applied in a targeted fashion. It can be applied on "innovative and/or security-critical" hardware blocks in the chip and/or the locations in the chip that would cripple the chip functionality more effectively [4].

Obviously, the entire defense depends on the secrecy of the logic locking key, as once it has been retrieved, logic locking can easily be circumvented. The "attacks on logic locking" therefore aim to retrieve the secret key to unlock or de-obfuscate a logic-locked design/chip. The chip foundry has full access to the chip blueprint, which contains all the information about the design netlist (aka

Deadline: April 25, 2022
(Abstracts due: April 18, 2022)
Oct 3 - 5, 2022
http://www.vlsi-soc.com

Upcoming Conferences

ASP-DAC'22 - Asia and South Pacific Design Automation Conference
Virtual Conference
Jan 17-20, 2022
http://www.aspdac.com

ISSCC'22 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Feb 20-24, 2022
http://isscc.org

VLSID'22 – International Conference on VLSI Design & International Conference on Embedded Systems
Virtual Conference
Feb 19 - 23, 2022
http://embeddedandvlsidesignconference.org/

FPGA'22 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Monterey, CA
Feb 27 - Mar 1, 2022
http://www.isfpga.org

DATE'22 - Design Automation and Test in Europe
Antwerp, Belgium, and online
Mar 14 - 23, 2022

the logic-locked design). Furthermore, depending on the market that the chips are targeted for, a working chip (with the key already stored in it) can be obtained from the market, enabling the generation of input-output pairs from a logic-locked chip. The locked design netlist and the working chip are resources for an adversary to launch an attack on the logic locking defense and retrieve the key [5]. The locked design netlist can be simulated (with the key input unknown) and the working chip can be used to prune away the incorrect keys. Machine learning methods can empower the simulations to develop more effective attacks on logic locking [6]. A strong logic locking defense is one that can thwart such attacks and keep its secret key protected [7].

An adversary may also utilize targeted probing of live signals on the chip to directly read out the secret key, but such attacks are quite impractical for chips fabricated at advanced technology nodes. Furthermore, there are simple packaging-based solutions to shield chips from probing [8].

Logic locking, when implemented properly, is a proactive and strong defense at chip designers' disposal in mitigating chip supply chain vulnerabilities such as Trojans, IP piracy, and chip overbuilding.

References

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http://www.date-conference.com

ISPD’22 – ACM Int’l Symposium on Physical Design
Banff, Alberta, Canada
Mar 27 - 30, 2022
http://www.ispd.cc

ISQED'22 - Int'l Symposium on Quality Electronic Design
California
April 6 - 8, 2022
http://www.isqed.org

RTAS'22 - IEEE Real-Time and Embedded Technology and Applications Symposium
Milano, Italy
May 4 - 6, 2022
http://2022.rtas.org

ISCA’22 – Int’l Symposium on Computer Architecture
New York City, USA
June 11-15, 2022
https://iscaconf.org/isca2022/

ISCAS'22 – IEEE Int'l Symposium on Circuits and Systems
Austin, TX
May 28 - June 1, 2022
http://iscas2022.org

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SIGDA Awards

1. Student Research Competition@ICCAD 2021

- **Undergraduate category (8 participants in total):**

(1) **1st place:** Zizheng Guo, Peking University (Presentation Title: Accelerating Static Timing Analysis with Parallel and Heterogeneous Computing)
(2) **2nd place:** Cynthia Chen, California Institute of Technology (Presentation Title: Optimizing Quantum Circuit Synthesis for Permutations on Limited Connectivity Topologies)
(3) **3rd place:** Yu Qian, Zhejiang University (Presentation Title: Energy-Aware Designs of Ferroelectric Ternary Content Addressable Memory)

- **Graduate category (22 participants in total):**

(1) **1st place:** Xiaofan Zhang, UIUC (Presentation Title: Bridge the Hardware-Software Gap: Exploring End-to-End Design Flows for Building Efficient AI Systems)
(2) **2nd place:** Sanmitra Banerjee, Duke University (Presentation Title: Optimizing Emerging AI Accelerators under Random Uncertainties)
(3) **3rd place:** Qi Sun, Chinese University of Hong Kong (Presentation Title: Fast and Efficient Deployment of Deep Learning Algorithms via Learning-based Methods)

2. CADathlon@ICCAD 2021

1st Place Team: iDEA-01, Xueyan Zhao and Haitong Huang
2nd Place Team: Whatever, Shiju Lin and Jinwei Liu

3. University Demonstration @ DAC 2021

- **First place:**
  Demo 1.2: Hardware/Software Co-Design Frameworks for Deep Learning Accelerators
  Weiwen Jiang, Lei Yang, Zheyu Yan, Qing Lu, Jingtong Hu and Yiyu Shi
- **Second place:**
  Demo 2.1: Experimental Demonstration of STT-MRAM based Nonvolatile Instantly On/Off Systems for Low Power IoT Applications
  Yueting Li, Wang Kang, Kunyu Zhou, Keni Qiu and Weisheng Zhao
- **Third place:**
  Demo 2.3: PACT: An Extensible Parallel Thermal Simulator for Emerging Integration and Cooling Technologies
  Zihao Yuan, Prachi Shukla, Sofiane Chetoui, Carlton Knox, Sean Nemtzow, Sherief Reda and Ayse Coskun

SIGDA Partner Journal: ACM Transactions on Design Automation of Electronic Systems

1. ACM TODAES announces the introduction of the Distinguished Review Board

Reviewers who consistently return timely and quality reviews provide invaluable services to ACM Transactions on Design Automation of Electronic Systems (TODAES) as well as to the community. To acknowledge such reviewers' contributions, TODAES will formally recognize such reviewers by establishing the **ACM TODAES Distinguished Reviewer Board**. The Distinguished Reviewer Board will be shown on TODAES webpage and will also be flagged within the Manuscript Central system.

Criteria and process:

- A Distinguished Reviewer must have reviewed 3 or more distinct papers in a 12 month period.
- A Distinguished Reviewer returns all the reviews on time.
- The reviewer has been rated by the inviting AEs to have 4 or above score (based on the quality of the reviews).
- The Distinguished Reviewer Board will go live in January 2022, and will be updated every three months.

If you are interested in being considered as a Distinguished Review, please fill the form at https://docs.google.com/forms/d/e/1FAIpQLScSOiAK5KEGP9bMLw5Rrmph9SPOYdkLtIA_ECO777n2bGu0PA/viewform?usp=sf_link.

2. TODAES Rookie Author of the Year (RAY) Award

ACM Transactions on Design Automation of Electronic Systems (TODAES) is excited to announce the introduction of a brand new award: TODAES Rookie Author of the Year (RAY) Award. This newly introduced award aims to highlight the achievement of junior researchers in the Design and Design Automation of Electronic Systems field. Specifically, the award recognizes an author whose first-ever peer-reviewed journal paper as a lead author is published in ACM TODAES.

The lead author of a paper refers to the author who made the most contribution to the submission. Since people may adopt different ways to order the authors, any nomination for the RAY Award must make it clear that the nominee is the lead author. If two authors satisfy this requirement (meaning that they made equal contributions and both are rookie authors), both can receive the RAY award.

We are now seeking nominations for the inaugural 2022 TODAES RAY Award. The nomination deadline is February 15, 2022. All papers published in the ACM TODAES between January 2021 and December 2021 are eligible. The RAY award will be selected based on originality, timeliness, potential impact and overall quality. The RAY award will be announced and recognized during the 2022 Design Automation Conference, San Francisco, CA.

A nomination should include the following material:

- Name and email of the nominator
- Title and author list of the paper, and the issue in which the paper was published
- Confirmation that the paper is the very first peer-reviewed journal publication in ACM or IEEE where the nominee is the lead author.
- A brief supporting statement of no more than 150 words.
- A PDF copy of the paper

Submit the nomination by February 15, 2022 via e-mail to Matthew Morrison, Managing Editor of TODAES, at matt.morrison@nd.edu. No self-nomination is allowed.

3. Call for Submissions - ACM TODAES Special Issue on Machine Learning for CAD / EDA

Advances in machine learning (ML) over the past half-dozen years have revolutionized the effectiveness of ML for a variety of

applications. However, design processes present challenges that require parallel advances in ML and CAD as compared to traditional ML applications such as image classification.

This special issue seeks original submission on ML applications to the entire design flow – including ML applications to validation and test. The application of machine learning to mask preparation and layout generation are topics which are seeing very active research recently. ML is also being applied to improve the robustness of integrated circuits and systems. Power and thermal management are probably the most important limiting factors for ICs today - ML-based techniques are being explored to address this bottleneck. All these topics, as well as further potential topics are of interest to this special issue. In addition to submissions from academia, submissions from industry are much welcome.

Important Dates
Submissions deadline: February 15, 2022
First-round review decisions: April 15, 2022
Deadline for revision submissions: May 15, 2022
Notification of final decisions: June 15, 2022
Tentative publication: Summer 2022

Submission Information
Authors are encouraged to submit high-quality original research contributions. Please clearly identify the additional material from any original conference or workshop paper in your submitted manuscript.

Submissions should be made through the ACM TODAES submission site (http://mc.manuscriptcentral.com/todaes) and formatted according to TODAES author guidelines at: https://dl.acm.org/journal/todaes/author-guidelines. Select the paper type “Special Issue on Machine Learning for CAD/EDA.”

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