

4 June 2021, Vol. 51, No. 6

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Comments from the Editors

Dear ACM/SIGDA members,

We are excited to present to you June E-Newsletter.

First of all, we would like to share with you an important news in our community. Recognizing the importance of diversity and ethics, SIGDA Executive Committee (EC) has approved the addition of a new position, i.e., Diversity and Ethics Chair. Please consider nominating qualified volunteers as candidates for this position. Self-nominations are also welcome. Please kindly refer to the Call for Nominations column for more details.

We still encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from the upcoming conferences and hot research topics to technical news and activities from our community. Get involved and contact us if you want to contribute an article or announcement.

The newsletter is evolving. Please let us know what you think.

Happy reading!

[Debjit Sinha](#), Keni Qiu, Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit <http://www.acm.org/renew> or call

between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or 1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org.

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Rajsaktish Sankaranarayanan, E-Newsletter Associate Editor for SIGDA Researcher spotlight column

Xin Zhao, E-Newsletter Associate Editor for SIGDA Paper submission deadline column

Ying Wang, E-Newsletter Associate Editor for SIGDA Technical activities column

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SIGDA News

(1) "Apple vs. Huawei: Decoupled Economies, Tech & Supply Chains"

<https://www.eetimes.com/apple-vs-huawei-decoupled-economies-tech-supply-chains/>

An accelerated U.S. vs. China trade war has elevated “decoupling” into a trendy buzzword to describe the possibility of a breakup between two of the world’s most powerful economies.

(2) "IBM Unveils World’s First 2 nm Chip"

<https://www.eetimes.com/ibm-unveils-worlds-first-2-nm-chip/>

IBM has unveiled the world’s first 2 nm chip, built at its R&D facility in Albany, New York. The test chip features gate-all-around transistors built with IBM’s nanosheet technology. Overall, IBM says the new process technology will enable 2 nm chips to achieve 45% higher performance or 75% lower power consumption than state-of-the-art 7 nm chips in production today.

(3) "Qualcomm Aims 10-Gbps 5G at Laptops, PCs"

<https://www.eetimes.com/qualcomm-aims-10-gbps-5g-at-laptops-pcs/>

Qualcomm has unveiled reference designs targeting 5G-enabled M.2 cards that it hopes will be embedded in a range of laptops, PCs, tablets and routers as well as gaming and other mobile broadband devices.

(4) "Multi-Node Quantum Network on the Horizon"

<https://www.eetimes.com/multi-node-quantum-network-on-the-horizon/>

Researchers at the Dutch QuTech research center in Delft have demonstrated a multi-node quantum network capable of connecting three quantum processors, or ‘qubits’ .

(5) "TSMC’s Zhang: Automotive is Going HPC"

<https://www.eetimes.com/tsmcs-zhang-automotive-is-going-hpc/>

Among the new process nodes introduced by Taiwan Semiconductor Manufacturing Co. at its 2021 Virtual Technology Symposium was N5A, which the company said is “aimed at satisfying the growing demand for computing power in newer and more intensive automotive applications such as

AI-enabled driver assistance and the digitization of vehicle cockpits.”

(6) "AI Drives Renewed Interest in PIM"

[\[https://www.eetimes.com/ai-drives-renewed-interest-in-pim/\]](https://www.eetimes.com/ai-drives-renewed-interest-in-pim/)

The ever-increasing demands of artificial intelligence (AI) mean concepts for memory that have been around for decades are getting renewed attention, and Samsung Electronics Co., Ltd.’ s recent announcement of a high bandwidth memory (HBM) integrated with AI processing power is good example.

(7) "Arm Upgrades Its Entire PC And Mobile Portfolio"

[\[https://www.eetimes.com/arm-upgrades-its-entire-pc-and-mobile-portfolio/\]](https://www.eetimes.com/arm-upgrades-its-entire-pc-and-mobile-portfolio/)

In its largest IP product release ever, Arm released complete families of CPU, GPU, DSU, and interconnect IP as it continues to sync up releases across product lines to what it calls “Total Compute solutions.” In fact, the only major computing core family that did not receive an update with this release is the newest family of products, the Ethos NPUs for machine learning acceleration.

(8) "What to Look For at the VLSI Technology Symposium"

[\[https://www.eetimes.com/what-to-look-for-at-the-vlsi-technology-symposium/\]](https://www.eetimes.com/what-to-look-for-at-the-vlsi-technology-symposium/)

The VLSI 2021 Symposia (plural, since there’ s a semiconductor technology track and a circuits & systems track) will be a virtual event held the week of June 12. In normal times, VLSI alternates between Hawaii and Japan. This year’ s “location” is Japan.

(9) "Modeling Battery Designs via Quantum Computers"

[\[https://www.eetimes.com/modeling-battery-designs-via-quantum-computers/\]](https://www.eetimes.com/modeling-battery-designs-via-quantum-computers/)

The prodigious potential of quantum computing is being applied to a critical energy storage problem: Improving battery simulation models that could help accelerate research into safer, more efficient energy storage along with new battery materials for electric vehicle and other consumer applications.

(10) "DRAM Destined to be 3D"

[\[https://www.eetimes.com/dram-destined-to-be-3d/\]](https://www.eetimes.com/dram-destined-to-be-3d/)

It may take a few years, but DRAM is likely to follow the footsteps of NAND and go 3D, which means it will need new manufacturing equipment and materials to do it cost-effectively.

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Paper Submission Deadlines

ICCD’ 21 – IEEE Int’ l Conference on Computer Design

Virtual Conference

Deadline: June 11, 2021

Oct 24-27, 2021

<http://www.iccd-conf.com>

HiPC’21 – IEEE Int’l Conference on High Performance Computing, Data, And Analytics

Bangalore, India

Deadline: June 11, 2021 (Abstracts due: June 4, 2021)

Dec 17-20, 2021

<http://www.hipc.org>

BioCAS'21 – Biomedical Circuits and Systems Conference
Berlin, Germany
Deadline: June 13, 2021
Oct 7-9, 2021
<https://2021.ieee-biocas.org/>

BodyNets'21 – Int'l Conference on Body Area Networks
Virtual Conference
Deadline: June 16, 2021
Oct 25-26, 2021
<http://www.bodynets.org>

iSES' 21 – IEEE Int'l Symposium on Smart Electronic Systems
Jaipur, India
Deadline: June 28, 2021
Dec 20-22, 2021
<http://www.ieee-ises.org>

FPT'21 - Int'l Conference on Field-Programmable Technology
Auckland, New Zealand
Deadline: Jul 19, 2021 (Abstracts due: Jul 12, 2021)
Dec 6-10, 2021
<http://icfpt.org>

DAForum'21 - SIGDA/IEEE CEDA Ph.D. Forum at DAC 2021
San Francisco, CA
Deadline: July 20, 2021
Dec 6, 2021
<https://easychair.org/cfp/daforum21>

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Upcoming Conferences and Symposia

LCTES' 21 – ACM Int'l Conference on Languages Compilers, Tools and Theory of Embedded Systems
Virtual conference
Jun 20-25, 2021
<https://pldi21.sigplan.org/home/LCTES-2021>

GLSVLSI' 21 – ACM Great Lakes Symposium on VLSI
Virtual Conference
Jun 22-25, 2021
<http://www.glsvlsi.org>

ICDCS'21 – IEEE Int'l Conference on Distributed Computing Systems
Virtual
Jul 7 - 10, 2021
<https://icdcs2021.us/>

ISVLSI' 21 – IEEE Computer Society Annual Symposium on VLSI
Tampa, Florida
Jul 7-9, 2021
<http://www.ieee-isvlsi.org>

ISED' 21 – 10th Int' l Symposium on Embedded Computing & System Design
Kollam, India
Jul 16-18, 2021
<http://isedconf.org>

IWLS'21 - International Workshop on Logic & Synthesis
Virtual conference
Jul 19-21, 2021
<https://www.iwls.org>

ISLPED' 21 – ACM/IEEE Int' l Symposium on Low Power Electronics and Design
Hybrid Zoom/Boston, MA
Jul 26-28, 2021
<http://www.islped.org>

ASYNC'21 – IEEE Int' l Symposium on Asynchronous Circuits and Systems
Virtual Conference
Sept 7-10, 2021
<http://asynsymposium.org>

PACT'21 - Int'l Conference on Parallel Architectures and Compilation Techniques
Virtual Conference
Sept 26-28, 2021
<http://www.pactconf.org>

VLSI-SoC' 21 – IFIP/IEEE Int' l Conference on Very Large Scale Integration
Virtual conference
Oct 4-8, 2021
<http://www.vlsi-soc.com>

ESWEEK'21 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)
Virtual Conference
Oct 10-15, 2021
<http://www.esweek.org>

MICRO' 21 – IEEE/ACM Int'l Symposium on Microarchitecture
Athens, Greece
Oct 16-20, 2021
<http://www.microarch.org/micro54>

ICCAD' 21 – IEEE/ACM Int' l Conference on Computer-Aided Design
Virtual Conference
Nov 1-4, 2021
<http://www.iccad.com>

DAC' 21 – Design Automation Conference
San Francisco
Dec 5–9, 2021
<http://www.dac.com/>

HOST'21 – IEEE Int' l Symposium on Hardware-Oriented Security and Trust
Washington DC
Dec 12-15, 2021
<http://www.hostsymposium.org>

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Call for Nominations - SIGDA Diversity and Ethics Chair

Recognizing the importance of diversity and ethics, SIGDA Executive Committee (EC) has approved the addition of a new position, i.e., Diversity and Ethics Chair. The duties of Diversity and Ethics Chair include the following:

- Disseminate ACM policies to SIGDA sponsored conferences and SIGDA related ACM journals
- Consult and work with ACM SIGDA sponsored conferences on issues related to diversity and ethics
- Help develop new ethics and diversity policies collected from ACM sponsored conferences
- Help enforce penalties determined by ACM COPE (Committee On Professional Ethics)

Please consider nominating qualified volunteers as candidates for this position. Self-nominations are also welcome. Submit your nomination at

https://docs.google.com/forms/d/e/1FAIpQLSfNI4Rzg8YmnjuVAm67jyfUdJlQvnI7Hy2_opSu.... The new SIGDA board (starting on July 1st, 2021) will make the final selection.

The nomination deadline is June 25th, 2021. For questions, please contact Sharon Hu, SIGDA EC Chair, at shu@nd.edu.

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SIGDA Partner Journal

1. Approximate Computing Survey Paper Published in April Issue – The ACM Transactions on Design Automation of Electronic Systems (TODAES) invited you to read a survey paper published in the April 2021, Article No.: 32 issue titled “Security Threat Analyses and Attack Models for Approximate Computing Systems: From Hardware and Micro-architecture Perspectives” (<https://doi.org/10.1145/3442380>). The article was written by Pruthvy Yellu, Landon Buell, Dongpeng Xu, and Qiaoyan Yu from the University of New Hampshire and Miguel Mark and Michel A. Kinsy from Texas A&M University. In this survey paper, they focus on the paradigm shift represented by Approximate Computing (AC) from conventional precise processing to inexact computation but still satisfying the system requirement on accuracy, and the security threats that arise from utilizing AC systems. Their work focuses on potential security vulnerabilities of AC systems, specifically existing circuit-, architecture-, and compiler-level approximate mechanisms/algorithms. They also review four unique visionary attack models, which systematically cover the attacks that build covert channels, compensate approximation errors, terminate normal error resilience mechanisms, and propagate additional errors. Finally, they present a guideline of countermeasure designs, as well as several case studies to illustrate the implementation of the suggested countermeasures.

2. Call for Papers – Special Issue on High-Level Synthesis for FPGA: Next-Generation

Technologies and Applications: The ACM Transactions on Design Automation of Electronic Systems (TODAES) invites you to submit high-quality original research contributions that will not require major revisions for the Special Issue on High-Level Synthesis for FPGA: Next-Generation Technologies and Applications. Due to the end of Dennard scaling and Moore’s law, complex hyper-pipelined processors are increasingly replaced by heterogeneous System-on-Chip (SoC) architectures with many specialized components. FPGA devices are becoming common targets for these systems since they allow fast turn-around time, field upgradability, and easy deployment of hardware/software solutions. To cope with the increasing complexity of such systems, designers need to raise the abstraction level from custom design flows to high-level approaches. High-level synthesis (HLS) is a popular method that allows designers to describe the functionality of a component at the software level and automatically generate the corresponding hardware description, reducing the gap between application and hardware designers. Since HLS has been making a great amount of progress and an increasing number of different application domains are pushing designers towards hardware acceleration, HLS is becoming a key enabling technology for FPGA design.

The application landscape for hardware acceleration is rapidly and deeply changing. Modern applications are increasingly based on machine learning that require access to huge amounts of data to extract valuable knowledge and make accurate predictions. Also, novel technologies like quantum computing are opening novel research questions on how to design accelerators for these systems (including post-quantum cryptography). The combined requirements of modern technologies and applications pose novel challenges and threats for high-level synthesis. For example, side-channel and adversarial attacks are serious threats for security and machine learning applications.

Topics:

This special issue aims at presenting the latest advances in high-level synthesis for FPGAs, focusing on the interplay with (and between) artificial intelligence and security. Topics of interest include, but are not limited to, the following:

- Use of high-level synthesis for emerging applications (e.g., AI, post-quantum cryptography)
- Use of emerging methods for high-level synthesis (e.g., machine learning for design space exploration and predictions)
- Domain-specific languages and compiler-based optimizations to specify and integrate extra-functional properties (e.g., security requirements) during high-level synthesis
- Algorithms for scheduling, binding, and controller synthesis for the co-optimization of hardware security protections
- Automatic synthesis (and protection) of near-memory computation systems
- Identification of security vulnerabilities in HLS-generated designs

Important Dates:

- Submissions deadline: 30 June 2021
- First-round review decisions: 31 August 2021
- Deadline for revision submissions: 15 October 2021
- Notification of final decisions: 31 November 2021
- Tentative publication: January/February 2022

Submissions should be made through the ACM TODAES submission site (<http://mc.manuscriptcentral.com/todaes>) and formatted according to TODAES author guidelines at: <https://dl.acm.org/journal/todaes/author-guidelines>.

For questions and further information, please contact the guest editors at:

- Christian Pilato <christian.pilato@polimi.it>
- Zhenman Fang <zhenman@sfu.ca>
- Yuko Hara-Azumi <hara@cad.ict.e.titech.ac.jp>
- Jim Hwang <jhwang@xilinx.com>

3. Call for Special Issue Proposals: TODAES invites proposals for special issues within the scope of TODAES. Special issues often focus on topics that represent emerging research trends, cross-disciplinary efforts, or significant new developments in an area. High visibility workshops and special sessions at leading conferences can be good sources for special issue proposals. Special issues typically publish 4-6 papers and should aim to attract between 15-20 submissions.

A special issue proposal should contain the following

- Title and names of the guest editors (typically 2-4 guest editors)
- Extended abstract describing the focus of the special issue, why the topic is important and timely, relevance of the proposed topic to TODAES, a brief survey of related recent publications (special issues, workshops, special sessions at conferences)
- Potential submitters as well as a strategy for getting high quality papers;
- Qualification of the guest editors
- At least one guest editor should be from industry or have significant recent industrial experience
- Tentative timeline (from call for papers to final acceptance)
- If a proposal is accepted, the timeline will be subject to negotiation and agreement with the TODAES Editor-in-Chief.

- A submitted proposal will be evaluated by the TODAES editorial board and revision may be required.

Guest editors are welcome to write an overview/survey paper about the topic but cannot be authors or co-authors of other papers in the special issue. The guest editors/ article will be reviewed.

To submit a proposal for a special issue, please email the proposal directly to Joerg Henkel, Senior Associate Editor of TODAES (joerg.henkel@kit.edu).

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Technical Activities

1. "Arm Upgrades Its Entire Portfolio of PC And Mobile IP"

With this huge announcement of new IP, Arm set a new bar for not only itself but for other IP and semiconductor companies...

[\[https://www.eetasia.com/arm-upgrades-its-entire-portfolio-of-pc-and-mobile-ip/\]](https://www.eetasia.com/arm-upgrades-its-entire-portfolio-of-pc-and-mobile-ip/)

2. "CEA-Leti Unveils World' s First Autonomous Imager For Smartphones, Smart-Home Appliances and Automobiles"

CEA-Leti today announced the world' s first autonomous imager technology that activates smartphones and small appliances through face recognition or other specific patterns...

[\[https://www.edacafe.com/nbc/articles/1/1839820/CEA-Leti-Unveils-Worlds-First-Aut...\]](https://www.edacafe.com/nbc/articles/1/1839820/CEA-Leti-Unveils-Worlds-First-Aut...)

3. "Top-15 Semiconductor Companies Register 21% YoY Growth in Q1"

The top-15 worldwide semiconductor companies have logged total sales of \$101.86 billion for 1Q21, up by 21% year-on-year...

[\[https://www.eetasia.com/top-15-semiconductor-companies-register-21-yoy-growth-in...\]](https://www.eetasia.com/top-15-semiconductor-companies-register-21-yoy-growth-in...)

4. "EV Charging Stations: Technology, Market Trends"

Electrification is one of the main macro-trends that are reshaping the world of mobility...

[\[https://www.eetimes.eu/ev-charging-stations-technology-market-trends/\]](https://www.eetimes.eu/ev-charging-stations-technology-market-trends/)

Job Openings:

1. Vanderbilt University School of Engineering, United States

Job Title: Professor of the Practice in Computer Science and Data Science

Description: The Department of Electrical Engineering and Computer Science (EECS) and Data Science Institute (DSI) at Vanderbilt University invites applicants for a professor of the practice or lecturer of computer science position with a target start date of Fall 2021. Primary responsibilities are to teach three core data science and/or computer science courses per semester for data science master's students. Courses may include lecture, lab, or directed research components. Ideal qualifications include a Ph.D. degree in computer science, data science, or a related discipline and prior teaching experience in these programs. This is a term appointment, eligible for renewal, contingent on performance. Data science programs at Vanderbilt are growing, are committed to teaching and research excellence, and include a number of professors of the practice and lecturers who are fully integrated into EECS and DSI faculty operations. Vanderbilt University has a strong institutional

commitment to recruiting and retaining an academically and culturally diverse community of faculty. Minorities, women, individuals with disabilities, and members of other underrepresented groups, in particular, are encouraged to apply. Vanderbilt is an Equal Opportunity/Affirmative Action employer. Applications should include a full CV, statement of teaching experience and interests, as well as names and email addresses of three references. Applications should be submitted on-line at: <http://apply.interfolio.com/86198> . For more information, please visit our web sites: <https://engineering.vanderbilt.edu/eecs/> and <https://www.vanderbilt.edu/datascience/>. Review of applications will begin immediately, and applications will be accepted until the position is filled. For questions regarding the position, send an email to: d.schmidt@vanderbilt.edu.

2. Shandong University, China

Job Title: Faculty Members in Theoretical and Computational Sciences

Description: Qingdao Institute for Theoretical and Computational Sciences (QiTCS; <http://www.qitcs.qd.sdu.edu.cn/>) is a newly founded research institute associated to Shandong University at Qingdao campus. QiTCS focuses on theories, methods, algorithms, software and applications in theoretical and computational chemistry, biophysics, materials, condensed matter and numerical mathematics. In each of the 5 directions there will be 2 to 3 principle investigators, each of whom may lead a group of 2 to 3 faculty members (full, associate or assistant professors), totaling up to 40 faculty members. Personnels who are skilled at software development are especially welcome. For further information, please refer to <http://www.qitcs.qd.sdu.edu.cn/>

3. The Education University of Hong Kong Hong Kong

Title: Associate/Assistant Professor of Artificial Intelligence and Educational Technology

Description: Applicants should have a doctoral degree in Computer Science, Information Technology, Artificial Intelligence or a closely related discipline, with expertise in artificial intelligence and educational technology. They should be active researchers with a growing publication record, be able to continue conducting research that attracts competitive external funding and leads to publications in leading international journals, and have post-qualification teaching experience in the tertiary education sector and commitment to high quality teaching. For the post of Associate Professor, applicants must also show the capacity for academic leadership in promoting teaching, research and community services in Hong Kong and the Asia Pacific Region. Bilingual competency in English and Chinese will be advantageous. Immediate availability is preferred. For information on the Department, please visit this website: <http://www.eduhk.hk/mit>. Salary will be commensurate with qualifications and experience. Initial appointment will be made on a fixed-term contract. Fringe benefits include contract-end gratuity, leave, medical and dental benefits, and where applicable, housing benefits. Application Forms are obtainable from (a) <http://www.eduhk.hk/hro/applyfor.htm>; or (b) the Human Resources Office, 3/F, Cho Kwai Chee Foundation Building, The Education University of Hong Kong, 10 Lo Ping Road, Tai Po, New Territories, Hong Kong. The completed Application Form, together with full CV, should be sent to the Human Resources Office by email to hro1@eduhk.hk or by post to the above address. Review of applications will start from 28 May 2021, and will continue until the post is filled. Applications which are not made in prescribed form, or incomplete, or late, or not signed, or without the required supporting documents may not be considered. Please quote the reference number of the position in the application and mark "Strictly Confidential – Job Application" on the envelope. Personal data provided by applicants will be used for recruitment and other employment-related purposes. For details of the Personal Information Collection Statement, please refer to <http://www.eduhk.hk/jobsoff/index.php?glang=en>.

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Circulation: 2,700

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