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Comments from the Editors

Dear ACM/SIGDA members,

Happy New Year 2021!

We are excited to present to you January E-Newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from the upcoming conferences and hot research topics to technical news and activities from our community. Get involved and contact us if you want to contribute an article or announcement.

The newsletter is evolving. Please let us know what you think.

Happy reading!

[Debjit Sinha](#), Keni Qiu, Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit <http://www.acm.org/renew> or call between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or

1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org.

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Ying Wang, E-Newsletter Associate Editor for SIGDA Technical activities column

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SIGDA News

(1) "Samsung Touts Superiority of Stand Alone Version of 5G"

[\[https://www.eetimes.com/samsung-touts-superiority-of-stand-alone-version-of-5g/\]](https://www.eetimes.com/samsung-touts-superiority-of-stand-alone-version-of-5g/)

Samsung and Intel are claiming a major breakthrough in the data processing capacity of 5G Stand Alone (SA) cores. The companies say they achieved 305 Gbps per server and latency capacity in a commercial network set-up.

(2) "Intel Benchmarks Neuromorphic Chip Against AI Accelerators"

[\[https://www.eetimes.com/intel-benchmarks-neuromorphic-chip-against-ai-accelerato...\]](https://www.eetimes.com/intel-benchmarks-neuromorphic-chip-against-ai-accelerato...)

At Intel Labs Day today, Intel presented a summary of performance results comparing its neuromorphic chip, Loihi, to classical computing and mainstream deep learning accelerators for the first time. The results show that while Loihi may not offer many advantages over other approaches for feed-forward neural networks, big latency and power efficiency gains can be achieved for other workloads, such as recurrent neural networks.

(3) "Intel Labs, What' s Next for Quantum Computing?"

[\[https://www.eetimes.com/intel-labs-whats-next-for-quantum-computing/\]](https://www.eetimes.com/intel-labs-whats-next-for-quantum-computing/)

At the recently held Intel Labs Day, Intel spotlighted research initiatives across multiple domains. During the discussion on Quantum Computing Intel introduced the 2nd-Gen Horse Ridge Cryogenic Quantum Control Chip.

(4) "Intel' s Xe GPUs — from Laptops to Supercomputers"

[\[https://www.eetimes.com/intels-xe-gpus-from-laptops-to-supercomputers/\]](https://www.eetimes.com/intels-xe-gpus-from-laptops-to-supercomputers/)

Having released two Xe GPUs, Intel is now officially a maker of discrete graphics processors. There is a big difference between being a participant and being a leader and with its multifaceted graphics strategy that spans from laptops for casual gamers to high-end gaming desktops and from entry-level Android games to supercomputers, Intel certainly wants to become a leader.

(5) "AWS Invests in Habana AI Training Chips"

[\[https://www.eetimes.com/aws-invests-in-habana-ai-training-chips/\]](https://www.eetimes.com/aws-invests-in-habana-ai-training-chips/)

Amazon Web Services (AWS) has invested in Habana Gaudi AI training chips for its cloud offering, a

big win for the Intel-owned startup.

(6) "Intel Teams Optane with QLC NAND"

<https://www.eetimes.com/intel-teams-optane-with-qlc-nand/>

Intel frontloaded its latest Optane product announcements with a few new flash-based offerings, even as the sale of its NAND business to SK Hynix is pending.

(7) "Low Power DRAM Can Meet Edge AI Demands"

<https://www.eetimes.com/low-power-dram-can-meet-edge-ai-demands/>

For all the chatter about high performance or emerging memories meeting the needs of artificial intelligence (AI), the enduring, legacy memories appear to have a role to play for AI devices at the edge, including older generations of low power DRAM (LPDDR).

(8) "NXP' s 4D Imaging Radars Offer Higher Latitude Resolution"

<https://www.eetimes.com/nxps-4d-imaging-radars-offer-higher-latitude-resolution/>

Radar is getting hot, especially with advancements that promise object identification/classification and higher latitude resolution — something traditional radars couldn' t do. With these new innovations, radars are emerging as the most sought-after sensor among carmakers and Tier Ones developing highly automated vehicles.

(9) "GrAI Matter Raises \$14M for Sparsity-Driven AI SoC"

<https://www.eetimes.com/grai-matter-raises-14m-for-sparsity-driven-ai-soc/#>

GrAI Matter Labs has raised \$14 million in a series A+ round of funding in order to introduce its full-scale AI SoC for edge applications early next year. GrAI Matter launched its proof-of-concept chip, GrAI One, a year ago, but the new device will be much bigger, to enable running popular vision networks such as ResNet-50.

(10) "Snapdragon Ups Ante in Photography, Mobile Gaming"

<https://www.eetimes.com/snapdragon-ups-ante-in-photography-mobile-gaming/>

Day two of the Qualcomm Snapdragon Tech Summit provided the details of Snapdragon 888. As we indicated in our previous article, Qualcomm focused technology enhancements of the new SoC on improving three key areas: the camera, gaming, and AI.

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SIGDA Local Chapter News

Event 5 of the Design Automation WebiNar (DAWN): Quantum Computing and Design Automation: Challenges and Opportunities, has been held on December 11, 2020. The hosts are Prof. Yiran Chen and Prof. Tsung-yi Ho. The webpage is at <https://duke-cei-lab.github.io/DAWN/event5/>. This event is supported by SIGDA and CEDA.

The moderator of this webinar is Prof. Anupam Chattopadhyay at NTU, Singapore. There are four invited talks.

Talk 1: Dr. Oliver Dial from IBM

General introduction on quantum computing

Quantum computation is a novel computational paradigm that is provably different from classical computers. I will briefly introduce the ideas behind their operation and the main types of quantum

computers today, and then as a specific example I will discuss in somewhat more detail the quantum computers based on superconducting Transmon qubits in use at IBM, Google, Rigetti, and many other commercial and academic quantum computing organizations.

Talk 2: Dr. Ross Duncan from Cambridge Quantum Ltd.

Compilers for NISQ computers

We live in the era of NISQ : noisy intermediate-scale quantum computers. These computers are not like the quantum computers you read about in Nielsen and Chuang. They have many limitations and pose many obstacles to the quantum programmer. I'll discuss some of these difficulties and how a compiler — specifically tket from Cambridge Quantum Computing — can help overcome these problems.

Talk 3: Dr. Carmen G. Almudever from Delft University of Technology

Structured Architecting and Benchmarking of Quantum Computers in the NISQ Era

Quantum computing is now in the so-called NISQ (Noisy Intermediate-Scale Quantum) era, in which quantum processors with a limited number of qubits and imperfect behaviour are capable to execute relatively small quantum algorithms. In order to leverage the computational power of such resource-constrained and error-prone devices, not only efficient compilation techniques are required but also optimal full-stacks need to be developed. In this talk, I will provide an overview on the compilation of quantum algorithms on NISQ devices. I will also discuss how the use of structured design space exploration methodologies could help towards the development of a cross-layer co-design framework for full-stack quantum systems that will allow for a top-bottom, bottom-up optimizations across layers and the benchmarking of quantum computers.

Talk 4: Prof. Robert Wille from Johannes Kepler University Linz, Austria

Design Automation for Quantum Computing

In order to develop proper (quantum) algorithms, dedicated design flows and tools are required. In the conventional realm, corresponding solutions are standard in the meantime. In the quantum realm, however, developments are at the beginning (although great accomplishments have been made in the recent years). In this talk, we review how methods for design automation can help in this regard. More precisely, we show how certain data-structures and procedures that are established in conventional design automation can be used to improve the simulation and verification of quantum algorithms.

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"What is" Column

What is Neuromorphic Computing?

Anup Das
Assistant Professor,
Electrical and Computer Engineering Department,
Drexel University

Neuromorphic Computing is a term coined by Carver Mead in the late 1980s describing Very Large-Scale Integration (VLSI) systems, which mimic the neuro-biological architecture of the central nervous system [1]. Neuromorphic systems are energy efficient in executing Spiking Neural Networks (SNNs), which are considered as the third generation of neural networks. SNNs use spike-based computations and bio-inspired learning algorithms in solving pattern recognition problems [2]. In an SNN, pre-synaptic neurons communicate information encoded in spike trains to post-synaptic neurons, via synapses. Performance, e.g., accuracy of an SNN model, is assessed in terms of the inter-spike interval (ISI), which is defined as inverse of the mean firing rate of neurons. Neuromorphic systems are

efficient in executing SNNs, thanks to their event-driven activation and their tile-based distributed architecture with in-place neural computations and synaptic storage [3].

In recent years, many approaches are proposed to use SNN algorithms designed for neuromorphic hardware. Examples include the liquid state machine (LSM)-based heart-rate estimation [4], spiking residual network (ResNet) architecture for ImageNet classification [5], deep learning architecture for DNA sequence analysis [6], heart-rate classification with spiking convolution architecture [7], recurrent architecture-based predictive visual pursuit [8], and spiking architecture for seizure classification using EEG data [9].

Recently, various large-scale neuromorphic platforms have been demonstrated that integrate more than 1000 neurons. In SpiNNaker [10], each ARM9 core can implement multiple neuron functionality, with the local memory serving as the synaptic storage. The SpiNNaker chip consists of 18 cores and 48 such chips are integrated on a SpiNNaker board. Chips are organized in a hexagonal topology and communicate via direct connections. TrueNorth is a million-neuron digital CMOS chip from IBM [11]. The chip has 4,096 tiles, with each tile hosting 12.75 kilobytes of local SRAM memory to store the synapses. TrueNorth uses asynchronous communication between tiles. Loihi is a 128-tile neuromorphic chip from Intel [12], with each tile having 1,024 spiking neurons and 2 Mb of SRAM to store synapses. The chip is designed in 14 nm FinFET process. There are also many other neuromorphic chips such as Neurogrid[13], BrainScaleS [14], Braindrop [15], DYNAP-SE [16], and ODIN [17]. These architectures consist of tiled arrays, with each tile integrating neurons and synapses locally.

From software perspective, several frameworks are proposed to map SNNs to neuromorphic hardware. Corelet is a proprietary tool from IBM to map SNNs to TrueNorth. PACMAN is used to map SNNs to SpiNNaker. Beside these hardware-specific tools, there are also general-purpose ones. For instance, PyCARL is used to map SNNs on Loihi, BrainScaleS, SpiNNaker, and Neurogrid by balancing the load on each tile [18]. SpiNeMap is used to map SNN-based applications to DYNAP-SE and other tile-based neuromorphic hardware [19].

On the technology front, Non-Volatile Memory (NVM) technologies such as Phase-Change Memory (PCM), Oxide-Based Resistive RAM (RRAM), Ferro-Electric RAM (FeRAM), and Spin-Transfer Torque Magnetic or Spin-Orbit-Torque RAM (STT- and SoT-MRAM) can be used to implement synapses in a neuromorphic hardware [20]. NVMs are non-volatile; they have high integration density and low power consumption; they are compatible with CMOS technology scaling.

To harness the full potential of neuromorphic computing, it is essential to co-optimize the algorithm, architecture, system software, and technology, as demonstrated recently for OxRRAM-based neuromorphic hardware [21].

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Paper Submission Deadlines

ISLPED' 21 – ACM/IEEE Int' l Symposium on Low Power Electronics and Design
Hybrid Zoom/Boston, MA
Deadline: Mar 15, 2021 (Abstract due: Mar 8, 2021)
Jul 26-28, 2021
<http://www.islped.org>

TAU' 21 – ACM Int' l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems
Monterey, CA
Deadline: Jan 9, 2021
Apr 8-9, 2021
<http://www.tauworkshop.com>

FCCM' 21 - The 29th IEEE International Symposium On Field-Programmable Custom Computing Machines
Orlando, FL
Deadline: Jan 11, 2021 (Abstracts due: Jan 4, 2021)

May 9 – May 12, 2021
<https://www.fccm.org/>

DAC' 21 – Design Automation Conference
San Francisco

Deadline: Jan 20, 2021 (Designer Track, Embedded Track, and IP Track), Mar 5, 2021 (Late Breaking Results)

Jul 11–15, 2021
<http://www.dac.com/>

GLSVLSI' 21 – ACM Great Lakes Symposium on VLSI
Virtual Conference
Jun 22-25, 2021
<http://www.glsvlsi.org>

ISVLSI' 21 – IEEE Computer Society Annual Symposium on VLSI
Tampa, Florida
Deadline: Feb 21, 2021
Jul 7-9, 2021
<http://www.eng.ucy.ac.cy/theocharides/isvlsi21/>

LCTES' 21 – ACM Int' l Conference on Languages Compilers, Tools and Theory of Embedded Systems
Virtual conference
Deadline: Mar 1, 2021
Jun 20-25, 2021
<https://pldi21.sigplan.org/home/LCTES-2021>

MDTS'21 – IEEE Microelectronics Design & Test Symposium
Virtual workshop
Deadline: Mar 30, 2021
May 19-21, 2021
<http://natw.ieee.org>

ESWEEK'21 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)
Virtual Conference
Deadline: Apr 9, 2021 (Abstracts due: Apr 2, 2021)
Oct 10-15, 2021
<http://www.esweek.org>

ISED' 21 – 10th Int' l Symposium on Embedded Computing & System Design
Kollam, India
Deadline: Apr 25, 2021
Jul 16-18, 2021
<http://isedconf.org>

VLSI-Soc' 21 – IFIP/IEEE Int' l Conference on Very Large Scale Integration
Singapore
Deadline: Apr 26, 2021 (Abstracts due: Apr 19, 2021)
Oct 5-7, 2021
<http://www.vlsi-soc.com>

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Upcoming Conferences and Symposia

ASP-DAC'21 - Asia and South Pacific Design Automation Conference
Virtual Conference
Jan 18-21, 2021
<http://www.aspdac.com>

HiPEAC'21: Int'l Conference on High Performance Embedded Architectures & Compilers
Budapest, Hungary
Jan 18-20, 2021
<https://www.hipeac.net/2021/budapest>

DATE'21 - Design Automation and Test in Europe
Grenoble, France
Feb 1-5, 2021
<http://www.date-conference.com>

ISSCC'21 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Feb 14-18, 2021
<http://isscc.org>

VLSID'21 – International Conference on VLSI Design & International Conference on Embedded Systems
Virtual Conference
Feb 20-24, 2021
<http://embeddedandvlsidesignconference.org/>

FPGA' 21 – ACM/SIGDA Int' l Symposium on Field-Programmable Gate Arrays
Virtual Conference
Feb 28-Mar 2, 2021
<http://www.isfpga.org>

ISPD' 21 – ACM Int' l Symposium on Physical Design
Mar 21-24, 2021
<http://www.ispd.cc>

ISQED'21 - Int'l Symposium on Quality Electronic Design
Virtual Conference
Apr 7-8, 2021
<http://www.isqed.org>

RTAS'21 – 27th IEEE Real-Time and Embedded Technology and Applications Symposium
Nashville, USA
May 18-21, 2021
<http://2021.rtas.org>

ISCA' 21 – Int' l Symposium on Computer Architecture
Valencia, Spain
May 22–26, 2021
<https://iscaconf.org/isca2021/>

DAC' 21 – Design Automation Conference
San Francisco
Jul 11-15, 2021
<http://www.dac.com/>

SIGDA Partner Journal

1. Call for Special Issues Proposals – The ACM Transactions on Design Automation of Electronic Systems (TODAES) is a premier ACM journal in design and automation of electronic systems. TODAES invites proposals for special issues within the scope of TODAES. Special issues often focus on topics that represent emerging research trends, cross-disciplinary efforts, or significant new developments in an area. High visibility workshops and special sessions at leading conferences can be good sources for special issue proposals. Special issues typically publish 4-6 papers and should aim to attract between 15-20 submissions.

A special issue proposal should contain the following

- Title and names of the guest editors (typically 2-4 guest editors)
- Extended abstract describing the focus of the special issue, why the topic is important and timely, relevance of the proposed topic to TODAES, a brief survey of related recent publications (special issues, workshops, special sessions at conferences)
- Potential submitters as well as a strategy for getting high quality papers;
- Qualification of the guest editors
- At least one guest editor should be from industry or have significant recent industrial experience
- Tentative timeline (from call for papers to final acceptance)
- If a proposal is accepted, the timeline will be subject to negotiation and agreement with the TODAES Editor-in-Chief.

A submitted proposal will be evaluated by the TODAES editorial board and revision may be required.

Guest editors are welcome to write an overview/survey paper about the topic but cannot be authors or co-authors of other papers in the special issue. The guest editors/ article will be reviewed.

To submit a proposal for a special issue, please email the proposal directly to Joerg Henkel, Senior Associate Editor of TODAES at joerg.henkel@kit.edu

2. Best Paper Award Nominations - TODAES is seeking nominations for the 2021 TODAES Best Paper Award. The nomination deadline is February 15, 2021. All papers published in the ACM TODAES between January 2019 and December 2020 are eligible. The best paper will be selected based on originality, timeliness, potential impact and overall quality. The award will be announced and recognized during the 2021 Design Automation Conference, July 11-15, 2021, San Francisco, CA.

A nomination should include the following material:

- Name and email of the nominator
- Title and author list of the paper, and the issue in which the paper was published
- A brief supporting statement of no more than 150 words
- A PDF copy of the paper

Submit the nomination by email to Matthew Morrison, Managing Editor of TODAES, at matt.morrison@nd.edu.

Both nominations by peers and self-nominations are welcome.

Technical Activities

1. "The Importance of SiC Semiconductors for Energy Efficiency"

The development of new technologies in power electronics has directed the industrial market towards other resources to optimize energy efficiency. Silicon and germanium are two of the main materials used today to produce semiconductors. The limited development in terms of losses and switching speed has directed technology towards new wide-bandgap resources such as silicon carbide (SiC)...

[\[https://www.eetimes.eu/the-importance-of-sic-semiconductors-for-energy-efficienc...\]](https://www.eetimes.eu/the-importance-of-sic-semiconductors-for-energy-efficienc...)

2. "5G is Booming! Safety Should Be the Top Priority"

5G commercialization has been gradually deployed around the globe, and its high speed, great bandwidth and low latency will contribute hugely to the development and application of V2X...

[\[https://www.eetasia.com/5g-is-booming-safety-should-be-the-top-priority/\]](https://www.eetasia.com/5g-is-booming-safety-should-be-the-top-priority/)

3. "Teardown: Tesla's Hardware Retrofits for Model 3"

Tesla Model 3 is a three-year old vehicle. But With software updates and a hardware swap, Tesla is promising to make it ready for full self-driving future...

[\[https://www.eetasia.com/teslas-hardware-retrofits-for-model-3/\]](https://www.eetasia.com/teslas-hardware-retrofits-for-model-3/)

4. "CEA-Leti Papers at IEDM 2020 Highlight Progress in Overcoming Challenges to Making GaN Energy-Saving, Power-Electronics Devices"

Gallium Nitride Seen as Highly Efficient Replacement for Silicon In Wide Range of Consumer and Industrial Uses...

[\[https://www.edacafe.com/nbc/articles/1/1804616/CEA-Leti-Papers-IEDM-2020-Highlig...\]](https://www.edacafe.com/nbc/articles/1/1804616/CEA-Leti-Papers-IEDM-2020-Highlig...)

Job Openings:

1. Microelectronics Thrust, Hong Kong University of Science and Technology (GZ), China

Job Title: Tenured/Tenure-Track Faculty Positions

Description: Microelectronics Thrust is an academic department in the Guangzhou campus and focuses on integrating novel electronic and photonic devices into circuits, architecting systems, and automating designs and optimizations. Microelectronics Thrust has multiple tenured/tenure-track positions at the ranks of Assistant Professor, Associate Professor, and Professor. Applicants should have a PhD degree and research in areas such as electronic design automation; photonic design automation; processor, memory, and storage system architecture; reconfigurable architecture; interconnection network; multiprocessor system; neural computing; approximate computing; quantum computing; hardware-software co-design; compilation techniques; operating system; system software; power management; thermal management; embedded system; system-on-chip; system-in-package; integrated photonic circuit; RF/mm-Wave/terahertz technology; modeling and simulation technology; emerging technology. English is the instruction and administration medium at the Guangzhou campus, and a good command of written and spoken English is required.

Applications should be sent to gzrecruitFUN@ust.hk and cc to Prof. Jiang Xu at jiang.xu@ust.hk together with (i) a CV including education, honors, publications, projects, teaching experience, etc.; (ii) a statement and future plan on research and teaching; (iii) three to five representative publications in PDF in the last five years; (iv) the contact information of three referees; and (v) for Associate/Full Professor applications, records of teaching performance.

2. Vanderbilt University Department of Electrical Engineering and Computer Science, United States

Job Title: Faculty Positions in Computer Science

Description: The Department of Electrical Engineering and Computer Science (EECS) is launching a multi-year faculty recruitment and hiring process in Computer Science for 20 tenure-track positions at the Assistant, Associate, and Full Professor levels, but with preference at early-career appointments. This year, the initiative will support at least six new faculty positions. Destination-CS is part of the university's recently launched Destination Vanderbilt, a \$100 million university excellence initiative to recruit new faculty. Over the next two to four years, the university will leverage the investment to recruit approximately 60 faculty who are leaders and rising stars in their fields. We seek exceptional candidates in broadly defined areas of computer science that enhance our research strengths in areas that align with the following investment and growth priorities of the Vanderbilt University School of Engineering (<http://vu.edu/destination-cs>): Autonomous and Intelligent Human-AI-Machine Systems and Urban Environments; Cybersecurity and Resilience; Computing and AI for Health, Medicine, and Surgery; Design of Next Generation Systems, Structures, Materials, and Manufacturing. Applications should be submitted on-line at: <http://apply.interfolio.com/80624>. For more information, please visit our web site: <http://vu.edu/destination-cs>. Applications will be reviewed on a rolling basis beginning December 15, 2020 with interviews beginning January 1, 2021. For full consideration, application materials must be received by January 31, 2021.

3. University of Texas Austin Department of Computer Science, United States

Job Title: Assistant/Associate/Full Professor of Computer Science

Description: The Department of Computer Science of the University of Texas at Austin is recruiting for full-time, non-tenure track faculty (Lecturer, Assistant Professor of Instruction, Associate Professor of Instruction, Professor of Instruction) positions. The department is consistently ranked among the top computer science programs in the nation and is a core unit of Texas Computing, <https://computing.utexas.edu>. It is renowned for its collegial environment that fosters innovation and collaboration. We value undergraduate education and have a committed group of highly effective educators. The department is committed to building a diverse faculty, and we are interested in candidates who will contribute to diversity and equal opportunity in higher education through teaching and service. The primary duty is teaching undergraduate courses. Teaching opportunities range from introductory computer science courses, such as computer theory, discrete math, data structures, and computer organization to advanced courses, such as game development, mobile computing and cybersecurity. Applicants should be able to teach in one or more areas of computer science. All faculty positions require a cover letter, current curriculum vita, teaching statement and three (3) professional reference letters. Letters of reference must address the candidate's overall quality of teaching and/or presentation skills, the ability to communicate complex topics and expertise in the field of computer science. Applications for non-tenure track positions will be considered on an on-going basis. Inquiries may be directed to faculty-search@cs.utexas.edu.

4. Duke Kunshan University Institute of Applied Physical Sciences and Engineering, China

Job Title: Faculty Position (Open Rank) in Electrical and Computer Engineering

Description: Duke Kunshan University seeks applications for a faculty position (rank open) in the area of electrical and computer engineering. The position is expected to start as early as summer 2021. Duke Kunshan University has recently established the Institute of Applied Physical Sciences and Engineering (iAPSE) and the Data Science Research Center (DSRC) with strong research programs in several emerging areas, including image processing and computer vision, speech and natural language processing, smart manufacturing, autonomous driving, business data analysis, etc. Duke Kunshan University has launched a Master of Engineering Program in Electrical and Computer Engineering in Fall 2019 – students fulfilling the degree requirement will receive a Duke University degree. Candidates must hold a Ph.D. degree in electrical and computer engineering, computer science or relevant fields. Candidates must have strong technical backgrounds in professional

software development and testing in C/C++ and are familiar with professional development tools such as Linux, emacs, git, gcc, make, valgrind, gdb, etc. Experience of postdoctoral training and/or industrial research is highly desirable. Candidates must demonstrate a strong ability to conduct outstanding independent research and show promise for excellent teaching and mentoring. Candidates, whose research and teaching are interdisciplinary and connected to the educational programs and research institutes/centers at Duke Kunshan University, are strongly encouraged to apply. The application address is <https://academicjobsonline.org/ajo/jobs/14141>. The search committee also invites and encourages letters of nomination for potential candidates. Nominations may be sent to ece-search@dukekunshan.edu.cn. Use "ECE Faculty" as the subject line.

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