

1 September 2020, Vol. 50, No. 9

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Comments from the Editors

Dear ACM/SIGDA members,

We are excited to present to you the September e-newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from the upcoming conferences and hot research topics to technical news and activities from our community. From this month, we add a new column titled "SIGDA Partner Journal" where we will introduce the dynamics of SIGDA related journals. For this month, we are introducing the new editorial board of ACM TODAES and announcing a new partnership between SIGDA and ACM TRETTS. Get involved and contact us if you want to contribute an article or announcement.

The newsletter is evolving, let us know what you think.

Happy reading!

[Debjit Sinha](#), Keni Qiu, Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit <http://www.acm.org/renew> or call between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or 1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org

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""Xin Zhao"" , E-Newsletter Associate Editor for SIGDA Paper submission deadline column

""Ying Wang"" , E-Newsletter Associate Editor for SIGDA Technical activities column

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SIGDA News

(1) "Electronics Supply Chains Splitting Between China and U.S."

[\[https://www.eetimes.com/electronics-supply-chains-splitting-between-china-and-u-...\]](https://www.eetimes.com/electronics-supply-chains-splitting-between-china-and-u-...)

Foxconn, the world' s largest contract manufacturer, says it plans to move more of its production outside China under the impact of the trade war between the world' s two largest economies.

(2) "Marvell Joins TSMC' s Big League Customers with 5G ICs"

[\[https://www.eetimes.com/marvell-joins-tsmcs-big-league-customers-with-5g-ics/\]](https://www.eetimes.com/marvell-joins-tsmcs-big-league-customers-with-5g-ics/)

Marvell, after reinventing itself as a supplier of data infrastructure silicon, has joined the upper echelon of Taiwan Semiconductor Manufacturing Co. (TSMC) customers by winning capacity allocation at the 5nm node.

(3) "TSMC Plots the Process Course to Its Next 'Generational Node' "

[\[https://www.eetimes.com/tsmc-plots-the-process-course-to-its-next-generational-n...\]](https://www.eetimes.com/tsmc-plots-the-process-course-to-its-next-generational-n...)

Even as it ramps up production on its N5 process, Taiwan Semiconductor Manufacturing Co. (TSMC),

at its annual Technology Symposium, introduced its N4 process, which it said is scheduled to come online in late 2021, with volume production in 2022. Anticipating the inevitable question, the company also provided some details about its subsequent N3.

(4) "Nvidia Data Center Growth: Could Buying Arm Be an Ideal Match?"

[\[https://www.eetimes.com/nvidia-data-center-growth-could-buying-arm-be-an-ideal-m...\]](https://www.eetimes.com/nvidia-data-center-growth-could-buying-arm-be-an-ideal-m...)

As Nvidia announced record data center revenue in its quarterly financial results this week, it has been hailed in the financial press as a new "king of chips." In an interview that founder and CEO Jensen Huang gave to the UK's Financial Times, he highlighted the company's plans to rule the data center. Marrying this up with rumors that Nvidia is considering purchasing Arm, could we be seeing signs of a transition in both the direction and fortune of both Nvidia and Arm?

(5) "The Revolution of Electrical Infrastructure is Starting"

[\[https://www.eetimes.com/the-revolution-of-electrical-infrastructure-is-starting/\]](https://www.eetimes.com/the-revolution-of-electrical-infrastructure-is-starting/)

There is plenty of opportunities to make old residential electric infrastructure more efficient. The residential represents an attractive market for companies that offer intelligent control systems.

(6) "Demand for Edge AI Chips to Surpass Cloud AI by 2025"

[\[https://www.eetimes.com/demand-for-edge-ai-chips-to-surpass-cloud-ai-by-2025/\]](https://www.eetimes.com/demand-for-edge-ai-chips-to-surpass-cloud-ai-by-2025/)

Despite the current pandemic-related downturn, the demand for edge AI chips will grow to outstrip demand for cloud AI chips for the first time in 2025, according to a new report from ABI Research.

(7) "Syntiant Raises Another \$35M, Ships 1 Million Edge AI Chips"

[\[https://www.eetimes.com/syntiant-raises-another-35m-ships-1-million-edge-ai-chip...\]](https://www.eetimes.com/syntiant-raises-another-35m-ships-1-million-edge-ai-chip...)

Ultra-low-power AI accelerator startup Syntiant has raised another \$35 million in a series C round of funding to bring the total raised by the company to \$65 million. Syntiant, whose 66 staff work out of Irvine, Calif., also announced that it has hit a shipping milestone with 1 million parts in the hands of customers.

(8) "In Transition, Sensor Market Is Seen Riding IoT Wave"

[\[https://www.eetimes.com/in-transition-sensor-market-is-seen-riding-iot-wave/\]](https://www.eetimes.com/in-transition-sensor-market-is-seen-riding-iot-wave/)

The sensor market is among the technology sectors hardest hit by the pandemic. Already rocked by the decline of fossil fuels and internal combustion engines as well as the commoditization of existing sensor technologies, Covid-19 has further clouded the picture of the automotive sensor market.

(9) "Optical Compute Promises Game-Changing AI Performance"

[\[https://www.eetimes.com/optical-compute-promises-game-changing-ai-performance/\]](https://www.eetimes.com/optical-compute-promises-game-changing-ai-performance/)

Lightmatter, the MIT spinout developing optical compute processors for AI acceleration, presented a test chip at Hot Chips 32 this week. Using techniques from silicon photonics and MEMS, the processor performs matrix-vector multiplication at the speed of light (in silicon), powered by a milliwatt laser light source. Computation is orders of magnitude faster than transistor-based chips, including the latest GPUs, and it uses very little power.

(10) "NVMe Controllers Look to Maximize NAND Potential"

[\[https://www.eetimes.com/nvme-controllers-look-to-maximize-nand-potential/\]](https://www.eetimes.com/nvme-controllers-look-to-maximize-nand-potential/)

Just as NVMe has unlocked the true value of non-volatile flash in SSDs, it's becoming more important that these SSDs have a controller that maximizes the potential of today's NAND in these drives, especially as NVMe makes gains against SATA and SAS drives. The customer base is evolving too, with OEMs and hyperscalers expecting more flexibility and programmability for their own

customizations.

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SIGDA Local Chapter News

The CEDA/SIGDA Design Automation WebiNar (DAWN) Event 3 has been held. The title of this event is "Secure Silicon: Recent Developments and Upcoming Challenges". The four prestigious presenters and their presentation titles are:

Dr. Brandon Wang, Vice President, Synopsys Inc.
Keys to Hardware Security

Prof. Mark M. Tehranipoor, Director, Florida Institute for Cybersecurity Research, Univ. of Florida
Automated Implementation of Secure Silicon

Prof. Gang Qu, Professor, ECE, University of Maryland
Assessment of Hardware Security and Trust

Ahmad-Reza Sadeghi, Professor, TU Darmstadt
Enclave Computing on RISC-V: A Brighter Future for Platform Security?

The moderator is Prof. Yier Jin at University of Florida. The webpage is <https://duke-cei-lab.github.io/DAWN/event3/>.

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"What is" Column

What is Neural Architecture Search?

Callie (Cong) Hao
Faculty Fellow,
Electrical and Computer Engineering Department,
Georgia Institute of Technology

With the rapid development of machine learning algorithms, especially artificial neural network (ANN) models, the growing size and complexity of such ANN models make it challenging for manual designs. To this end, neural architecture search (NAS) has been attracting more and more research interest [1]. NAS is a technique for automating the design of ANNs which can outperform hand-crafted ones. It can be seen as a subfield of AutoML.

The NAS process involves three major components: ANN search space, search strategy, and performance evaluation. The ANN search space defines the ANN structure that is to be discovered by NAS: it can be a single-path chain-like structure or a complex multi-branch network with non-regular connections between layers and operations. The search strategy determines how the best ANN structure is searched. Currently the most widely used search strategies include reinforcement learning, evolutionary algorithms, differentiable NAS and supernet based one-shot search. Finally, the performance evaluation assesses the quality of the searched ANNs, which usually requires ANN training and is the most time-consuming part. Thus, many works aim to reduce the training complexity by coming up with estimations such as weight sharing and weight inheritance [2, 3].

Early NAS works like NASNet [4] and AmoebaNet [5] utilized reinforcement learning or evolutionary algorithms to search for the DNN architectures by massively training a large number of independent networks from scratch. More recently, another approach called one-shot NAS has been proposed. It defines the search space as a supernet composed of weight-sharing subnets, and the desirable

subnets will be extracted from the supernet after training. One-shot NAS is favored by researchers in academia and industry due to its significantly lower demands on computational resources and shorter search time (within a few GPU-days). There are two main types of one-shot NAS. One is the differentiable NAS (DNAS) [6], which uses a continuous relaxation of the architecture representations and introduces architecture parameters to distinguish the subnets. The other category is random-sampling NAS (RandomNAS) [7]. RandomNAS approach typically constructs a supernet composed of weight-sharing subnets, and goes through supernet training and subnet selection iteratively, followed by subnet retraining in the end. Compared to DNAS, RandomNAS requires much less computational resources and shorter search time.

To target the efficient hardware deployment of DNNs, researchers also start focusing on hardware-aware solutions, i.e., hardware-aware NAS. Some works incorporate hardware latency into the objective of NAS, while some treat latency as a hard constraint [8, 9]. On top of hardware-aware NAS, simultaneous NAS and hardware implementation co-exploration has demonstrated further success in developing hardware friendly ANN models as well as efficient hardware accelerators. For example, the work NAIS [10] discussed neural architecture and implementation search, while a follow-up work called EDD [11] materialized the NAIS idea and proposed a fully simultaneous NAS and hardware implementation co-exploration framework.

Given the remarkable achievements of NAS, hardware-aware NAS and NAIS, it is definitely a promising but also challenging area to further boost the development of AI and machine learning. Much more works and exciting research areas are worth exploring, to expand NAS into wider application scenarios with high search efficiency and low carbon footprint.

References

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- [9] Tan, Mingxing, Bo Chen, Ruoming Pang, Vijay Vasudevan, Mark Sandler, Andrew Howard, and Quoc V. Le. "Mnasnet: Platform-aware neural architecture search for mobile." In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, pp. 2820-2828. 2019.
- [10] Cong Hao, Yao Chen, Xinheng Liu, Atif Sarwari, Daryl Sew, Ashutosh Dhar, Bryan Wu, Dongdong Fu, Jinjun Xiong, Wen-mei Hwu, Junli Gu, [Deming Chen](#). "NAIS: Neural Architecture and Implementation Search and its Applications in Autonomous Driving." In 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 1-8. IEEE, 2019.
- [11] Yuhong Li, Cong Hao, Xiaofan Zhang, Xinheng Liu, Yao Chen, Jinjun Xiong, Wen-mei Hwu, [Deming Chen](#). "EDD: Efficient differentiable DNN architecture and implementation co-search for embedded AI solutions." Proceedings of the ACM/IEEE Design Automation Conference (DAC), 2020.

Paper Submission Deadlines

VLSID'21 – International Conference on VLSI Design

Virtual Conference

Deadline: Sept 1, 2020

Jan 4-8, 2021

<http://embeddedandvlsidesignconference.org/>

WOSET'20 - Workshop on Open-Source EDA Technology (co-located with ICCAD 2020)

San Diego, CA

Deadline: Sept 6, 2020

Nov 5, 2020

<https://woset-workshop.github.io>

FPGA' 21 – ACM/SIGDA Int' l Symposium on Field-Programmable Gate Arrays

Virtual Conference

Deadline: Sept 7, 2020

Feb 28-Mar 2, 2021

<http://www.isfpga.org>

ISSCC'21 – IEEE Int'l Solid-State Circuits Conference

San Francisco, CA

Deadline: Sept 9, 2020

Feb 13-18, 2021

<http://isscc.org>

ArchEdge'20 - The 3rd Workshop on Computing Architecture for Edge Computing

Virtual Conference

Deadline: Sept 10, 2020

November 11-13, 2020

<http://acm-ieee-sec.org/2020/archedge.php>

DATE'21 - Design Automation and Test in Europe

Grenoble, France

Deadline: Sept 21, 2020 (Abstracts due: Sept 14, 2020)

Feb 1-5, 2021

<http://www.date-conference.com>

ISED' 20 – Int' l Symposium on Electronic System Design

Kollam, India

Deadline: Sept 25, 2020

Dec 18-20, 2020

<http://isedconf.org>

ISQED'21 - Int'l Symposium on Quality Electronic Design

Santa Clara, CA

Deadline: Oct 2, 2020

Apr , 2021

<http://www.isqed.org>

SLIP^2 - System-Level Interconnect Problems and Pathfinding (co-located with ICCAD 2020)

San Diego, CA

Deadline: Oct 3, 2020 (Abstracts due: Sept 26, 2020)

Nov 5, 2020

<http://sliponline.org>

ISPD' 21 – ACM Int' l Symposium on Physical Design (canceled)

Deadline: Oct 12, 2020 (Abstracts due: Oct 2, 2020)

Mar 21-24, 2021

<http://www.ispd.cc>

TAU' 21 – ACM Int' l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems

Monterey, CA

Deadline: Dec xx, 2020

Apr 8-9, 2021

<http://www.tauworkshop.com>

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Upcoming Conferences and Symposia

GLSVLSI' 20 – ACM Great Lakes Symposium on VLSI

Virtual Conference

Sept 8-11, 2020

<http://www.glsvlsi.org>

ESWEEK'20 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)

Virtual Conference

Sept 20-25, 2020

<http://www.esweek.org>

NOCS'20 – IEEE/ACM Int' l Symposium on Networks-on-Chip (co-located with ESWEEK'20)

Virtual Conference

Sept 24-25, 2020

<http://nocs2020.engr.uky.edu/>

PACT'20 - Int'l Conference on Parallel Architectures and Compilation Techniques

Virtual Conference

Oct 3-7, 2020

<http://www.pactconf.org>

VLSI-SoC' 20 – IFIP/IEEE Int' l Conference on Very Large Scale Integration

Virtual Conference

Oct 5-9, 2020

<http://www.vlsi-soc.com>

ISCAS'20 – IEEE Int'l Symposium on Circuits and Systems

Virtual Conference

Oct 10-21, 2020

<http://iscas2020.org>

MICRO' 20 – IEEE/ACM Int'l Symposium on Microarchitecture

Virtual Conference

Oct 17-21, 2020

<http://www.microarch.org/micro53>

BodyNets'20 – Int' l Conference on Body Area Networks

Virtual Conference

Oct 21-22, 2020

<http://www.bodynets.org>

ICCAD' 20 – IEEE/ACM Int' l Conference on Computer-Aided Design
Virtual Conference

Nov 2-5, 2020

<http://www.iccad.com>

HOST'20 – IEEE Int' l Symposium on Hardware-Oriented Security and Trust
Virtual Conference

Dec 6-9, 2020

<http://www.hostsymposium.org>

FPT'20 - Int'l Conference on Field-Programmable Technology
Virtual

Dec 7-11, 2020

<http://icfpt.org>

HiPC'20 – IEEE Int'l Conference on High Performance Computing, Data, And Analytics
Pune, India

Dec 16-19, 2020

<http://www.hipc.org>

iSES' 20 – IEEE Int' l Symposium on Smart Electronic Systems
Chennai, India

Dec 14-16, 2020

<http://www.ieee-ises.org>

ASP-DAC'21 - Asia and South Pacific Design Automation Conference
Tokyo, Japan

Jan 18-21, 2021

<http://www.aspdac.com>

HiPEAC'21: Int'l Conference on High Performance Embedded Architectures & Compilers
Budapest, Hungary

Jan 18-20, 2021

<https://www.hipeac.net/2021/budapest>

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SIGDA Partner Journal

1. New Editorial Board -- ACM TODAES

The ACM Transactions on Design Automation of Electronic Systems (TODAES), the premier ACM journal in design and automation of electronic systems and a closer partner of SIGDA, has a new Editorial Board since June 1, 2020. It is calling for submission of Special Issue proposals as well as tutorials, surveys and the newly established Designer Notes. You can find TODAES' s updated scope at <https://dl.acm.org/journal/todaes/about>.

The election of TODAES' s new Senior Editorial Board is for a three-year term from June 1, 2020 through May 31, 2023. Sharon Hu, as its Editor in Chief, is currently a Professor of Computer Science and Engineering at the University of Notre Dame, IN, USA. Her current research interests include computing with beyond-CMOS technologies, low-power system design, and cyber-physical systems. She has served as an associate editor for several ACM and IEEE Transactions journals, including

TODAES, the ACM Transactions on Embedded Computing Systems (TECS), and the ACM Transactions on Cyber-Physical Systems (TCPS). She was the General Chair of the 2018 Design Automation Conference (DAC) in 2018.

TODAES also welcomes Jörg Henkel and David Pan as its new Senior Associate Editors. Professor Henkel is a Professor and Chair for Embedded Systems CES at Karlsruhe Institute of Technology (KIT). His research areas include co-design for embedded hardware/software systems with respect to power, thermal, and reliability aspects. For two consecutive terms, he served as the Editor-in-Chief for the ACM TECS and IEEE Design & Test Magazine, and has served as an Associate Editor for several ACM and IEEE journals, including ACM TCPS.

Professor David Pan is currently a Professor and the Silicon Laboratories Endowed Chair in Electrical Engineering at The University of Texas at Austin. His research interests include electronic design automation, design for manufacturing, machine learning and hardware acceleration, design/CAD for analog/mixed signal designs and emerging technologies. He has served as an Associate Editor of several ACM and IEEE journals, including TODAES. He has served in the Executive and Program Committees of many major conferences, including DAC, ICCAD, ASPDAC, and ISPD.

You are invited to visit the TODAES homepage at <https://dl.acm.org/journal/todaes>, where you may read innovative work documenting significant research and development advances in electronic system design, emphasizing a computer science/engineering orientation. You are also invited to submit research in these areas, and theoretical analysis and practical solutions are welcome.

2. SIGDA Partnership Announcement -- ACM TRET

We are pleased to announce a new partnership between SIGDA and the ACM Transactions on Reconfigurable Technology and Systems (TRET). TRET is a peer-reviewed and archival journal covering technology, systems, and applications on reconfigurable computers or devices. TRET has been the vehicle for publishing many seminal papers over the past decade. Reconfigurable technology includes field programmable gate arrays (FPGAs) and other adaptable fabrics. Topics appropriate for TRET include all levels of reconfigurable system abstractions and technologies, platforms, programming environments, operating systems, design automation, and application successes.

Recent TRET papers have presented work in the areas of neural net design space exploration, security of FPGAs in the cloud, open-source FPGA CAD tools, advances in high-level synthesis, hardware acceleration of graph algorithms, novel FPGA architectures, reconfigurable space systems, and more.

We invite you to visit the homepage of TRET, <https://dl.acm.org/journal/trets>, where you can find links to recent issues, our current call for papers, and author information. In addition, we have recently launched a TRET twitter account, https://twitter.com/ACM_TRET, where you can receive notifications of new quarterly issues, occasional features of popular publications from recent issues, and awards announcements.

[Deming Chen](#)

Editor-in-Chief, TRET

Abel Bliss Professor of University of Illinois at Urbana-Champaign

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Call for Nomination -- ACM TCPS EiC

The term of the current Editor-in-Chief (EiC) of the ACM Transactions on Cyber-Physical Systems (TCPS) is coming to an end, and the ACM Publications Board has set up a nominating committee to assist the Board in selecting the next EiC. Nominations, including self-nominations, are invited for a three-year term as TCPS EiC, beginning on March 1, 2021. The EiC appointment may be renewed at most one time. This is an entirely voluntary position, but ACM will provide appropriate administrative support.

The EiC is responsible for maintaining the highest editorial quality, for setting technical direction of the papers published in TCPS, and for maintaining a reasonable pipeline of articles for publication. He/she has final say on acceptance of papers, size of the Editorial Board, and appointment of Associate Editors. The EiC is expected to adhere to the commitments expressed in the policy on Rights and Responsibilities in ACM Publishing. For more information about the role of the EiC, see ACM's Evaluation Criteria for Editors-in-Chief.

Nominations should include a vita along with a brief statement of why the nominee should be considered. Self-nominations are encouraged, and should include a statement of the candidate's vision for the future development of TCPS. The deadline for submitting nominations is 30 October 2020, although nominations will continue to be accepted until the position is filled.

Please send all nominations to the search committee chair, Krithi Ramamritham (ramamrithamk@gmail.com). The search committee members are:
Krithi Ramamritham (Indian Institute of Technology Bombay), Chair
Tarek Abdelzaher (University of Illinois at Urbana-Champaign)
Samarjit Chakraborty (University of North Carolina at Chapel Hill)
Tulika Mitra (National University of Singapore)
Wei Zhao (American University of Sharjah)
Divesh Srivastava (AT&T Research), ACM Publications Board Liaison

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Technical Activities

1. "GPT-3; TSMC 5nm customers; ML-enhanced simulation; processor updates"

Catching up on some recent news after a two-week summer break, let's start by briefly reporting about GPT-3, the new language model from OpenAI. Other updates concern EDA, processors, and more...

[\[https://www10.edacafe.com/blogs/editorial\]](https://www10.edacafe.com/blogs/editorial)

2. "Optical Processor Targets to Accelerate Compute for Next-Gen AI"

MIT spinout Lightmatter presented its optical compute chip at Hot Chips 32, promising orders of magnitude improvements in latency and power consumption...

[\[https://www.eetasia.com/optical-processor-targets-to-accelerate-compute-for-next...\]](https://www.eetasia.com/optical-processor-targets-to-accelerate-compute-for-next...)

3. "Challenges and Trends in Sustainable Battery Manufacturing"

New comprehensive automation concepts can help the European battery industry become more efficient and extra competitive. These concepts are based on artificial intelligence (AI), smart robotics, and the latest vision technology...

[\[https://www.eetimes.eu/challenges-and-trends-in-sustainable-battery-manufacturin...\]](https://www.eetimes.eu/challenges-and-trends-in-sustainable-battery-manufacturin...)

4. "Implementing a Hybrid Approach to Eliminate Software Defects in ADAS Features"

As shown by a recent study by the American Automobile Association, safety-critical automotive applications are not exactly free from software defects...

[<https://www.eetasia.com/implementing-a-hybrid-approach-to-eliminate-software-def...>]

Job Openings:

1. Indiana University Bloomington United States

Job Title: Assistant Professor of Informatics

Description: Please see Special Instructions for more details. Interested candidates should review the application requirements and submit their application at:

<http://indiana.peopleadmin.com/postings/9805>. The application must include a cover letter, a curriculum vitae outlining appropriate education and work experience, a one-page statement outlining teaching philosophy, a one-page statement outlining research agenda, unofficial copies of undergraduate and graduate transcripts, and the names, mailing addresses, email addresses, and telephone numbers of at least three professional references.

Interested candidates should review the application requirements and submit their application at: <http://indiana.peopleadmin.com/postings/9805>. The application must include a cover letter, a curriculum vitae outlining appropriate education and work experience, a one-page statement outlining teaching philosophy, a one-page statement outlining research agenda, unofficial copies of undergraduate and graduate transcripts, and the names, mailing addresses, email addresses, and telephone numbers of at least three professional references.

2. University of Washington United States

Job Title: Assistant Professor Tenure-Track in Human-Computer Interaction

Description: Competitive applicants will have evidence of demonstrated research excellence and effective and engaging teaching. The successful applicant will be expected to engage in service for their department and the broader HCI field. The successful applicant will also be expected to conduct research that not only furthers possibilities for human-computer interaction, but also shows an understanding of the ways that technology can and has been used to exclude, marginalize, privilege, and even harm people, societies, and the environment (e.g., via inaccessible user interfaces, exclusionary data schemas, misleading data visualizations, selective data collection practices, biased training data or algorithms, unobtainable technologies for learning, inadequate Internet access in rural communities, inscrutable face and image classifiers, deep fakes, and many other ways). The Assistant Professor will be expected to excel in their work while also understanding its possible social limitations and harms, and who appreciate the larger ramifications surrounding interactive technologies, especially concerning matters of social justice. The UW Information School brings together faculty and students in HCI and many other disciplines. Current HCI faculty and students are world-class leaders in accessible computing, computing education, digital youth, health and wellness informatics, crisis informatics, ICT4D, information ethics, social computing, and value sensitive design, to name a few. We welcome applications from researchers investigating HCI topics that will deepen and/or extend our strengths in HCI.

The University of Washington is using Interfolio's Faculty Search to conduct this search. Applicants to this position receive a free Dossier account and can send all application materials, including confidential letters of recommendation, free of charge. For help signing up, accessing your account, or submitting your application, please check out Interfolio's help and support section or get in touch via email at help@interfolio.com or phone at (877)997-8807.

3. Carleton University Canada

Job Title: Assistant / Associate Professor of Software Engineering for Autonomous and Self-Adapting Systems

Description: The Department of Systems and Computer Engineering invites applications for a Canada Research Chair (CRC) Tier 2 appointment in the field of Software Engineering for autonomous and self-adapting systems at the rank of Assistant/Associate Professor beginning July 1, 2020. The appointment is conditional on the approval of the application by the CRC Secretariat. Tier 2 Chairs are intended for exceptional emerging researchers (i.e. candidate will typically be less than 10 years from their highest degree at the time of nomination, or more than 10 years and has experienced legitimate career interruptions), acknowledged by their peers as having potential to lead in their field. Applicants who are more than 10 years from their highest degree may have their eligibility for a Tier 2 Canada Research Chair assessed through the program's Tier 2 justification process (chairs-chaire.gc.ca). Please contact Carleton's research grants office (carleton.ca/coris) for more information. The Department of Systems and Computer Engineering (carleton.ca/sce) is a research-intensive department and hosts a large and active community of faculty members, instructors, and undergraduate and graduate students. The Department participates in a broad range of undergraduate and graduate programs. Full advantage is taken of the high concentration of industry and government in the Ottawa area.

4. University of Twente Faculty of Electrical Engineering, Mathematics and Computer Science, Netherlands

Job Title: Full Professor of Computer Science

Description: In a world in which trust and resilience of our communication infrastructures become of key importance for our digital society and our digital sovereignty becomes at stake, it is important to understand how crucial networks and systems should be designed in a responsible way. The Design and Analysis of Communication Systems (DACS) group of the University of Twente (UT) is an internationally leading group in the area of network security and performs research in these societal challenges. Within DACS there is a new position for a Full Professor who performs research on network and IoT security, with a focus on Open and Software Defined Networking.

You are welcome to contact prof.dr. Dirk Heylen for any questions you might have (d.k.j.heylen@utwente.nl).

5. University of Adelaide School of Computer Science, Australia

Job Title: Senior Lecturer - School of Computer Science

Description: The School is especially keen to recruit an individual whose Software Engineering research might lead to inter-disciplinary work in areas such as AI, Optimisation, Data Science or Cybersecurity. The School enjoys excellent research and industry collaboration opportunities in the area of software engineering and, there is a great opportunity to develop new teaching directions and approaches in the area of Software Engineering.

In addition, we offer a wide range of attractive staff benefits. These include: salary packaging; flexible work arrangements; high-quality professional development programs and activities; and an on-campus health clinic, gym and other fitness facilities. Learn more at: adelaide.edu.au/jobs

For a confidential discussion regarding this position, contact:

Professor Ian Reid

Head of School, School of Computer Science

P: +61 (0) 8313 2135

E: ian.reid@adelaide.edu.au

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