1 April 2020, Vol. 50, No. 4

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From: Xiang Chen < <a href="mailto:shawn.xiang.chen@gmail.com">shawn.xiang.chen@gmail.com</a>>

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Contributing author: Dr. Xiaolong Guo, Electrical and Computer Engineering Department,

Kansas State University

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# Comments from the Editors

Dear ACM/SIGDA members,

We are excited to present to you the April e-newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from the upcoming conferences and funding deadlines, hot research topics to news and technical activities from our community. Get involved and contact us if you want to contribute an article or announcement.

For this month, we are introducing a new column titled "Technical Activities" and the column Editor: Prof. Ying Wang. In this column, we will introduce exciting technical trends, industrial dynamics, etc. and post position openings from time to time.

The newsletter is evolving, let us know what you think.

Happy reading!

Debjit Sinha, Keni Qiu, Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit <a href="http://www.acm.org/renew">http://www.acm.org/renew</a> or call between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or 1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org

- "SIGDA E-News Editorial Board:"
- ""Debjit Sinha"", E-Newsletter co Editor-in-Chief
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- "Xin Zhao", E-Newsletter Associate Editor for SIGDA Paper submission deadline column
- "'Ying Wang'", E-Newsletter Associate Editor for SIGDA Technical activities column

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#### **SIGDA News**

(1) "ISSCC 2020: Chiplets, 5G, and Automotive Processors" [https://www.eetimes.com/isscc-2020-chiplets-5g-and-automotive-processors/]

This year's processor session at the ISSCC led off with two presentations by AMD (for the first time) followed by presentations from Samsung and MediaTek talking about their latest 5G smart phone chips, a research project/proof of concept design from CEA technology, an automotive system on chip (SoC) from Texas Instruments (TI), and the latest IBM Z series mainframe processor.

(2) "OFC 2020: Looking at the Future of Optics and Silicon Photonics" [https://www.eetimes.com/ofc-2020-looking-at-the-future-of-optics-and-silicon-pho...]

Of the few events that survived the current wave of cancelled events, the OFC 2020 conference and exhibition took place in San Diego, California this week, exploring the future of optics communications and 5G innovations.

(3) "U.S. IC Companies Maintain Global Marketshare Lead" [https://www.eetimes.com/u-s-ic-companies-maintain-global-marketshare-lead/#]

Propelled by 51% share of IDM sales and 65% share of fabless sales, U.S. companies captured 55% of the total worldwide IC market in 2019, according to semiconductor research firm IC Insights.

(4) "Hot EDA Sector Cooled Off in Q4" [https://www.eetimes.com/hot-eda-sector-cooled-off-in-q4/]

Global revenue in the EDA segment of the electronics industry grew 8.3 percent in 2019, despite tailing off to weaker growth of just 2.2 percent in the fourth quarter of 2019, according to statistics published by Semi and the Electronic System Design (ESD) Alliance.

(5) "Xilinx Launches Biggest ACAP Yet"
[https://www.eetimes.com/xilinx-launches-biggest-acap-yet/]

Xilinx has released details of its Versal Premium series, designed for telco network infrastructure and cloud applications. These devices offer three times the bandwidth and will enable double the compute density for accelerated workloads in the data centre, when compared to Xilinx' previous generation of FPGAs.

[6] "SMIC Graduating from 14nm to Something Sort of Akin to 7nm" [https://www.eetimes.com/smic-graduating-from-14nm-to-something-sort-of-akin-to-7...]

Published reports that SMIC is preparing a 7-nanometer production process are incorrect. The error is understandable, however, as it is based on favorable comparisons SMIC has been making between its newest process technology (called N+1) and rivals' 7nm processes.

[7] "Qualcomm Poised For Post-Virus Rebound" [https://www.eetimes.com/qualcomm-poised-for-post-virus-rebound/]

Although hopes are fading for rebounding component demand in the second half of the year (2H), Qualcomm is positioned to be an exception. The chip maker will benefit from the long-term 5G investment cycle, according to Canaccord Genuity, as Apple re-enters the model for shipments and global demand for smartphones improves.

[8] "Intel Scales Neuromorphic Computer to 100 Million Neurons" [https://www.eetimes.com/intel-scales-neuromorphic-computer-to-100-million-neuron...]

Intel has scaled up its neuromorphic computing system by integrating 768 of its Loihi chips into a 5 rack-unit system called Pohoiki Springs. This cloud-based system will be made available to Intel's Neuromorphic Research Community (INRC) to enable research and development of larger and more complex neuromorphic algorithms. Pohoiki Springs contains the equivalent of 100 million neurons, about the same number as in the brain of a small mammal such as a mole rat or a hamster.

[9] "5G Rollout Will Slow as Standards Work is Suspended"
[https://www.eetimes.com/5g-rollout-will-slow-as-standards-work-is-suspended/]

The 5G rollout will grind to a slower pace with a decision by the 3GPP to suspend work on some crucial parts of the specification due to the impact of the novel coronavirus.

[10] "New Microchip MCU Enables Secure Boot Protection from SPI Flash" [https://www.eetimes.com/new-microchip-mcu-enables-secure-boot-protection-from-sp...]

As growth in 5G expands, with new cellular infrastructure, networks and data centers supporting cloud computing, there is an ever growing need to keep operating systems secure and ensure they are not compromised. They are particularly vulnerable to rootkit malware, which loads before an operating system boots and can hide from ordinary anti-malware software – making it very difficult

to detect. One way of defending against rootkits is with secure boot.

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# "What is" Column

What is Hardware Trustworthiness?

Xiaolong Guo

Assistant Professor,

Electrical and Computer Engineering Department,

**Kansas State University** 

The exponential growth of the integrated circuit (IC) industry results in the rapid globalization of its supply chain. Since a complicated IC design often involves numerous IP suppliers, fabrication foundries, and testing facilities spanning multiple continents, it is extremely challenging, if not outright impossible, to track the source of every component and secure the entire supply chain. The sophistication of today's IC development process gives rise to the increasing threats of hardware Trojans (HTs) and hardware vulnerabilities.

Among the supply chain, Trojans and vulnerabilities may exist in the untrusted design house, third party vendor, back-end house and foundry. The wide usage of hardware intellectual property (IP) cores and software programs from untrusted third-party vendors have raised security concerns for computer system designers. Due to the extremely high cost of building foundries, chip manufacturing is usually outsourced to existing foundries. On the other hand, hardware vulnerabilities are often due to design mistakes because the designer does not sufficiently consider potential security vulnerabilities at the design stage. Meanwhile, current Trojan detection approaches always assume HTs are composed of digital circuits. However, recent demonstrations of analog attacks, such as A2 [1] and Rowhammer [2], invalidate the digital assumption in previous HT detection or testing methods.

As a consequence, security experts from different domains have begun to make every endeavor to guarantee the trustworthiness of the hardware. For instance, to overcome the threat of untrusted third-party resources, many pre-silicon trust evaluation methods have recently been developed. Some of those methods detect malicious logic by using enhanced functional testing methods [3]. In the post-silicon stage, based on the fact that the chip's side channel parameters are affected due to the insertion of a malicious hardware Trojan, side channel analysis approaches identify the hardware Trojan by comparing the measured side channel parameters with golden ICs or references [4][5]. Formal methods have shown their importance in exhaustive hardware security verification through validating the trustworthiness of IP cores and their respective SoC system [6][7]. They cover a wide range in the supply chain, like proof-carrying hardware (PCH) framework applied in the design stage [8-10], information-flow tracking (IFT) in the transistor level layout [11], runtime verification in the post-silicon [12-14], etc.

In summary, as a result of the globalization of the semiconductor supply chain, companies and the government have decentralized control over this industry. Vulnerabilities in the pre- and post-silicon stages of an IC supply chain may cause IP piracy and the inclusion of a Trojan circuit can derail the entire hardware industry. Upon all these challenges, we look forward to more flexible, comprehensive and automated solutions for eliminating the security concerns for the semiconductor industry.

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MICRO' 20 – IEEE/ACM Int'l Symposium on Microarchitecture

Athens, Greece

Deadline: Apr 17, 2020 (Abstracts due: Apr 10, 2020)

Oct 17-21, 2020

http://www.microarch.org/micro53

ESWEEK'20 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)

Hamburg, Germany

Deadline: Apr 17, 2020 (Abstracts due: Apr 3, 2020)

Sept 20-25, 2020 <a href="http://www.esweek.org">http://www.esweek.org</a>

IWBDA'20 - Int'l Workshop on Bio-Design Automation

Worcester, MA

Deadline: Apr 10, 2020

Jun 8-10, 2020

http://www.iwbdaconf.org/2020

BodyNets'20 – Int' | Conference on Body Area Networks

Tallinn, Estonia

Deadline: Apr 15, 2020

Oct 21-22, 2020

http://www.bodynets.org

PACT'20 - Int'l Conference on Parallel Architectures and Compilation

Techniques Atlanta, GA

Deadline: Apr 24, 2020 (Abstracts due: Apr 17, 2020)

Oct 3-7, 2020

http://www.pactconf.org

VLSI-SoC' 20 – IFIP/IEEE Int' I Conference on Very Large Scale Integration

Salt Lake City, UT

Deadline: Apr 27, 2020 (Abstracts due: Apr 20, 2020)

Oct 5-7, 2020

http://www.vlsi-soc.com

NOCS'20 – IEEE/ACM Int' | Symposium on Networks-on-Chip (co-located with ESWEEK'20)

Hamburg, Germany

Deadline: May 1, 2020 (Abstracts due: Apr 24, 2020)

Sept 24-25, 2020

http://nocs2020.engr.uky.edu/

ICCAD' 20 – IEEE/ACM Int' I Conference on Computer-Aided Design

San Diego, CA

Deadline: May 28, 2020 (Abstracts due: May 21, 2020)

Nov 2-5, 2020

http://www.iccad.com

iSES' 20 – IEEE Int' | Symposium on Smart Electronic Systems

Chennai, India

Deadline: May 31, 2020

Dec 14-16, 2020

http://www.ieee-ises.org

HiPC'20 – IEEE Int'l Conference on High Performance Computing, Data, And Analytics

Pune, India

Deadline: June 16, 2020 (Abstracts due: June 9, 2020)

Dec 16-19, 2020 http://www.hipc.org

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# **Upcoming Conferences and Symposia**

ASYNC'20 – IEEE Int' I Symposium on Asynchronous Circuits and Systems Snowbird, UT
May 17-20, 2020
<a href="http://asyncsymposium.org">http://asyncsymposium.org</a>

NATW' 20 – IEEE North Atlantic Test Workshop Albany, NY May 18-20, 2020 http://natw.ieee.org

ISCA' 20 – Int' I Symposium on Computer Architecture Virtual May 30 – Jun 3, 2020 <a href="https://iscaconf.org/isca2020/">https://iscaconf.org/isca2020/</a>

LCTES' 20 – ACM Int' I Conference on Languages Compilers, Tools and Theory of Embedded Systems
London, UK
Jun 15-20, 2020
<a href="https://conf.researchr.org/home/LCTES-2020">https://conf.researchr.org/home/LCTES-2020</a>

ISVLSI' 20 – IEEE Computer Society Annual Symposium on VLSI Limassol, Cyprus Jul 6-8, 2020 http://www.isvlsi.org

ICDCS'20 – IEEE Int'l Conference on Distributed Computing Systems Singapore Jul 8-10, 2019 https://icdcs2020.sq

DAC' 20 – Design Automation Conference San Francisco, CA Jul 19-23, 2020 http://www.dac.com/

ISLPED' 20 – ACM/IEEE Int' I Symposium on Low Power Electronics and Design Boston, MA Aug 10-12, 2020 <a href="http://www.islped.org">http://www.islped.org</a>

GLSVLSI' 20 – ACM Great Lakes Symposium on VLSI Beijing, China Sept xxxx, 2020 http://www.glsvlsi.org ISCAS'20 – IEEE Int'l Symposium on Circuits and Systems Seville, Spain Oct 11-14, 2020 <a href="http://iscas2020.org">http://iscas2020.org</a>

HOST'20 – IEEE Int' I Symposium on Hardware-Oriented Security and Trust San Jose, CA
TBD (postponed later this year)
<a href="http://www.hostsymposium.org">http://www.hostsymposium.org</a>

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# Call for Papers - 2020 CVPR Workshop on Low-Power Computer Vision

2020 CVPR Workshop on Low-Power Computer Vision

Call for Papers (Three Tracks)

- 1. Solutions for Low-Power Computer Vision
- 2. Grand Challenges in Low-Power Computer Vision
- 3. Poster for Low-Power Computer Vision

Track 1: Solutions for Low-Power Computer Vision:

Computer vision technologies have made impressive progress in recent years, but often at the expense of increasingly complex models needing more and more computational and storage resources. This workshop aims to improve the energy efficiency of computer vision solutions for running on systems with stringent resource constraints, for example, mobile phones, edge devices, Internet of Things, drones, or renewable energy systems. Efficient computer vision can enable many new applications (e.g., wildlife observation) powered by ambient renewable energy (e.g., solar, vibration, and wind). This workshop will discuss the state of the art of low-power computer vision, challenges in creating efficient vision solutions, promising technologies that can achieve the goals, methods to acquire and label data, benchmarks and metrics to evaluate progress and success. Authors are encouraged to present innovation in any part of the entire system, such as new hardware components, new algorithms, new methods for system integration, new semiconductor devices, and new computing paradigms. This workshop emphasizes "system-level" solutions with implementations for demonstrations and experiments. Conceptual designs or solutions for individual components without integration into functional systems are discouraged.

Authors are encouraged to discuss the following issues in their papers:

Description of the vision problem

Description of the solution

Description of the connections between low-power and computer vision

Description of the data for evaluation

Description of the system requirements (for example, but not limited to, solar powered, autonomous robots, drones)

Description of the entire system

Metrics for evaluation

Comparison with the state-of-the-art

Description of the procedure to reproduce the results

Track 2: Grand Challenges in Low-Power Computer Vision:

Competitions are widely adopted in academia, industry, and government to propel technology forward. Well-known competitions include the DARPA Autonomous Vehicle Challenge and the Space X prize. The competitions have been attributed as the accelerators of making significant progress in

the technologies. This workshop solicits papers that describe future competition in low-power computer vision. Authors are encouraged to think boldly, imagining competitions a la "Grand Challenge" or "X Prize". The winners' solutions (hardware, software, or some combination) should be far beyond today's available technologies.

Authors are encouraged to discuss the following issues in their papers:

Description of the challenge and why it is worth the community's efforts for several years Description of the state-of-the-art (the challenge should be far beyond today's technology but achievable)

Description of the connections between low-power and computer vision

Description of how people that can benefit from the technologies

Description of the market size in billions of dollars per year (if applicable)

Description of the data (e.g., image, video, with or without captions, etc.)

Methods to acquire the data and methods for scoring

Paths toward solving the problems. Do they need innovation in vision algorithms? Hardware?

Software? Will non-traditional systems be needed? Why?

Description about copyright and privacy (if applicable)

Methods to annotate the data (if applicable, forgetting the ground truth)

Constraints of hardware (if applicable, e.g., weight and size)

Minimum or maximum requirements (if applicable, e.g., accuracy and execution time)

#### Track 3: Posters for Low-Power Computer Vision:

The poster track is designed for projects that can benefit from an interactive setting between authors and audience. Authors may choose this format to present projects that may have, for example, demonstrations or user participation. Students may take advantage of this format and solicit suggestions or critiques of their projects. Researchers and practitioners from industry may present their projects and recruit users. The topics can be on either solutions for low-power computer vision or grand challenges in low-power computer vision. Works-in-progress are welcome.

Authors are encouraged to discuss the following issues in their papers:

Description of the vision problem

Description of the low-power solution

Description of the connections between low-power and computer vision

Description of the stage of this project

Description of the demonstration (if applicable)

#### Submission:

All submissions must be in PDF format. Submissions are limited to eight pages (tracks 1 and 2) or two pages (track 3), including all figures and tables. References are not included in the page limit. All submitted papers will be double-blind reviewed. Authors must not reveal their identities. Please refer to the Author Guidelines (<a href="http://cvpr2020.thecvf.com/submission/main-conference/author-quidelines#call-for...">http://cvpr2020.thecvf.com/submission/main-conference/author-quidelines#call-for...</a>)

The papers selected from Tracks 1 and 2 may be in the form of oral presentations or posters (in the event of a large number of outstanding papers). The papers selected from Track 3 will be in the form of posters. If a paper in Track 1 or 2 is selected for a poster, the authors will need to shorten the paper to two pages.

Important dates (Anywhere On Earth)

Online paper submission: 2020/03/27 (will not be extended)

Notification to authors: 2020/04/10

Final version: 2020/04/17 (This is a deadline set by CVPR)

Submission site: <a href="https://cmt3.research.microsoft.com/LPCV2020">https://cmt3.research.microsoft.com/LPCV2020</a>

**Student Travel Grants** 

Travel grants will be available to students. Details will be available in April.

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# Call for EiC Nominations ACM TODAES

ACM Transactions on Design Automation of Electronic Systems

The term of the current Editor-in-Chief (EiC) of the ACM Transactions on Design Automation of Electronic Systems (TODAES) is coming to an end, and the ACM Publications Board has set up a nominating committee to assist the Board in selecting the next EiC. ACM TODAES publishes recent significant results of research and development efforts in the area of design automation of electronic systems. It intends to provide comprehensive coverage of innovative works concerning the specification, design, analysis, simulation, testing, and evaluation of very large scale integrated electronic systems, emphasizing a computer science/engineering orientation.

Nominations, including self-nominations, are invited for a three-year term as TODAES EiC, beginning in June 2020. The EiC appointment may be renewed at most one time. This is an entirely voluntary position, but ACM will provide appropriate administrative support.

Appointed by the ACM Publications Board, EiCs of ACM journals are delegated full responsibility for the editorial management of the journal consistent with the journal's charter and general ACM policies. The Board relies on EiCs to ensure that the content of the journal is of high quality and that the editorial review process is both timely and fair. He/she has the final say on acceptance of papers, size of the Editorial Board, and appointment of Associate Editors. The EiC is expected to adhere to the commitments expressed in the policy on Rights and Responsibilities in ACM Publishing. For more information about the role of the EiC, see ACM's Evaluation Criteria for Editors-in-Chief.

Nominations should include a vita along with a brief statement of why the nominee should be considered. Self-nominations are encouraged, and should include a statement of the candidate's vision for the future development of TODAES. The deadline for submitting nominations is March 15, 2020, although nominations will continue to be accepted until the position is filled.

Please send all nominations to the nominating committee chair, Shiyan Hu (S.Hu@soton.ac.uk), with the subject line: "EiC Nomination for ACM TODAES" and make sure that you receive a confirmation.

The search committee members are:

Shiyan Hu, University of Southampton, Chair Duane Boning, MIT Rajesh Gupta, University of California, San Diego Subhasish Mitra, Stanford University Sanjit Seshia, University of California, Berkeley Lothar Thiele, ETH Zurich

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# **Technical Activities**

(1) "Covid-19: Industry Visibility Becomes Impaired" Infineon, Applied Materials and Broadcom have withdrawn their 2020 outlook. Others, including On Semi and NXP, are reducing guidance numbers.

#### [https://www.eetasia.com/news/article/Covid-19-Industry-Visibility-Becomes-Impair...]

(2) "Huagiangbei Gets Back to Work"

Huaqiangbei is Shenzhen's built-in ecosystem where design, manufacturing and supply chain come together in tight proximity. EE Times' colleague in Shenzhen visited there earlier this month to observe the recovery in Huaqiangbei.

[https://www.eetasia.com/news/article/Huanqiangbei-Gets-Back-to-Work]

- (3) "EDA 2019 results; EUV-based DRAMs; supercomputers; fast charging batteries; image sensors" [https://www10.edacafe.com/blogs/editorial/]
- (4) "The 4 cities competing to fully implement autonomous vehicles" [https://iot.eetimes.com/the-4-cities-competing-to-fully-implement-autonomous-veh...]

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(1) Part-Time Lecturer Pool - Electrical Engineering and Computer Science

From: University of California, Berkeley

Description: The Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley invites applications for a pool of qualified temporary instructors to teach Electrical Engineering or Computer Science courses should an opening arise. These are not tenure-track positions – selected candidates will hold the title of Lecturer. Screening of applicants is ongoing and will continue as needed. The number of positions varies from semester to semester, depending on the needs of the department.

More information can be found at <a href="https://computeroxy.com/lecturer-in-electrical-engineering-and-computer-science">https://computeroxy.com/lecturer-in-electrical-engineering-and-computer-science</a>,i9181.html (Please input the whole link.)

(2) Adjunct Professor in Computer Science and Engineering

From: University of California San Diego

Description: The UC San Diego Department of Computer Science and Engineering (CSE) invites applications for an Adjunct Professor position at Full Professor rank. The department is looking for exceptional candidates in the area of Architecture of Large-Scale Systems, preferably with extensive industry experience building, designing, implementing, and deploying Large-Scale Databases atscale. We are looking for applicants with outstanding research credentials. Successful applicants are expected to lead a vigorous research program and will be required to teach university students. We are particularly seeking faculty passionate about working with graduate students and training the next generation of researchers.

More information can be found at <a href="https://computeroxy.com/adjunct-professor-of-computer-science-and-engineering">https://computeroxy.com/adjunct-professor-of-computer-science-and-engineering</a>, i9190.html (Please input the whole link.)

(3) Assistant Professor of Computer Science and Engineering

From: Ohio State University College of Engineering

Description can be found at <a href="https://computeroxy.com/assistant-professor-of-computer-science-and-engineering">https://computeroxy.com/assistant-professor-of-computer-science-and-engineering</a>,i9244.html (Please input the whole link.)

(4) Research Fellow in Electrical Power Systems

From: School of Electronics and Computer Science, University of Southampton Description can be found at <a href="https://jobs.soton.ac.uk/Vacancy.aspx?ref=1252820FP">https://jobs.soton.ac.uk/Vacancy.aspx?ref=1252820FP</a>

(5) Tenure-Track Faculty Position in Artificial Intelligence

From: The University of Mons, Belgium

Description: The University of Mons announces the opening of a full-time tenure-track faculty position in artificial intelligence at the assistant professor level. The position is opened jointly in the Faculty of Science and the Faculty of Engineering, with a starting date of September 1, 2020. In a first stage, the person will be appointed for a period of three years, which can be extended with two extra years. The definitive appointment will be decided during or at the end of this period. The appointed person will take the lead of a new research group in the Department of Computer Science in the Faculty of Science.

All additional information can be obtained from Prof. Christian Michaux, Dean of the Faculty of Science (christian.michaux@umons.ac.be), and from Prof. Christine Renotte, Dean of the Faculty of Engineering (christine.renotte@umons.ac.be).

(6) Professor / Associate Professor / Assistant Professor of Microelectronics

From: Southern University of Science and Technology in Shenzhen China

Description: School of Microelectronics (SME) , National Exemplary School of Microelectronics, Southern University of Science and Technology (SUSTech) invites highly qualified candidates to fill multiple tenure-track/tenured faculty positions in the areas of (but not limited) Emerging Microelectronic Devices (Wide-bandgap, Nonvolatile memory, MEMS Sensor), and IC-Chip Designs (Future Computing/Communication/Biomedical SoC).

For more information, please visit: <a href="http://ohr.sustc.edu.cn/sustczp/product/recruit/a.do?">http://ohr.sustc.edu.cn/sustczp/product/recruit/a.do?</a> <a href="mailto:action=toZPGWList2&entityld...">action=toZPGWList2&entityld...</a>.

(7) Tenure-Track Faculty Positions in Engineering

From: Zhejiang University, China

Description: Tenure-Track Faculty Positions in Engineering in Zhejiang University The Zhejiang University-University of Illinois at Urbana-Champaign Institute (the ZJU-UIUC Institute) invites highly qualified candidates for multiple tenure-track faculty positions at all levels and in areas of engineering and science that match its multidisciplinary mission. The ZJU-UIUC Institute is an engineering college on the new Zhejiang University (ZJU) International Campus, China, about 120 km southwest of Shanghai. The Institute has interests that address but are not limited to interdisciplinary topics exemplified by data science, artificial intelligence, internets of things, advanced communication, digital manufacturing, systems and networking, transportation electrification, micronano-electronics and photonics, Terahertz, smart power, biotechnology, nanotechnology, and atomic-scale materials, intelligent infrastructure. Classes and student activities are conducted in English.

For more information, please visit <a href="https://my.zjui.illinois.edu/submit/login.asp">https://my.zjui.illinois.edu/submit/login.asp</a>

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