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The resource for EDA Professionals

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Comments from the Editors

Dear ACM/SIGDA member,

We are excited to present to you the March e-newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from upcoming conference and funding deadlines, hot research topics to news from our community. Get involved and contact us if you want to contribute an article or announcement.

From this month, we are taking the duty as Editors-in-Chief of SIGDA E-Newsletter. Firstly thanks are due to our predecessors Prof. Aida Todri-Sanial and Prof. Yu Wang. They have served as EiC for the last year. Their great contributions to the e-newsletter are highly appreciated.

The newsletter will continue evolving to ensure full advantage is taken of the rapidly changing world. Please let us know what you think.

Happy reading!

Debjit Sinha

Keni Qiu

Editors-in-Chief, SIGDA E-News

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SIGDA News

(1) "Covid-19 Is Crimping the Electronics Industry"
[https://www.eetimes.com/covid-19-is-crimping-the-electronics-industry/]

The coronavirus outbreak in China is already affecting the electronics industry business. A new analysis published by IDC predicts a drop in smartphone sales in China of more than 30% in the January-March quarter. Canalys Researchers estimated that “Technology vendors are likely to pause marketing activities; they are unlikely to focus on launching new products, including 5G devices. “It will take vendors time to change their roadmap for product launches in China, and this will probably decrease the number of 5G smartphones distributed in 2020.

(2) "Supply Chain Poised for Coronavirus Disruption"
[https://www.eetimes.com/supply-chain-poised-for-coronavirus-disruption/]

Global technology companies have made employees their priority as the deadly coronavirus spreads across the Chinese mainland and beyond. Late Thursday afternoon, the World Health Organization (WHO) declared the virus a global public health emergency.

(3) "Production Resuming in China, But Travel Bans Cripple Shipping"
[https://www.eetimes.com/production-resuming-in-china-but-travel-bans-cripple-shi...]

China’s manufacturing plants have resumed work, but it is far from business as usual. Will it ever be? Will China be able to remove the stigmata of the vicious Covid-19, and achieve full recovery any time soon? With analysts on the ground in Asia, market research firm Yole Développement has a clear understanding of the supply chain disruptions triggered by the coronavirus outbreak.

(4) "Chip Industry Dodges Direct Impact of Coronavirus"
[https://www.eetimes.com/report-chip-industry-dodges-direct-impact-of-coronavirus...]

The semiconductor industry appears to have escaped the direct impact of the coronavirus crisis so far, but the market is likely to suffer the repercussions as the outbreak slows or suspends production among electronics manufacturers, according to Omdia.

(5) "UK Press on with 5G & Huawei, But Place a Cap on Traffic, Equipment"
[https://www.eetimes.com/uk-press-on-with-5g-huawei-but-place-a-cap-on-traffic-eq...]

Keen not to halt the progress of its 5G rollout, the U.K. government Tuesday concluded its telecoms supply chain review and issued guidance on how to treat 'high-risk vendors' (HRVs) such as Huawei as part of a new set of telecoms security requirements. It said these vendors should be excluded from sensitive 'core' parts of 5G and gigabit-capable networks.

(6) "Arm Leaps Into TinyML With New Cores"
[https://www.eetimes.com/arm-leaps-into-tinyml-with-new-cores/]

Arm has unveiled two new IP cores designed to power machine learning in endpoint devices, IoT devices and other low-power, cost-sensitive applications. The Cortex-M55 microcontroller core is the first to use Arm's Helium vector processing technology, while the Ethos-U55 machine learning accelerator is a micro-version of the company's existing Ethos NPU (neural processing unit) family. The two cores are designed to be used together, though they can also be used separately.

(7) "TI's First Automotive SoC with an AI Accelerator Launches"
[https://www.eetimes.com/tis-first-automotive-soc-with-an-ai-accelerator-launches...]

TI has added a dedicated AI accelerator to one of its automotive SoCs for the first time, in a move that perfectly illustrates the growing adoption of deep learning techniques in automotive ADAS systems. The new deep learning block is based on TI's brand new C7x DSP IP plus an in-house-developed matrix multiplication accelerator.

(8) "XMOS adapts Xcore into AIoT 'crossover processor'"
[https://www.eetimes.com/xmos-adapts-xcore-into-aiot-crossover-processor/]

XMOS has adapted its Xcore processor core for machine learning, creating a crossover processor for AIoT applications. The Xcore.ai will be available from $1.

(9) "Thermal and Vibration Energy Harvesting for IoT devices"
[https://www.eetimes.com/thermal-and-vibration-energy-harvesting-for-iot-devices/]

Achieving so-called zero-power sensors will require harvesting energy from sources in the environment. After narrowing down one's options to available sources, the next criteria will be the amount of energy available and the amount of energy needed.

(10) "Legacy DRAM Finds Its Way to the Edge"
[https://www.eetimes.com/legacy-dram-finds-its-way-to-the-edge/]

There has been plenty of discussion about how emerging memories might address opportunities created by the Internet of things (IoT) and obviate the need for expensive options such as SRAM. One company thinks low-pin DRAM may be the answer.

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"What is" Column

What is Cyber-Physical Checkpointing and Recovery?

Fanxin Kong

Assistant Professor

Department of Electrical Engineering and Computer Science

Syracuse University

Cyber-Physical Systems (CPS) such as autonomous systems, industrial robots, medical devices, and power systems, tightly couple computing and communication processes with sensing and actuation components that interact with the physical world. Accurate and timely interaction is fundamental for functional and safe CPS. Achieving such interaction heavily depends on the consistency between cyber and physical spaces, e.g., cyber values accurately reflect physical states and cyber inputs are timely actuated in physical systems. However, this cyber-physical consistency is vulnerable to

many adversarial factors including environmental uncertainty, faults, attacks, and human errors. Cyber-physical inconsistency can cause misled control decisions that drift off the physical system to perform dangerous actions.

Cyber-Physical Checkpointing and Recovery have been recently proposed as a solution framework that reconstructs cyber-physical consistency and restores the physical system to safe states [1]. By this framework, cyber-physical states (e.g., state estimates and control inputs) are occasionally checkpointed when the system operates normally. Then, after cyber-physical inconsistency is detected, a two-step recovery is activated. The first step is cyber recovery, that is, reconstructing state estimates or control inputs to match the current physical states. Based on the reconstructed information, the second step is physical recovery, that is, controlling the physical system to safe states or even the current reference states.

Following this framework, our previous work proposes techniques to realize checkpointing and recovery [1, 2]. First, a checkpointing protocol is designed on how to record system states for recovery. The protocol introduces a sliding window that accommodates attack-detection delay to improve the correctness of stored states. Second, a new concept of roll-forward recovery is proposed, that is, rolling the system forward starting from a consistent historical system state to a reference state. The recovery technique adopts model-based prediction for state estimate reconstruction and control. Third, a use case of the proposed techniques is presented to deal with compromised sensor measurements. Finally, the effectiveness is illustrated by the use of our design in an unmanned vehicle case study. There are several issues left unsolved. First, conceptual and theoretical fundamentals of cyber-physical consistency are not well defined. Second, our previous work records all system states at all times, which incurs large overhead to the system. Third, the model-based recovery has accumulated prediction errors over time and thus cause the system to drift off little by little in the presence of sensor attacks.

To sum up, responding to adversarial factors such as attacks and faults, cyber-physical checkpointing and recovery is a solution framework that restores cyber-physical consistency and the physical system to a safe state. While our previous work proposes techniques to realize the framework, many future works are needed to address the above issues.

References

[1] Kong, Fanxin, Meng Xu, James Weimer, Oleg Sokolsky, and Insup Lee. "Cyber-physical system checkpointing and recovery." In 2018 ACM/IEEE 9th International Conference on Cyber-Physical Systems (ICCPS), pp. 22-31. IEEE, 2018.

[2] Kong, Fanxin, Oleg Sokolsky, James Weimer, and Insup Lee. "State Consistencies for Cyber-Physical System Recovery." In the 2nd Workshop on Cyber-Physical Systems Security and Resilience (CPS-SR). 2019.

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Paper Submission Deadlines

ISLPED'20 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
Boston, MA
Deadline: Mar 9, 2020 (Abstracts due: Mar 2, 2020)
Aug 10-12, 2020
http://www.islped.org

MICRO'20 – IEEE/ACM Int'l Symposium on Microarchitecture
Athens, Greece
Deadline: Apr 3, 2020 (Abstracts due: Mar 27, 2020)
Oct 17-21, 2020
http://www.microarch.org/micro53

ESWEEK'20 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)
Hamburg, Germany
Deadline: Apr 10, 2020 (Abstracts due: Apr 3, 2020)
Sept 20-25, 2020
http://www.esweek.org

BodyNets'20 – Int'l Conference on Body Area Networks
Tallinn, Estonia
Deadline: Apr 15, 2020
Oct 21-22, 2020
http://www.bodynets.org

PACT'20 - Int'l Conference on Parallel Architectures and Compilation
Techniques

Atlanta, GA
Deadline: Apr 17, 2020 (Abstracts due: Apr 10, 2020)
Oct 3-7, 2020
http://www.pactconf.org

VLSI-SoC'20 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Salt Lake City, UT
Deadline: Apr 27, 2020 (Abstracts due: Apr 20, 2020)
Oct 5-7, 2020
http://www.vlsi-soc.com

NOCS'20 – IEEE/ACM Int'l Symposium on Networks-on-Chip (co-located with ESWEEK'20)
Hamburg, Germany
Deadline: May 1, 2020 (Abstracts due: Apr 24, 2020)
Sept 24-25, 2020
http://nocs2020.engr.uky.edu/

ICCAD'20 – IEEE/ACM Int'l Conference on Computer-Aided Design
San Diego, CA
Deadline: May 28, 2020 (Abstracts due: May 21, 2020)
Nov 2-5, 2020
http://www.iccad.com

HiPC'20 – IEEE Int'l Conference on High Performance Computing, Data, And Analytics
Pune, India
Deadline: June 16, 2020 (Abstracts due: June 9, 2020)
Dec 16-19, 2020
http://www.hipc.org

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Upcoming Symposia, Conferences and Workshops

DATE'20 - Design Automation and Test in Europe
Grenoble, France
Mar 9-13, 2020
http://www.date-conference.com

TAU'20 – ACM Int'l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems
Monterey, CA
Mar 19-20, 2020
http://www.tauworkshop.com

ISQED'20 - Int'l Symposium on Quality Electronic Design
Santa Clara, CA
Mar 25-26, 2020
http://www.isqed.org

ISPD'20 – ACM Int'l Symposium on Physical Design
San Francisco, CA
Mar 29 - Apr 1, 2020
http://www.ispd.cc

HOST'20 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
San Jose, CA
May 4-7, 2020
http://www.hostsymposium.org

ASYNC'20 – IEEE Int'l Symposium on Asynchronous Circuits and Systems Snowbird, UT
May 17-20, 2020
http://asyncsymposium.org

ISCAS'20 – IEEE Int'l Symposium on Circuits and Systems
Seville, Spain
May 17-20, 2020
http://iscas2020.org

NATW'20 – IEEE North Atlantic Test Workshop
Albany, NY
May 18-20, 2020
http://natw.ieee.org

GLSVLSI'20 – ACM Great Lakes Symposium on VLSI
Beijing, China
May 27-29, 2020
http://www.glsvlsi.org

ISCA'20 – Int'l Symposium on Computer Architecture
Valencia, Spain
May 30 – Jun 3, 2020
https://iscaconf.org

IWBDA'20 - Int'l Workshop on Bio-Design Automation
Worcester, MA
Jun 8-10, 2020
http://www.iwbdaconf.org/2020

LCTES'20 – ACM Int'l Conference on Languages Compilers, Tools and Theory of Embedded Systems
London, UK
Jun 15-20, 2020
https://conf.researchr.org/home/LCTES-2020

ISVLSI'20 – IEEE Computer Society Annual Symposium on VLSI
Limassol, Cyprus
Jul 6-8, 2020
http://www.isvlsi.org

ICDCS'20 – IEEE Int'l Conference on Distributed Computing Systems
Singapore
Jul 8-10, 2019
https://icdcs2020.sg

DAC'20 – Design Automation Conference
San Francisco, CA
Jul 19-23, 2020
http://www.dac.com/

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SIGDA Awards

Best Paper Awards at ASP-DAC 2020: 25th Asia and South Pacific Design Automation Conference,
https://aspdac2020.github.io/aspdac20/program/index.html

1."Towards Area-Efficient Optical Networks: An FFT-based Architecture" by Jiaqi Gu, Zheng Zhao, Chenghao Feng, Mingjie Liu, Ray T. Chen and David Z.Pan - Univ. of Texas at Austin, USA.

2."Equivalent Capacitance Guided Dummy Fill Insertion for Timing and Manufacturability" by Sheng-Jung Yu, Chen-Chien Kao, Chia-Han Huang and Iris Hui-Rui Jiang - National Taiwan University, Taiwan.

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Research Spotlight

Hello readers,
In this edition of Researcher spotlight we have a discussion with Dr. Aida Todri-Sanial, Director of Research, CNRS, France (www.lirmm.fr/~todri). She received her B.S.E.E from Bradley University, Peoria, M.S.E.E. from Long Beach State University, California and Ph.D. in Electrical and Computer Engineering from University of California, Santa Barbara.

1. Can you share with us some of the research areas you are working on?

My research interest is primarily focused on the physical design of nanoscale devices and interconnects for low-power integrated circuits and systems. So far, I have worked on many projects, but there are several things that they all have in common. First, nearly all my research projects involved investigating the physical characteristics and behavior that governed the electrical and thermal properties of the devices and interconnects. A second common denominator is that even though my work has performed design and optimization of circuits in an “academic context", the goals were targeted toward industrial needs. Lastly, the design methods and techniques developed, they were all based on the mathematical description of the circuits that enabled to formulate close-form analytical problems that can be solved efficiently and accurately.

Over the years my research has evolved and my current research activities are in four main directions: (1) exploring the full potential of 1D (carbon nanotubes) and 2D TMDs by developing physics-driven modeling (atomistic to TCAD models) and simulation for devices, interconnects, and circuits, (2) physical design for 3D-stacked and monolithic 3D, (3) neuromorphic computing based on phase-change memristor elements, and (4) our recent activity on computer-aided design for quantum computing. These activities are conducted in the framework of a large collaborative research project funded by the European Commission such as EU H2020 CONNECT, EU H2020 SMARTVISTA and EU H2020 NEURONN in collaboration with industrial and academic partners. By the way, I am currently recruiting on these topics, so I encourage students to get in contact if any of these topics spark their interest.

2. Carbon nanotubes seem a promising candidate for silicon applications, particularly as a replacement for copper interconnects. However, to achieve comparable performance CNTs require doping and not encounter alignment issues. Is this likely to morph into parameter variation challenges as currently seen in advanced technologies? If so, what needs to be accomplished by industry and research communities early on?

Interconnect innovation with novel material such as carbon nanotubes has been the focus of extensive research with the goal of propagating terabits/second at femtoJoule per bit. Carbon nanotubes have sparked a lot of interest because of their desirable properties such as large electron mean free path, mechanical strength, high thermal conductivity, and large current carrying capacity. The advent of carbon nanotube as new material for back-end of line interconnects is a direct result of active research in academia, research laboratories, and industry over the past decade. Today, carbon nanotube integration takes many forms depending on the applications. In this research topic, we have investigated doping of carbon nanotubes both experimentally (CNT growth and doping) and by DFT modeling. We have found that doping is an efficient method to mitigate the impact of defects on carbon nanotubes and improve its conductance. As our goal is to grow carbon nanotubes at low temperatures for CMOS compatibility, defects are a big challenge which degrades their quality. With doping, we believe that is can be a simple yet efficient method that can allow further investigations of carbon nanotubes for back-end-of-line.

3. Over the years, you are also a proactive member of the ACM SIGDA community. Can you share with us your experience?

I have been volunteering as co-EiC for ACM SIGDA e-newsletter since 2016, and it has been one of my favorite and rewarding outreach activities. My role together with co-EiC Prof. Yu Wang, has been to provide timely information to our community, broaden participation and to engage our community. We put together an excellent editorial board with AE members from the US, Europe and Asia, representing diverse young professionals and women scientists. After three years, it is time to pass the flambeau, and I am thrilled to hand over the leadership to the new Co-EiCs, Debjit Sinha and Keni Qiu. Overall, it has been a great experience to engage with our community, and I will look forward to the monthly e-newsletters.

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Tools announced at WOSET 2019

ACT: Asynchronous Digital Flow
http://github.com/asyncvlsi/act

AMC: Asynchronous Memory Compiler
https://github.com/asyncvlsi/AMC

BLASYS: A Tool for Approximate Logic Synthesis
https://github.com/scale-lab/BLASYS

CirKit: A logic synthesis framework
https://github.com/msoeken/cirkit

EvoApproxLib: Extended Library of Approximate Arithmetic Circuits

https://ehw.fit.vutbr.cz/evoapproxlib/

Fault: An Open Source DFT Toolchain
https://github.com/Cloud-V/Fault

LiveHD: A Productive Open-Source Hardware Development Flow
https://github.com/masc-ucsc/livehd

LSOracle: Automated AIG/MIG-based Logic Synthesis
https://github.com/LNIS-Projects/LSOracle

OGRE: Open-Source LEF/DEF Global Router
https://github.com/Cloud-V/OGRE

OpenDB: Physical Database for EDA tool development
https://github.com/The-OpenROAD-Project/OpenDB

OpenFPGA: An Open-source FPGA IP Generator
https://github.com/LNIS-Projects/OpenFPGA

OpeNPDN: Neural networks for automated synthesis of Power Delivery Networks
https://github.com/The-OpenROAD-Project/OpeNPDN

RTLog: A HDL together with a Compiler to create Relative Timing circuits.
https://github.com/VLSI-UTN-FRBA/RTLog

Skeletor: A tool for generating RTL templates from specification
https://github.com/jaquerinte/Skeletor

The EPFL logic synthesis libraries: A collection of modular open-source C++ libraries for logic synthesis
https://github.com/lsils/lstools-showcase

TherMOS: A thermal model for self-heating in advanced MOS devices
https://github.com/VidyaChhabria/TherMOS

Verible: A SystemVerilog parser, linter and formatter.
https://github.com/google/verible

Xyce: A parallel, SPICE-compatible analog circuit simulator
https://xyce.sandia.gov

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Call for Nominations - ACM/IEEE A. Richard Newton Award

Call for Nomination (Deadline Feb. 1, 2020)

ACM/IEEE A. Richard Newton Technical Impact Award in Electronic Design Automation

Presented by the ACM Special Interest Group on Design Automation and the IEEE Council on Electronic Design Automation

Description: To honor a person or persons for an outstanding technical contribution within the scope of electronic design automation, as evidenced by a paper published at least ten years before the presentation of the award. The award is based on the impact of the contribution.

Background: The IEEE Council on Electronic Design Automation sponsors or co-sponsors the Donald Pederson Award for best paper in IEEE Transactions on Computer-Aided Design, the William McCalla Award for best paper at the International Conference on Computer-Aided Design, and the Phil Kaufman Award for Distinguished Contributions to Electronic Design Automation (with the EDA Consortium). The Kaufmann Award is the major award normally given to a senior person in the field for distinguished contributions. The other IEEE CEDA awards recognize outstanding publications. The ACM Special Interest Group on Design Automation sponsors or co-sponsors the ACM Transactions on Design Automation of Electronic Systems Best Paper Award, the William McCalla Award for best paper at the International Conference on Computer-Aided Design, and two awards for outstanding graduate students and new faculty. The ACM Outstanding Ph.D. Dissertation Award is given each year to a graduating Ph.D. student in recognition of his/her thesis contributions to advancement in the EDA field. The SIGDA Outstanding New Faculty Award is also given each

year to a junior faculty whose research contributions are likely to make a significant impact.

The proposed A. Richard Newton Technical Impact Award complements these awards and is intended for contributors whose impact is recognized over a significant period of time. The Award honors A. Richard Newton, a luminary in the design automation area in academia and industry, faculty contributor and advisor to many of the leaders in the field, company founder, and dean of engineering at the University of California, Berkeley, who died in 2007. Professor Newton embodied the idea of technical impact which this award seeks to recognize.

Nominee Solicitation: The call for nominees will be published each fall by email to members of participating societies, by flyers and publicity at the International Conference on Computer-Aided Design, and on the web sites of the IEEE Council on Electronic Design Automation (and its participating societies) and the web site of ACM's Special Interest Group on Design Automation, in the SIGDA and CEDA newsletters, and in IEEE Design & Test magazine.

The nomination form will ask for (i) the paper and authors to be honored, (ii) a proposed citation, (iii) a description of the impact of the paper over at least a ten-year period, including evidence in support of the significant intellectual contributions and high impact in the field of the nominated paper. At a minimum, supporting material should cover these aspects of impact:
- impact on the research community reflected in citations
- impact on the practitioner community via evidence of usage of the described technology in an industrial setting impact on the EDA community as a whole via evidence of starting new directions and spawning new ideas.
In addition to the evidence of impact, the nomination form will include biographical information (including education and employment), professional activities, publications, and recognition. Three endorsements attesting to the impact of the work may be included.

The nomination materials should be emailed by the deadline to SIGDA-Award@acm.org (Subject: ACM/IEEE A. Richard Newton Technical Impact Award in Electronic Design Automation).

Award Committee: Selection will be made by a committee comprised of three members designated by the IEEE Council on Electronic Design Automation and three members designated by the ACM Special Interest Group in Design Automation. The Committee will meet in February of each year to review nominations and make a recommendation to the sponsoring Council and SIG by March 15. Following approval by the sponsors, the committee will contact the recipient to ensure that the award will be accepted.

All standard conflicts of interest regulations as stated in ACM policy will be applied (see https://awards.acm.org/conflict-of-interest). Any awards committee members will recuse themselves from consideration of any candidates where a conflict of interest may exist.

Schedule: The call for nominees will be published annually in the fall, especially at the International Conference on Computer-Aided Design (see above). The submission deadline is Feb 1 of each year. The Awards Committee will meet in February to determine the winning paper and award recipient(s). The sponsors will approve the selection by March 15. The recipient will be notified by April 1. The award will be presented in June/July at the ACM/IEEE Design Automation Conference.

Selection/Basis for Judging: This award honors an individual or a group which has made an outstanding technical contribution in the scope of electronic design automation through a paper published at least ten years before the award is presented. The award is based on the impact of the paper as indicated above. Nominees from universities, industry, and government worldwide will be considered and encouraged. The award is not the best paper or initial original contribution award. Instead, the prime consideration will be the impact on technology, industry, and education, and on working electronic designers and engineers. Such impact might include a research result that is widely cited or spawned much innovative thinking, or a new technique that has been put into wide use in practice.

Presentation: The award includes a cash prize of $1500 to be split among the awardees. The award will be formally presented annually at the ACM/IEEE Design Automation Conference.

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Call for Papers - IEEE COINS 2020

IEEE COINS 2020: IEEE International Conference on Omni-Layer Intelligent Systems

Barcelona, Spain | July 27-29, 2020
IEEE CEDA | IEEE ComSoc | IEEE RAS | IEEE CASS | IEEE IoT
Submission Deadline: March 6, 2020
http://coinsconf.com

COINS is the premier conference devoted to Omni-layer techniques for smart AI-driven IoT systems, by identifying new

perspectives and highlighting impending research issues and challenges. COINS 2020 will include a multi-disciplinary cross-domain program from technical research papers, to panels, workshops, tutorials and forums on the latest technology developments and innovations in the fields of IoT, AI, Big Data, Blockchain, Cloud Computing, and Cybersecurity. COINS 2020 encourages high-quality technical papers and proposals related to one or more of the following topics (but not limited to):

Topical Area Tracks:
1) Internet of Things: From Device, to Edge, and Cloud
2) Circuit and System Design for Future Artificial Intelligence, Internet of Things and Big Data
3) Cloud Computing
4) Big Data
5) Artificial Intelligence, Machine Learning, Cognitive Computing, and Advanced Analytics
6) Distributed Ledger Technologies and Blockchain
7) Design Automation in AI & IoT Era: From Chips to Systems
8) Cyber Security and Privacy

Vertical Tracks:
1) Smart City
2) Industry 4.0
3) Intelligent IoT Healthcare
4) Agriculture
5) Automotive, Transportation, and Logistics
6) Smart Energy
7) Telecom
8) Smart Retail

Special Tracks:
1) Critical System Design
2) Data Monetization and Data Sharing
3) IoT Operating Systems
4) European Projects on Intelligent Systems

SUBMISSION INFORMATION
Submission Site: https://coinsconf.com
Technical Paper Submission Deadline: 6 March 2020

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Call for EiC Nominations ACM TODAES

ACM Transactions on Design Automation of Electronic Systems

The term of the current Editor-in-Chief (EiC) of the ACM Transactions on Design Automation of Electronic Systems (TODAES) is coming to an end, and the ACM Publications Board has set up a nominating committee to assist the Board in selecting the next EiC. ACM TODAES publishes recent significant results of research and development efforts in the area of design automation of electronic systems. It intends to provide comprehensive coverage of innovative works concerning the specification, design, analysis, simulation, testing, and evaluation of very large scale integrated electronic systems, emphasizing a computer science/engineering orientation.

Nominations, including self-nominations, are invited for a three-year term as TODAES EiC, beginning in June 2020. The EiC appointment may be renewed at most one time. This is an entirely voluntary position, but ACM will provide appropriate administrative support.

Appointed by the ACM Publications Board, EiCs of ACM journals are delegated full responsibility for the editorial management of the journal consistent with the journal's charter and general ACM policies. The Board relies on EiCs to ensure that the content of the journal is of high quality and that the editorial review process is both timely and fair. He/she has the final say on acceptance of papers, size of the Editorial Board, and appointment of Associate Editors. The EiC is expected to adhere to the commitments expressed in the policy on Rights and Responsibilities in ACM Publishing. For more information about the role of the EiC, see ACM's Evaluation Criteria for Editors-in-Chief.

Nominations should include a vita along with a brief statement of why the nominee should be considered. Self-nominations are encouraged, and should include a statement of the candidate's vision for the future development of TODAES. The deadline for submitting nominations is March 15, 2020, although nominations will continue to be accepted until the position is filled.

Please send all nominations to the nominating committee chair, Shiyan Hu <S.Hu@soton.ac.uk>, with the subject line: “EiC Nomination for ACM TODAES” and make sure that you receive a confirmation.

The search committee members are:

Shiyan Hu, University of Southampton, Chair
Duane Boning, MIT
Rajesh Gupta, University of California, San Diego
Subhasish Mitra, Stanford University
Sanjit Seshia, University of California, Berkeley
Lothar Thiele, ETH Zurich

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Circulation: 2,700

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