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The resource for EDA Professionals

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Comments from the Editors

Dear ACM/SIGDA member,

We are excited to present to you the December e-newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from upcoming conference and funding deadlines, hot research topics to news from our community. Get involved and contact us if you want to contribute an article or announcement.

The newsletter is evolving, let us know what you think.

Happy reading!

Aida Todri-Sanial
Yu Wang
Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit http://www.acm.org/renew or call between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or 1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org

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SIGDA News

(1) "Companies Clash over AI at the Edge"
[https://www.eetimes.com/document.asp?doc_id=1335247]

Micron Technology last week officially opened a key global development center in Hyderabad, India, and plans to recruit up to 2,000 people over the next couple of years. Speaking at the event, Micron president and chief executive officer Sanjay Mehrotra said Hyderabad offered the best combination of talent and environment for its development center to become one of the top three to four sites for Micron globally. It hopes the diversity of talent in India will help drive breakthroughs in artificial intelligence (AI), machine learning and emerging memory.

(2) "Benchmark Scores Reveal Who's Winning the AI Inference Race"
[https://www.eetimes.com/document.asp?doc_id=1335270]

MLPerf has released the first set of benchmark scores for its inference benchmark, following scores from the training benchmark which were released earlier this year. Compared to the training round, which currently has 63 entries from 5 companies, many more companies submitted results. In total there

were more than 500 scores verified from 14 organizations. This included figures from several startups, while some high-profile startups were still noticeably absent.

(3) "Microsoft Incorporates Graphcore AI Chips in Azure Cloud"
[https://www.eetimes.com/document.asp?doc_id=1335297]

Graphcore's AI accelerator chip, the Colossus intelligence processing unit (IPU) is now available for customers to use as part of Microsoft's Azure cloud platform. This is the first time any major cloud service provider has publicly offered customers the opportunity to run their data on an accelerator from any of the dozens of AI chip startups and as such, it represents a big win for Graphcore. Microsoft has said access will initially be prioritized for customers who are "pushing the boundaries of machine learning".

(4) "Nvidia Shrinks AI 'Supercomputer' to Credit Card Size"
[https://www.eetimes.com/document.asp?doc_id=1335268]

Nvidia has launched the Jetson Xavier NX, a new board that features the computing power of the AGX Xavier in the form factor of the Jetson Nano (70 x 45mm). The Xavier NX board can achieve 14 to 21 TOPS INT8 performance at power budgets between 10W and 15W, respectively. This amount of processing power would enable running multiple neural networks in parallel, and processing data from multiple high-resolution image sensors simultaneously, according to the company.

(5) "Nvidia Delivers on Promise to Support Arm"
[https://www.eetimes.com/document.asp?doc_id=1335307]

Nvidia introduced a reference design platform for GPU-accelerated Arm-based servers. Arm, Ampere, Cray, Fujitsu, HPE, and Marvell are all going to build such servers for a variety of applications including, of course, supercomputing, the GPU vendor announced at Supercomputing 2019 in Denver.

(6) "FPGA Acceleration Card Delivers on Bandwidth, Speed, and Flexibility"
[https://www.eetimes.com/document.asp?doc_id=1335253]

In most current devices, silicon-based CMOS chips are used for computing. Silicon in advanced communications systems is driven to its limits — limits that translate into thermal problems. This is why the current 5G mobile devices on the market become very hot during use and turn off after a short time.

(7) "LTE Positioning Spinout Targets Precision Location Services"
[https://www.eetimes.com/document.asp?doc_id=1335250]

PHY Wireless has been spun out from its parent Acorn Technologies to provide intellectual property (IP) cores enabling location-of-things services on LTE and 5G cellular networks.

(8) "Carbon Nanotube FETs Exceed 100GHz for RF Applications"
[https://www.eetimes.com/document.asp?doc_id=1335322]

Carbonics, Inc., has demonstrated a wafer-scalable approach for producing an array of aligned carbon nanotube (CNT) FETs with performance exceeding 100 GHz and linearity of 10dB.

(9) "Energy Harvesting is The Future of Power Supply"
[https://www.eetimes.com/document.asp?doc_id=1335269]

Energy-saving initiatives are a key driver in the growth of the energy harvesting equipment market. Companies are considering a whole series of tools necessary for energy harvesting to satisfy the growing demand for energy.

(10) "Thermal Analysis for Power Devices"
[https://www.eetimes.com/document.asp?doc_id=1335267]

Understanding the thermal performance of integrated circuits, whether they are microcontrollers, FPGAs, or processors, has always been essential to avoid the overheating that can cause circuit malfunctions. The miniaturization of electronic systems and the diffusion of components that generate a lot of heat, such as LEDs, make the role of thermal analysis more and more important as a tool to guarantee the good functioning and reliability of products.

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"What is" Column

What is Weakly-Hard Real-Time System?

Qi Zhu

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Real-time systems are pervasive. From antilock break system to air traffic controller, time plays a critical role in the correctness of these systems. Thus, the systems are designed in a way that the passage of time is explicitly linked with the evolution of the systems, allowing engineers to reason about the predictability of their behaviors. A central problem in real-time systems is the scheduling of real-time tasks, either statically or dynamically, so that the tasks are guaranteed to meet their deadlines. The traditional consideration of deadline misses leads to the categorization of hard timing and soft/firm timing constraints. With hard timing constraints, deadline misses are not allowed, so systems must be designed conservatively to anticipate for the worst case (e.g. with worst-case execution time). This often leads to either over-provisioning of system resources or rigid designs. On the other hand, with soft/firm timing constraints, deadline misses can be tolerated in the sense that system performance degrades when deadline misses occur. The drawback, however, is that they are not suitable for mission-critical settings due to the lack of deterministic guarantees.

Weakly-hard timing constraints were proposed to address these challenges. The notion of weakly-hard constraints was first formally introduced in [1], where the system is specified to tolerate at most m deadline misses in K consecutive task instances. Compared with hard timing constraints, weakly-hard constraints are more flexible in that they can tolerate occasional deadline misses. At the same time, the so-called (m, K) constraint bounds the degree of nondeterminism that a system can have in terms of tasks meeting their deadlines and therefore does not compromise predictability in principle. Existing works on weakly-hard constraints typically focus on system schedulability such as [2, 3]. More recently, several techniques have been proposed to reason about system-level properties assuming (m, K) constraints can be met. Notable examples include analyzing and optimizing control stability [4], verifying safety properties of nonlinear control systems [5], and analyzing properties of networked systems [6]. Together with schedulability analysis techniques, they open up the possibility of cross-layer analysis of weakly-hard systems in terms of control, scheduling, security, and other objectives [7]. Thus, adopting a weakly-hard perspective to system design can significantly expand the feasible design space, facilitate system changes where resources might need to be reallocated for adding new functionalities or fixing existing ones, and enable tradeoffs amongst a variety of design considerations such as timing, performance, cost, safety, security, and extensibility.

[1] G. Bernat, A. Burns, and A. Liamosi. Weakly hard real-time systems. IEEE Transactions on Computers, 50(4):308—321, 2001.

[2] S. Quinton, M. Hanke, and R. Ernst, Formal analysis of sporadic overload in real-time systems. In ACM/IEEE Design, Automation, and Test in Europe Conference (DATE), 2012.

[3] H. Choi, H. Kim, and Q. Zhu. Job-class-level fixed priority scheduling of weakly-hard real-time systems. In IEEE Real-Time Technology and Applications Symposium (RTAS), 2019.

[4] G. Frehse, A. Hamann, S. Quinton, and M. Woehrle. Formal analysis of timing effects on closed-loop properties of control software. In IEEE Real-Time Systems Symposium (RTSS), 2014.

[5] C. Huang, W. Li, and Q. Zhu. Formal verification of weakly-hard systems. In ACM International Conference on Hybrid Systems: Computation and Control (HSCC), 2019.

[6] K. Wardega, and W. Li. Application-aware scheduling of networked applications over the low-power wireless bus. In ACM/IEEE Design, Automation, and Test in Europe Conference (DATE), 2020.

[7] H. Liang, Z. Wang, D. Roy, S. Dey, S. Chakraborty, and Q. Zhu. Security-driven codesign with weakly-hard constraints for real-time embedded systems. In IEEE International Conference on Computer Design (ICCD), 2019.

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Paper Submission Deadlines

TAU'20 — ACM Int'l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems
Monterey, CA
Deadline: Dec 1, 2019
Mar 19–20, 2020
http://www.tauworkshop.com

GLSVLSI'20 — ACM Great Lakes Symposium on VLSI
Beijing, China
Deadline: Dec 17, 2019
May 27–29, 2020
http://www.glsvlsi.org

ASYNC'20 — IEEE Int'l Symposium on Asynchronous Circuits and Systems

Snowbird, UT
Deadline: Dec 19, 2019 (Abstracts due: Dec 5, 2019)
May 17–20, 2020
http://asyncsymposium.org

ICDCS'20 — IEEE Int'l Conference on Distributed Computing Systems
Singapore
Deadline: Jan 13, 2020 (Abstracts due: Jan 6, 2020)
Jul 8–10, 2019
https://icdcs2020.sg

NATW'20 — IEEE North Atlantic Test Workshop

Albany, NY
Deadline: Feb 7, 2020
May 18–20, 2020
http://natw.ieee.org

ISVLSI'20 – IEEE Computer Society Annual Symposium on VLSI
Limassol, Cyprus
Deadline: Feb 20, 2010
Jul 6–8, 2020
http://www.isvlsi.org

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Upcoming Symposia, Conferences and Workshops

ICPADS'19 – IEEE Int'l Conference on Parallel and Distributed Systems
Tianjin, China
Dec 4–6, 2019
http://www.icpads2019.cn

FPT'19 – Int'l Conference on Field–Programmable Technology
Tianjin, China
Dec 9–13, 2019
http://icfpt.org

ISED'19 – Int'l Symposium on Electronic System Design
Kollam, India
Dec 13–15, 2019
http://isedconf.org

iSES'19 – IEEE Int'l Symposium on Smart Electronic Systems
Rourkela, India
Dec 16–18, 2019
http://www.ieee-ises.org

HiPC'19 – IEEE Int'l Conference on High Performance Computing
Hyderabad, India
Dec 17–20, 2019
http://www.hipc.org

VLSID'20 – Embedded and VLSI Design Conference
Bengaluru, India
Jan 4–8, 2020
http://www.vlsidesignconference.org

ASP–DAC'20 – Asia and South Pacific Design Automation Conference
Beijing, China
Jan 13–16, 2020
www.aspdac.com

HiPEAC'20: Int'l Conference on High Performance Embedded Architectures & Compilers
Balogna, Italy
Jan 20–22, 2020

https://www.hipeac.net

ISSCC'20 — IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Feb 16–20, 2020
http://isscc.org

FPGA'20 — ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Seaside, CA
Feb 24–26, 2020
http://www.isfpga.org

DATE'20 – Design Automation and Test in Europe
Grenoble, France
Mar 9–13, 2020
http://www.date-conference.com

ISQED'20 – Int'l Symposium on Quality Electronic Design
Santa Clara, CA
Mar 25–26, 2020
http://www.isqed.org

ISPD'20 — ACM Int'l Symposium on Physical Design
San Francisco, CA
Mar 29 – Apr 1, 2020
http://www.ispd.cc

HOST'20 — IEEE Int'l Symposium on Hardware-Oriented Security and Trust
San Jose, CA
May 4–7, 2020
http://www.hostsymposium.org

ISCAS'20 — IEEE Int'l Symposium on Circuits and Systems
Seville, Spain
May 17–20, 2020
http://iscas2020.org

ISCA'20 — Int'l Symposium on Computer Architecture
Valencia, Spain
May 30 — Jun 3, 2020
https://iscaconf.org

IWBDA'20 – Int'l Workshop on Bio-Design Automation
Worcester, MA
Jun 8–10, 2020
http://www.iwbdaconf.org/2020

DAC'20 — Design Automation Conference
San Francisco, CA
Jul 19–23, 2020
http://www.dac.com/

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SIGDA Awards

Best Paper Awards at ESWEEK 2019: EMBEDDED SYSTEMS WEEK, https://www.esweek.org/awards

CASES
“An Ultra-Low Energy Human Activity Recognition Accelerator for Wearable Health Applications” by Ganapati Bhat, Yigit Tuncel, Sizhe An, Hyung Gyu Lee and Umit Ogras.

CODES+ISSS
“Achieving Lossless Accuracy with Lossy Programming for Efficient Neural-Network Training on NVM-Based Systems” by Wei-Chen Wang, Yuan-Hao Chang, Tei-Wei Kuo, Chien-Chung Ho, Yu-Ming Chang, Hung-Sheng Chang.

EMSOFT
“Deriving Equations from Sensor Data Using Dimensional Function Synthesis” by Sam Willis, Youchao Wang, Vasileios Tsoutsouras, Phillip Stanley-Marbell.

CASES Test-of-Time
“Process Cruise Control: Event-driven Clock Scaling for Dynamic Power Management”, 2002, by Andreas Weissel and Frank Bellosa.

CODES+ISS Test-of-Time
“Transaction level modeling: an overview”, 2003, by Lukai Cai and Daniel Gajski.

EMSOFT Test-of-Time
“Reliable and Precise WCET Determination for a
Real-Life Processor, 2001, by Christian Ferdinand, Reinhold Heckmann, Marc Langenbach, Florian Martin, Michael Schmidt, Henrik Theiling, Stephan Thesing and Reinhard Wilhelm.

Best Paper Award at NOCS 2019: 13th IEEE/ACM International Symposium on Networks-on-Chip, https://www.engr.colostate.edu/nocs2019/program/

“NoC-enabled Software/Hardware Co-Design Framework for Accelerating k-mer Counting”, by Biresh Kumar Joardar (Washington State University), Priyanka Ghosh (Washington State University), Partha Pratim Pande (Washington State University), Ananth Kalyanaraman (Washington State University), and Sriram Krishnamoorthy (Pacific Northwest National Laboratory).

Best Paper Award at MEMOCODE'19, 17th ACM-IEEE International Conference on Formal Methods and Models for System Design, https://www.engr.colostate.edu/nocs2019/program/

“Logical Specification and Uniform Synthesis of Robust Controllers”, by Paritosh Pandya and Amol Wakankar.
“Detecting Security Leaks in Hybrid Systems with Information Flow Analysis”, by Luan Nguyen, Gautam Mohan, James Weimer, Oleg Sokolsky, Insup Lee and Rajeev Alur.

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Call for Papers: IEEE Design and Test – Special issue on Open-Source EDA

Aim and Scope:
In the 80s the academic community produced several very high-quality EDA tools that spawned the EDA industry. Tools like Spice, Espresso, and SIS became the foundation of EDA companies. Open-source tools enable rapid innovation and create an ecosystem for scientific development. In recent years, the cost and difficulty of IC design in advanced nodes have stifled hardware design innovation and have raised unprecedented barriers to bringing new design ideas to the marketplace. Unlike the thriving software community, which enjoys a large number of open-source operating systems, compilers, libraries and applications, the hardware community lacks such a modern ecosystem. With the advent of Open Silicon IP Ecosystems like RISCV, Chips Alliance, and Free Silicon Foundation, the time has come to reinvigorate the open-source movement in EDA tools. The EDA open-source landscape is fragmented and a full open-source EDA flow is lacking. Recent programs from governmental agencies aim to jump-start development of open-source EDA tools to reduce the cost and turnaround time of hardware design. Open-source development also leads to special challenges such as physical design kit support and tool maintenance and support.
Topics of Interest:

Specific topics of interest include but are not limited to the following:
SoC architecture and design tools
Simulation tools
Automatic accelerator and high-level synthesis
Tools for security and system verification
Logic synthesis
P & R tools (Floorplanning, Placement, Physical synthesis, Clock tree synthesis, Global and detailed Routing and Layout finishing)
Analysis tools: parasitics, timing, power, IR drop and thermal
Pervasive machine learning for EDA flows
Automated analog design
Design for emerging technologies

Submission Guidelines:
Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at https://mc.manuscriptcentral.com/dandt

A specific special issue category will be available and selectable from a menu. All articles will undergo the standard IEEE Design & Test review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere.

Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Resources for links to Submission Guidelines Basics and Electronic Submission Guidelines and requirements.

Accepted articles must meet the following three criteria:
Technical novelty: all articles must meet the standard criteria of technical contribution, in terms of novel methodologies and algorithms with demonstrated superiority over existing methods.
Open-source and interoperability: all submissions must include a link to their open-source code. All open-source tools must use standard input and output file formats or databases to ensure interoperability in EDA flow.
High impact on EDA flows: acceptance priority will be given to articles that address missing or critical

needs within the existing open-source ecosystem.

Submissions that heavily overlap with prior conference publications by the same authors will be given low acceptance priority.

Schedule:
Initial Submission Deadline: 15 January 2020
Notification First Round: 1 March 2020
Revision Submission: 1 April 2020
Final Notification: 1 May 2020
Final Version Due: 15 May 2020

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Tools announced at WOSET 2019

ACT: Asynchronous Digital Flow
http://github.com/asyncvlsi/act

AMC: Asynchronous Memory Compiler
https://github.com/asyncvlsi/AMC

BLASYS: A Tool for Approximate Logic Synthesis
https://github.com/scale-lab/BLASYS

CirKit: A logic synthesis framework
https://github.com/msoeken/cirkit

EvoApproxLib: Extended Library of Approximate Arithmetic Circuits
https://ehw.fit.vutbr.cz/evoapproxlib/

Fault: An Open Source DFT Toolchain
https://github.com/Cloud-V/Fault

LiveHD: A Productive Open-Source Hardware Development Flow
https://github.com/masc-ucsc/livehd

LSOracle: Automated AIG/MIG-based Logic Synthesis
https://github.com/LNIS-Projects/LSOracle

OGRE: Open-Source LEF/DEF Global Router
https://github.com/Cloud-V/OGRE

OpenDB: Physical Database for EDA tool development
https://github.com/The-OpenROAD-Project/OpenDB

OpenFPGA: An Open-source FPGA IP Generator
https://github.com/LNIS-Projects/OpenFPGA

OpeNPDN: Neural networks for automated synthesis of Power Delivery Networks
https://github.com/The-OpenROAD-Project/OpeNPDN

RTLog: A HDL together with a Compiler to create Relative Timing circuits.
https://github.com/VLSI-UTN-FRBA/RTLog

Skeletor: A tool for generating RTL templates from specification
https://github.com/jaquerinte/Skeletor

The EPFL logic synthesis libraries: A collection of modular open-source C++ libraries for logic synthesis
https://github.com/lsils/lstools-showcase

TherMOS: A thermal model for self-heating in advanced MOS devices
https://github.com/VidyaChhabria/TherMOS

Verible: A SystemVerilog parser, linter and formatter.
https://github.com/google/verible

Xyce: A parallel, SPICE-compatible analog circuit simulator
https://xyce.sandia.gov

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Call for Papers: GLSVLSI 2020

The 30th Edition of the ACM Great Lakes Symposium on VLSI (GLSVLSI), Sponsored by ACM SIGDA

Conference dates: May 27-29, 2020
Location:Beijing, China

http://www.glsvlsi.org/

The 30th edition of GLSVLSI will be held in Beijing China, unpublished papers describing research in the general areas of VLSI and hardware design are solicited. Please visit http://www.glsvlsi.org/ for more information. In addition to the traditional topic areas of GLSVLSI listed below, papers are solicited for a special theme of “In-Memory Processing for future electronics”.

- Track 1: VLSI Design
- Track 2: VLSI Circuits and Power Aware Design
- Track 3: Computer-Aided Design (CAD)
- Track 4: Testing, Reliability, Fault-Tolerance
- Track 5: Emerging Computing & Post-CMOS Technologies
- Track 6: Hardware Security
- Track 7: VLSI for Machine Learning and Artificial Intelligence
- Track 8: Microelectronic Systems Education

Details of the requirements that each track places on submitted papers can be found on the conference website.

Paper Submission Guidelines

Authors are invited to submit full-length (6 pages maximum), original, unpublished papers along with an

abstract of at most 200 words. To enable blind review, the author list should be omitted from the main document. Previously published papers or papers currently under review for other conferences/journals should NOT be submitted and will not be considered. Electronic submission in PDF format to the http://www.glsvlsi.org/ website is required. Author and contact information (name, affiliation, mailing address, telephone, fax, e-mail) must be entered during the submission process.

Paper Format: Submissions should be in camera-ready two-column format, following the ACM proceedings specifications located at: http://www.acm.org/publications/proceedings-template-16dec2016 and the classification system detailed at: http://www.acm.org/publications/class-2012

Paper Publication and Presenter Registration: Papers will be accepted for regular or poster presentation at the symposium. Every accepted paper MUST have at least one author registered to the symposium by the time the camera-ready paper is submitted; at least one of the authors is also expected to attend the symposium and present the paper.

Important Dates

Paper submission deadline: December 17, 2019 (9pm EST)
Acceptance Notification: February 18, 2020
Camera-Ready Paper Due: March 13, 2020
Special Session Proposal submission deadline: January 15, 2020
Notification of acceptance/rejection: January 31, 2020

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