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The resource for EDA Professionals

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Comments from the Editors

Dear ACM/SIGDA member,

We are excited to present to you the November e-newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from upcoming conference and funding deadlines, hot research topics to news from our community. Get involved and contact us if you want to contribute an article or announcement.

The newsletter is evolving, let us know what you think.

Happy reading!

Aida Todri-Sanial
Yu Wang
Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit http://www.acm.org/renew or call between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or 1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org

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SIGDA News

(1) "Micron Opens Global Development Center in India"
[https://www.eetimes.com/document.asp?doc_id=1335179]

Micron Technology last week officially opened a key global development center in Hyderabad, India, and plans to recruit up to 2,000 people over the next couple of years. Speaking at the event, Micron president and chief executive officer Sanjay Mehrotra said Hyderabad offered the best combination of talent and environment for its development center to become one of the top three to four sites for Micron globally. It hopes the diversity of talent in India will help drive breakthroughs in artificial intelligence (AI), machine learning and emerging memory.

(2) "Arm Responds to RISC-V, and More"
[https://www.eetimes.com/document.asp?doc_id=1335196]

Arm CEO Simon Segars announced the changes in his opening keynote at Arm TechCon. After decades of tight control over the Arm instruction set architecture (ISA), Arm has finally decided that it can allow its licensees to build their own custom instructions, which are often useful to accelerate specialized workloads.

(3) "NXP Touts Auto-Grade AI Toolkit for AVs"
[https://www.eetimes.com/document.asp?doc_id=1335187]

NXP Semiconductors rolled out this week a new deep learning toolkit called eIQ Auto. NXP is seeking to set itself apart from competitors by making its tools "automotive-quality." NXP's goal is to make it easier for AV designers to implement deep learning in vehicles.

(4) "NXP Unveils GHz MCU, Hints at FinFET MCU"
[https://www.eetimes.com/document.asp?doc_id=1335162]

Gigahertz is where no microcontroller vendor has gone before, but FinFET is even deeper in outer space for the MCU sector. MCU powerhouse NXP, determined to outpace its peers, has crashed through the GHz barrier and might be on its way to a FinFET MCU.

(5) "TSMC Boosts Capital Expenditures on 5G Demand"
[https://www.eetimes.com/document.asp?doc_id=1335213]

TSMC has raised its capital expenditures for this year to as much as $15 billion on an improved outlook for 5G smartphones and related networking equipment.

(6) "III-V semiconductors-based Chips for 5G mobile"
[https://www.eetimes.com/document.asp?doc_id=1335227]

In most current devices, silicon-based CMOS chips are used for computing. Silicon in advanced communications systems is driven to its limits — limits that translate into thermal problems. This is why the current 5G mobile devices on the market become very hot during use and turn off after a short time.

(7) "Micron Claims Fastest SSD; Buys AI Startup"
[https://www.eetimes.com/document.asp?doc_id=1335231]

Micron Technology introduced what it claims is the world's fastest solid state drive (SSD), and also announced the acquisition of FWDNXT (pronounced "forward next"), a startup that specializes in neural networking with a product lineup that includes a series of inference engine modules based on Xilinx FPGAs.

(8) "Renesas MCUs Target Secure IoT With Open Software Platform"
[https://www.eetimes.com/document.asp?doc_id=1335198]

Renesas Electronics Corp. has launched a new family of microcontrollers (MCUs) targeting secure, scalable Internet of things (IoT) applications with an open software platform enabling customers to develop IoT endpoints with a wide range of partners or leveraging existing legacy software platforms.

(9) "Why Hardware Security is the Preferred Choice for IIoT"
[https://www.eetimes.com/document.asp?doc_id=1335189]

Industrial automation will be one of the biggest areas of spending on the internet of things (IoT) in

2019. So, how can the devices connecting the systems to the network be trusted, and what's the best way to ensure that their industrial IoT (IIoT) systems are secure: software or hardware? In this article, we look at the case for hardware-based security as the preferred choice for IIoT and its benefits beyond just security — such as time to market, scalability, and performance and manufacturing flexibility.

(10) "Lightweight AI Tracks Suspects Between Cameras"
[https://www.eetimes.com/document.asp?doc_id=1335233]

A novel neural network developed at the University of Surrey for the re-identification of people in video surveillance footage is small enough to be deployed on edge devices such as security cameras, its inventors say. They also claim it is more adept at the task than human camera operators.

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"What is" Column

What is Flexible Hybrid Electronics?
by Ganapati M. Bhat and Umit Y. Ogras

Umit Y. Ogras,
Associate Professor,
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ, USA

Flexible electronics refer to integrated circuits implemented on bendable, rollable, conformable, or elastic substrates which are lighter, thinner, and inexpensive to manufacture [1]. Physical advantages and low cost of flexible electronics have resulted in significant interest in recent years. Successful examples include flexible displays, sensors, photovoltaic cells, wireless tags, batteries, programmable logic circuits, simple micro-controllers, analog-to-digital converters (ADC) and radio frequency transmitters [2]. Due to its form factor advantages, flexible electronics technology has the potential to transform computing by enabling bendable and stretchable wearable systems at a low cost.

Flexible electronics still suffer from significantly lower performance and larger parameter variations compared to silicon CMOS circuits in spite of impressive progress in recent years [2]. For example, silicon technology offers more than 1 GHz frequency with features sizes as low as 14 nm, whereas the feature sizes of thin-film transistors (TFT) range from 8 µm to 50 µm, and frequencies hardly reach 10 MHz. Flexible hybrid electronics (FHE) technology addresses this problem by integrating rigid silicon integrated circuits and printed electronics. FHE can be used to combine rigid and flexible resources judiciously such that we can bridge the gap between the performance of flexible devices and conventional CMOS while preserving the form factor benefits of flexible electronics. Hence, FHE can drive the next big leap forward in device form factor, similar to the shift from laptop computers to smartphones and other hand-held devices.

FHE devices have attracted significant research interest in recent years due to their ability to combine the advantages of flexible electronics and conventional CMOS technologies. For instance, integration of CMOS devices on flexible substrates has recently been demonstrated at research centers including ASU Flexible Display Center. Circuits for interfacing flexible electronics and CMOS ICs have been also proposed [3]. Similarly, Khan et al. [4] developed devices that use FHE to monitor vital signs, such as heart rate and body temperature. While these studies show the advantages of FHE devices, there is still a need to develop standard methodologies for the design of FHE systems.

Design of FHE systems presents new challenges since we need to account for flexibility of the device as a new design metric [5]. For example, the flexibility of an FHE device changes as a function of the substrate used, the number and size of rigid components, the location of components, and the

flexibility of flexible components. Therefore, there is also a need for new flexibility-aware design tools and methodologies [6]. This will enable the development of standard design tools for FHE similar to the ones available for CMOS circuit design [7].
In summary, FHE can deliver a richer experience than currently available rigid wearable with the help of (1) physical flexibility (e.g., rollable or foldable devices become possible) and (2) wearable sensors that enable machines to understand and assist their users. Potential applications with high impact include human-computer interaction, health monitoring, gesture recognition, activity recognition, and patient rehabilitation.

References

[1] William S Wong and Alberto Salleo. Flexible Electronics: Materials and Applications, volume 24. Springer, 2009.

[2] Tsung-Ching Jim Huang et al. Design, Automation, and Test for Low-Power and Reliable Flexible Electronics. Found. and Trends in EDA, 9(2):99–210, 2015.

[3] Tiffany Moy et al. Thin-film Circuits for Scalable Interfacing between Large-area Electronics and CMOS ICs. In Device Research Conf., pages 271–272, 2014.

[4] Yasser Khan et al. Flexible Hybrid Electronics: Direct Interfacing of Soft and Hard Electronics for Wearable Health Monitoring. Advanced Functional Materials, 26(47):8764–8775, 2016.

[5] Ujjwal Gupta et al. Flexibility-Aware System-on-Polymer (SoP): Concept to Prototype. IEEE Trans. Multi-Scale Comput. Syst., 3(1):36–49, 2017.

[6] Ganapati Bhat et al. Multi-Objective Design Optimization for Flexible Hybrid Electronics. In Proc. of ICCAD, pages 1–8, 2016.

[7] Tsung-Ching Huang et al. Process Design Kit and Design Automation for Flexible Hybrid Electronics. In 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE), pages 36–41, 2019.

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Paper Submission Deadlines

ISPD’ 20 – ACM Int’ l Symposium on Physical Design
San Francisco, CA
Deadline: Oct 7, 2019 (Abstracts due: Sep 30, 2019)
Mar 29 - Apr 1, 2020
http://www.ispd.cc

ISCAS'20 – IEEE Int'l Symposium on Circuits and Systems
Seville, Spain
Deadline: Oct 20, 2019
May 17-20, 2020
http://iscas2020.org

HOST'20 – IEEE Int’ l Symposium on Hardware-Oriented Security and Trust
San Jose, CA
Deadline: Nov 15, 2019
May 4-7, 2020
http://www.hostsymposium.org

ISCA' 20 – Int' l Symposium on Computer Architecture
Valencia, Spain
Deadline: Nov 26, 2019 (Abstracts due: Nov 19, 2019)
May 30 – Jun 3, 2020
https://iscaconf.org

DAC' 20 – Design Automation Conference
San Francisco, CA
Deadline: Nov 27, 2019 (Abstracts due: Nov 21, 2019)
Jul 19-23, 2020
http://www.dac.com/

TAU' 20 – ACM Int' l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems
Monterey, CA
Deadline: Dec 1, 2019
Mar 19-20, 2020
http://www.tauworkshop.com

ISVLSI' 19 – IEEE Computer Society Annual Symposium on VLSI
Limassol, Cyprus
Deadline: Feb 20, 2010
Jul 6-8, 2020
http://www.isvlsi.org

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Upcoming Symposia, Conferences and Workshops

BodyNets'19 – Int' l Conference on Body Area Networks
Florence, Italy
Oct 2-3, 2019
http://www.bodynets.org

VLSI-SoC' 19 – IFIP/IEEE Int' l Conference on Very Large Scale Integration
Cuzco, Peru
Oct 6-9, 2019
www.vlsi-soc.com

MEMOCODE'19 – ACM/IEEE Int' l Conference on Formal Methods and Models for Codesign
San Diego, CA
Oct 9-11, 2019
https://memocode.github.io/2019

MICRO'19 – IEEE/ACM Int'l Symposium on Microarchitecture
Columbus, OH
Oct 12-16, 2019
http://www.microarch.org/micro52

ESWEEK'19 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)
New York, NY
Oct 13-18, 2019
http://www.esweek.org

NOCS'19 – IEEE/ACM Int' l Symposium on Networks-on-Chip

New York, NY
Oct 17-18, 2019
https://www.engr.colostate.edu/nocs2019

BIOCAS'19 – Biomedical Circuits and Systems Conference
Nara, Japan
Oct 17-19, 2019
http://www.biocas2018.org

ICCAD' 19 – IEEE/ACM Int' l Conference on Computer-Aided Design
Westminster, CO
Nov 4-7, 2019
http://www.iccad.com

WOSET' 19 – Workshop on Open Source EDA Technology (co-located with ICCAD' 19)
Westminster, CO
Nov 7, 2019
http://woset.org

ICPADS'19 – IEEE Int'l Conference on Parallel and Distributed Systems
Tianjin, China
Dec 4-6, 2019
http://www.icpads2019.cn

FPT'19 - Int'l Conference on Field-Programmable Technology
Tianjin, China
Dec 9-13, 2019
http://icfpt.org

ISED' 19 – Int' l Symposium on Electronic System Design
Kollam, India
Dec 13-15, 2019
http://isedconf.org

iSES' 19 – IEEE Int' l Symposium on Smart Electronic Systems
Rourkela, India
Dec 16-18, 2019
http://www.ieee-ises.org

HiPC'19 – IEEE Int'l Conference on High Performance Computing
Hyderabad, India
Dec 17-20, 2019
http://www.hipc.org

VLSID'20 – Embedded and VLSI Design Conference
Bengaluru, India
Jan 4-8, 2020
http://www.vlsidesignconference.org

ASP-DAC'20 - Asia and South Pacific Design Automation Conference
Beijing, China
Jan 13-16, 2020
www.aspdac.com

HiPEAC'20: Int'l Conference on High Performance Embedded Architectures & Compilers
Balogna, Italy

Jan 20-22, 2020
https://www.hipeac.net

ISSCC'20 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Feb 16-20, 2020
http://isscc.org

FPGA’ 20 – ACM/SIGDA Int’ l Symposium on Field-Programmable Gate Arrays
Seaside, CA
Feb 24-26, 2020
http://www.isfpga.org

DATE'20 - Design Automation and Test in Europe
Grenoble, France
Mar 9-13, 2020
http://www.date-conference.com

ISQED'20 - Int'l Symposium on Quality Electronic Design
Santa Clara, CA
Mar 25-26, 2020
http://www.isqed.org

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SIGDA Awards

Best Paper Awards at ESWEEK 2019: EMBEDDED SYSTEMS WEEK, https://www.esweek.org/awards

CASES
“An Ultra-Low Energy Human Activity Recognition Accelerator for Wearable Health Applications” by Ganapati Bhat, Yigit Tuncel, Sizhe An, Hyung Gyu Lee and Umit Ogras.

CODES+ISSS
“Achieving Lossless Accuracy with Lossy Programming for Efficient Neural-Network Training on NVM-Based Systems” by Wei-Chen Wang, Yuan-Hao Chang, Tei-Wei Kuo, Chien-Chung Ho, Yu-Ming Chang, Hung-Sheng Chang.

EMSOFT
“Deriving Equations from Sensor Data Using Dimensional Function Synthesis” by Sam Willis, Youchao Wang, Vasileios Tsoutsouras, Phillip Stanley-Marbell.

CASES Test-of-Time
“Process Cruise Control: Event-driven Clock Scaling for Dynamic Power Management”, 2002, by Andreas Weissel and Frank Bellosa.

CODES+ISS Test-of-Time
“Transaction level modeling: an overview”, 2003, by Lukai Cai and Daniel Gajski.

EMSOFT Test-of-Time
“Reliable and Precise WCET Determination for a Real-Life Processor, 2001, by Christian Ferdinand, Reinhold Heckmann, Marc Langenbach, Florian Martin, Michael Schmidt, Henrik Theiling, Stephan Thesing and Reinhard Wilhelm.

Best Paper Award at NOCS 2019: 13th IEEE/ACM International Symposium on Networks-on-Chip, https://www.engr.colostate.edu/nocs2019/program/

"NoC-enabled Software/Hardware Co-Design Framework for Accelerating k-mer Counting", by Biresh Kumar Joardar (Washington State University), Priyanka Ghosh (Washington State University), Partha Pratim Pande (Washington State University), Ananth Kalyanaraman (Washington State University), and Sriram Krishnamoorthy (Pacific Northwest National Laboratory).

Best Paper Award at MEMOCODE'19, 17th ACM-IEEE International Conference on Formal Methods and Models for System Design, https://www.engr.colostate.edu/nocs2019/program/

"Logical Specification and Uniform Synthesis of Robust Controllers", by Paritosh Pandya and Amol Wakankar.
"Detecting Security Leaks in Hybrid Systems with Information Flow Analysis", by Luan Nguyen, Gautam Mohan, James Weimer, Oleg Sokolsky, Insup Lee and Rajeev Alur.

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Call for Papers: WOSET 2019

Second Workshop on Open-Source EDA Technology (http://woset.org).
Co-located with ICCAD 2019, Nov 7,The Westin Westminster, Westminster CO.

This one-day workshop aims to galvanize the open-source EDA movement. The workshop will bring together EDA researchers who are committed to open-source principles to share their experiences and coordinate efforts towards developing a reliable, fully open- source EDA flow. The workshop will feature presentations that overview existing open-source tools, along with sessions and posters describing future planned EDA tools. The workshop will include a panel to brainstorm the current status and future challenges for open-source EDA, and to coordinate efforts and ensure quality and interoperability across open-source tools.

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Call for Papers: IEEE Design and Test - Special issue on Open-Source EDA

Aim and Scope:
In the 80s the academic community produced several very high-quality EDA tools that spawned the EDA industry. Tools like Spice, Espresso, and SIS became the foundation of EDA companies. Open-source tools enable rapid innovation and create an ecosystem for scientific development. In recent years, the cost and difficulty of IC design in advanced nodes have stifled hardware design innovation and have raised unprecedented barriers to bringing new design ideas to the marketplace. Unlike the thriving software community, which enjoys a large number of open-source operating systems, compilers, libraries and applications, the hardware community lacks such a modern ecosystem. With the advent of Open Silicon IP Ecosystems like RISCV, Chips Alliance, and Free Silicon Foundation, the time has come to reinvigorate the open-source movement in EDA tools. The EDA open-source landscape is fragmented and a full open-source EDA flow is lacking. Recent programs from governmental agencies aim to jump-start development of open-source EDA tools to reduce the cost and turnaround time of hardware design. Open-source development also leads to special challenges such as physical design kit support and tool maintenance and support.
Topics of Interest:

Specific topics of interest include but are not limited to the following:

SoC architecture and design tools
Simulation tools
Automatic accelerator and high-level synthesis
Tools for security and system verification
Logic synthesis
P & R tools (Floorplanning, Placement, Physical synthesis, Clock tree synthesis, Global and detailed Routing and Layout finishing)
Analysis tools: parasitics, timing, power, IR drop and thermal
Pervasive machine learning for EDA flows
Automated analog design
Design for emerging technologies

Submission Guidelines:
Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at
https://mc.manuscriptcentral.com/dandt

A specific special issue category will be available and selectable from a menu. All articles will undergo the standard IEEE Design & Test review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere.

Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Resources for links to Submission Guidelines Basics and Electronic Submission Guidelines and requirements.

Accepted articles must meet the following three criteria:
Technical novelty: all articles must meet the standard criteria of technical contribution, in terms of novel methodologies and algorithms with demonstrated superiority over existing methods.
Open-source and interoperability: all submissions must include a link to their open-source code. All open-source tools must use standard input and output file formats or databases to ensure interoperability in EDA flow.
High impact on EDA flows: acceptance priority will be given to articles that address missing or critical needs within the existing open-source ecosystem.

Submissions that heavily overlap with prior conference publications by the same authors will be given low acceptance priority.

Schedule:
Initial Submission Deadline: 15 January 2020
Notification First Round: 1 March 2020
Revision Submission: 1 April 2020
Final Notification: 1 May 2020
Final Version Due: 15 May 2020

Guest Editors:
Sherief Reda, Brown University, sherief_reda@brown.edu
Leon Stok, IBM, leonstok@us.ibm.com
Pierre-Emmanuel Gaillardon, University of Utah, pierre-emmanuel.gaillardon@utah.edu

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Call for Participation: SEC 2019

Dear Colleagues,

Join us on November 7 - 9, 2019 at the Hilton Crystal City at Washington Reagan National Airport in Arlington, VA to learn about the latest research related to edge computing.
The preliminary program is now available, featuring an outstanding combination of 2 keynotes, 1 panel, 20 peer-reviewd papers, 24 posters/demos, 3 workshops (ArchEdge, EdgeSP, HotWot), a PhD Student forum, a Women-in-Computing forum,
social networking & recruiting events, all packed into 3 intense days. The coverage and discussions on edge computing, vehicular edge system, and deep learning in edge systems will energize you with new ideas and business possibilities.

Early Registration Deadline is Oct 10, 2019!

Check out the Keynotes and Panels at http://acm-ieee-sec.org/2019/keynote%20and%20panel.php

Student travel grants from US NSF and IEEE Technical Committee on the Internet (TCI) are available at http://acm-ieee-sec.org/2019/index.php

We look forward to meeting you at SEC 2019!

General Co-Chairs
Songqing Chen, George Mason University
Ryokichi Onishi, Toyota

Program Co-Chairs
Ganesh Ananthanarayanan, Microsoft Research
Qun Li, College of William & Mary

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ACM TECS Call for Nominations new Editor-in-Chief

*** Call for Nominations
*** Editor-In-Chief
*** ACM Transactions on Embedded Computing Systems (TECS)

The term of the current Editor-in-Chief (EiC) of the ACM Transactions on Embedded Computing Systems (TECS) is coming to an end, and the ACM Publications Board has set up a nominating committee to assist the Board in selecting the next EiC. The design of embedded computing systems, both the software and hardware, increasingly relies on sophisticated algorithms, analytical models, and methodologies. ACM Transactions on Embedded Computing Systems (TECS) aims to present the leading work relating to the analysis, design, behavior, and experience with embedded computing systems.

Nominations, including self nominations, are invited for a three-year term as TECS EiC, beginning 2020. The EiC appointment may be renewed at most one time. This is an entirely voluntary position, but ACM will provide appropriate administrative support.
Appointed by the ACM Publications Board, Editors-in-Chief (EiCs) of ACM journals are delegated full responsibility for the editorial management of the journal consistent with the journal's charter and general ACM policies. The Board relies on EiCs to ensure that the content of the journal is of high quality and that the editorial review process is both timely and fair. He/she has final say on acceptance of papers, size of the Editorial Board, and appointment of Associate Editors. A complete list of responsibilities is found in the ACM Volunteer Editors Position Descriptions. Additional information can be found in the following documents:

· Rights and Responsibilities in ACM Publishing
· ACM's Evaluation Criteria for Editors-in-Chief
Nominations should include a vita along with a brief statement of why the nominee should be considered. Self-nominations are encouraged, and should include a statement of the candidate's vision for the future development of TECS. The deadline for submitting nominations is *** Oct. 31st, 2019 *** , although nominations will continue to be accepted until the position is filled.
Please send all nominations to the nominating committee chair, Jörg Henkel (henkel@kit.edu) with subject line: "EiC nomination ACM TECS" and make sure you receive a confirmation.
The search committee members are:
Jörg Henkel, Karlsruhe Institute of Technology, Chair
Petru Eles, Linkoping Univ., Sweden
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Christoph Kirsch, Univ. Salzburg, Austria
Tei-Wei Kuo, NTU, Taiwan
Partha Pande, Washington State Univ., USA
Sri Parameswaran, UNSW, Autralia

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CFP: Artificial Intelligence of Things Workshop

Internet of Things (IoT) is a disruptive technology that extends data collection to almost everything around us and enables them to react through intelligent data processing. Gartner estimates that the number of connected things will grow to over 20 billion by 2020. With recent innovative network and chip technology, devices are becoming smarter with increasing compute power, bandwidth, and storage available on the device. This enables intelligent decision making and information transfer through devices. Insights derived from data generated by IoT devices power new business scenarios and ensure long term success of existing business. Major IT solution providers have been investing in building IoT data platform to support customers to develop IoT solutions in different industry sectors such as smart cities, manufacturing, health care and transportation. These business scenarios impose technical challenges and opportunities in building intelligent cloud and edge solutions. This workshop provides a forum for researchers, data scientists and practitioners from both academia and industry to present the latest research results, share practical experience of building AI powered IoT solutions, and network with colleagues.

Topics

IoT is an interdisciplinary field that intersects with device, sensor network, stream analytics, and machine learning. AI for IoT is a workshop on IoT with its focus on technologies to enable machine learning algorithms to run on resource constrained, secure, and connected devices. The workshop encourages submissions of innovative technologies and applications that enable IoT scenarios. Topics of interest, include but not limited to:
• On device machine learning algorithms
• Real-time computer vision and speech processing
• Learning-enabled IoT applications
• AI for Edge computing
• AI for IoT security and privacy
• Low-power AI for IoT systems
• Distributed inferencing and learning
• Optimized Blockchain for IoT
• 5G and IoT

Format

The workshop will be a full day event with keynote, invited talks, technical paper presentation, and

project showcase.

Submissions

We solicit original papers in two formats – Technical Paper (6 pages) and project showcase (2 pages) in AAAI format. Submitted papers will be peer-reviewed and selected for presentation. Accepted papers will be published on the workshop' s website.

Submission site:
https://cmt3.research.microsoft.com/User/Login?ReturnUrl=%2FAIOTW2019%2FSubmissi...

Organizers

General Chair: Yiran Chen (Duke University)
Program Chairs: Jian Zhang (Microsoft) and Jian Tang (DiDi ChuXing)
Steering Committee: Jie Liu (Harbin Institute of Technology), Jieping Ye (DiDi Chuxing), Marilyn Claire Wolf (Georgia Tech), Mani Srivastava (UCLA), Michael I. Jordan (UC Berkeley), Victor Bahl (Microsoft), Vijaykrishnan Narayanan (Penn State University)

If you have any question or need any additional information, please contact us at mailto:aiotworkshop@gmail.com.

Thanks,

Jian Zhang and Jian Tang
AIoT Workshop Program Co-chairs

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Call for Submission: SIGDA Student Research Forum at ASP-DAC 2020

The Student Research Forum at the ASP-DAC is renovated from a traditional poster session hosted by ACM SIGDA for Ph.D. students to present and discuss their dissertations with experts in system design and design automation community. Starting from 2015, the forum includes both Ph.D. and M.S. students, offering great opportunity for the students to establish contacts for their future career. In addition, the forum helps the companies and academic institutes to get an overview of the latest research and discover the extraordinary candidates for their employment. The forum is open to all students of the relevant research community and is free-of-charge. Limited funds are available for travel assistance based on financial needs. It is co-
located with ASP-DAC but ASP-DAC registration is not required in order to attend this event.

ELIGIBILITY

Students must be within 1 year (M.S.) or 2 years (Ph.D.) of dissertation completion or have completed their dissertation during the last 12 months.

Dissertation topic must be relevant to the ASP-DAC community.

Previous ASP-DAC forum presenters are not eligible.

Students who have presented previously at the DAC and DATE Ph.D. forums are eligible, but will be less likely to receive travel assistance.

Only students with at least one published or accepted conference, symposium or journal "full"

paper are eligible for awards and travel assistance.

SUBMISSION REQUIREMENTS

A two-page PDF abstract of the dissertation (in two-column format, using 10pt. fonts and single-spaced lines), including name, institution, adviser, contact information, estimated (or actual) graduation date, whether the work has been presented at DAC Ph.D. Forum or DATE PhD Forum, as well as figures, and bibliography (if applicable). The two-page limit on the abstract will be strictly enforced: any material beyond the second page will be truncated before sending to the reviewers. Each accepted abstract has to prepare a poster and the student has to physically attend the forum.

To be considered for awards and travel assistance, a student must explicitly indicate, in the title of the two-page abstract, the venues for which the work was published or accepted, and a list of all papers authored or co-authored by the student should be included in the bibliography of the two-page abstract. The papers must be related to the dissertation topic, and those on topics unrelated to the dissertation abstract will not be considered in the review process. An additional appendix (as the third page) briefly specifies your travel budget and financial aid request, as well as the endorsement from your advisor or department about the fund matching for your travel to SRF.

Submit this material to the ASP-DAC online submission system at:

https://easychair.org/conferences/?conf=aspdacsrf2020

IMPORTANT DATES

Submission Deadline: November 06, 2019

Notification Date: November 20, 2019

Poster Session: January 14, 2020

CONTACT INFORMATION

For questions about Student Research Forum @ ASP-DAC 2020, please send e-mail to Prof. Hyung Gyu Lee (hglee@daegu.ac.kr). Please include "ASP-DAC SRF" in the subject line of your email.

COMMITTEE MEMBERS

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Co-Chair:

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Luan Huu Kinh Duong, Nanyang Technological University, Singapore

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