SIGDA Special Interest Group Design Automation
The resource for EDA Professionals

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Comments from the Editors

Dear ACM/SIGDA member,

We are excited to present to you the October e-newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from upcoming conference and funding deadlines, hot research topics to news from our community. Get involved and contact us if you want to contribute an article or announcement.

The newsletter is evolving, let us know what you think.

Happy reading!

Aida Todri-Sanial
Yu Wang
Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit http://www.acm.org/renew or call between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or 1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org

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SIGDA News

(1) "China Poised to Lead in Chip Equipment Spending"
[https://www.eetimes.com/document.asp?doc_id=1335130]

The market for chipmaking equipment is likely to recover next year, energized by China increasing its spending on production gear for memory ICs and other new projects. If China buys as much equipment as anticipated, it will become the world's largest buyer of fab tools for the first time ever, according to industry organization SEMI.

(2) "Semiconductor Industry to Rebound in 2020 with 4% Growth"
[https://www.eetimes.com/document.asp?doc_id=1335122]

Speaking at his mid-term semiconductor industry forecast seminar in London this week, Malcolm Penn, chairman and CEO of industry analyst Future Horizons, assured attendees that industry fundamentals were sound, and after a fall of around 15% in 2019, the industry will rebound with around 4% revenue growth to $414 billion in 2020.

(3) "Alibaba Unveils Powerful AI Inference Chip"
[https://www.eetimes.com/document.asp?doc_id=1335150]

At Alibaba's Apsara cloud computing conference in Hangzhou, China today, the company's CTO Jeff Zhang unveiled an AI inference accelerator chip for the cloud which he claimed offers ten times the computing power of today's GPUs.

(4) "Wireless, Battery-Free Sensor for Brain Aneurysm Treatment"
[https://www.eetimes.com/document.asp?doc_id=1335152]

Researchers have created a new medical sensor that promises to revolutionize the ability of doctors to treat brain aneurysms. The device, which is battery-less, is a capacitive sensor with an inductor. It can be implanted directly in patients' brains and, oddly enough, that's significantly less invasive than the most common treatment the medical profession uses today.

(5) "Samsung Steps up KV Spec with SSD Prototype"

[https://www.eetimes.com/document.asp?doc_id=1335146]

Samsung Electronics Co., Ltd., is one of the first companies out of the gate with an SSD prototype based on a new open standard for a key-value application programming interface (KV API).

(6) "Dell-EMC Combines Optane, NVMe"
[https://www.eetimes.com/document.asp?doc_id=1335139]

Much of the potential of 3D Xpoint technology is expected to come from the DIMM form factor, but Dell-EMC is bullish enough on the Intel Optane SSDs to include it in its latest PowerMax storage array, which also boasts end-to-end NVMe.

(7) "GaN is Driving Power Semiconductors"
[https://www.eetimes.com/document.asp?doc_id=1335143]

Power semiconductor devices with gallium nitride (GaN) and silicon carbide (SiC) are gradually replacing their silicon-based counterparts, largely because using GaN or SiC power transistors can lead to more straightforward and efficient energy storage solutions. The combined GaN and SiC market is projected to be valued at over US$3 billion by 2025 and will be substantially driven by renewables and electric vehicles. We live in a world where more and more data centers, electric vehicles, industrial engines are spreading. Everyone needs to improve their energy use.

(8) "MEMS Microphone Market Grows; Vesper Too"
[https://www.eetimes.com/document.asp?doc_id=1335128]

Microphones are virtually everywhere, and they are proliferating at an astonishing rate. It’s an inexorable trend attributed to the surging demand for smartphones, IoT devices, wearables, hearing aids, virtual reality headsets, and other consumer electronics. Those mics are always listening, always ready to switch on, so even while idle most of the time, in aggregate they consume kilowatt-hours of energy. That’s an opportunity Vesper Technologies Inc., a Boston-based provider of piezoelectric MEMS microphones, has seized.

(9) "Synopsys ARC Embedded Vision Processors Deliver 35 TOPS"
[https://www.eetimes.com/document.asp?doc_id=1335112]

Synopsys has launched its latest generation of embedded vision processors with deep neural network (DNN) accelerator delivering what it claims is an industry-leading 35 TOPS (tera operations per second) performance for artificial intelligence (AI) intensive edge applications. Also introduced is a functional safety processor version for automotive advanced driver assist systems (ADAS), radar/lidar, and automotive sensor system on chip (SoC) development.

(10) "Understand Speech on a Sub-$1 MCU"
[https://www.eetimes.com/document.asp?doc_id=1335118]

New technology from a Canadian startup means AI models for natural language processing can run efficiently on small CPUs and even microcontrollers. Voice control functionality, typically done via internet connection to the cloud today, can now be added to all manner of appliances.

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"What is" Column

What is a time-critical cyber-physical system?
by Wanli Chang
Assistant Professor
Real-Time Systems Research Group
Department of Computer Science, Faculty of Sciences
University of York, UK

Cyber-physical systems (CPS) have wide applications in robotics, autonomous driving, avionics, 5G networks, and medical devices. Timing is a critical issue in many of the CPS and often needs to be respected as a hard constraint. Take autonomous vehicles as an example. While hundreds of teams around the world are able to develop sufficient functionalities to make the prototypes look autonomous, two major challenges have not been addressed, obstructing mass production and deployment: (i) how to provide timing guarantees; (ii) how to realise the functions on limited resources. Another example is wireless base stations of 5G networks. Analysis shows that there is very little real-time concept in the current wireless base stations. The design philosophy is based on ‘best effort’. The average-case performance is good, mainly coming from strong hardware support, yet there is hardly any timing guarantee. Looking into the future, on one hand, many applications in the 5G era have stringent temporal requirements, and on the other hand, as Moore’s Law is most likely coming to an end, it will be difficult to exploit hardware for more resources.

In general, due to the significantly more complex functionalities and foreseeable slowing down of hardware evolvement, the simple safety margins (that can be up to one order of magnitude) in the existing design paradigm are disappearing. In order to achieve timing predictability in modern CPS, a cross-layer design methodology is required, covering from application software that interacts with physical dynamics, through programming languages and operating systems, to hardware platforms. This creates both challenges and opportunities. There have been some pioneer works along this direction, driven by collaboration between academia and industry. A memory-aware schedule is proposed in [1] to increase cache reuse and reduce the worst-case execution time (WCET) of certain instances. A novel controller design exploits non-uniform sampling to achieve better control performance. There is also guarantee on settling time, which defines how long it takes to complete an action, such as braking or steering. A software development framework that automatically converts standard time-sharing Java applications to real-time Java applications, with the support of model-driven techniques, is reported in [2]. Features of the operating systems, such as OSEK/VDX from the automotive domain, are considered in [3], to improve the application performance and reduce the processor utilisation. These works are just a very beginning in this line of research and there are lots of complex problems to be formulated and solved.

Besides the new design methodology covering various layers of CPS, there is an urgent demand to create real-time theories for multiprocessors that will inevitably be used in CPS. The existing real-time theories have been mostly developed for a single processor, and their optimality, or even applicability, can be undermined if multiprocessors are used. Design automation will become particularly important considering the significantly increased complexity. Take the widely applied fixed-priority preemptive scheduling (FPPS) as an example. Task priorities are assigned beforehand and there have been several well-established optimal priority assignment algorithms, e.g., the deadline monotonic priority ordering (DMPO), the Audsley's optimal priority assignment (OPA) [4], and the robust priority assignment (RPA) [5], all of which were developed considering a single processor. With exact schedulability tests for resource sharing in multiprocessors (such as those for MrsP in [6]), where the response time of a task depends potentially on all other tasks in the system, the optimality of DMPO no longer holds while OPA and RPA cannot be applied. Therefore, a thorough analysis of these algorithms on multiprocessors is required and new priority assignment methods need to be developed.

[1] Wanli Chang, Dip Goswami, Samarjit Chakraborty, Lei Ju, Chun Jason Xue, Sidharta Andalam, Memory-aware embedded control systems design, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 36, Iss. 4, pp. 586-599, 2017.
[2] Wanli Chang, Shuai Zhao, Ran Wei, Andy Wellings, Alan Burns, From Java to real-time Java: A model-driven methodology with automated toolchain, ACM SIGPLAN/SIGBED International Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2019.
[3] Wanli Chang, Dip Goswami, Samarjit Chakraborty, Arne Hamann, OS-aware automotive controller design using non-uniform sampling, ACM Transactions on Cyber-Physical Systems (TCPS), Vol. 2, Iss. 4, Article 26, 2018.
[4] Neil Audsley, On priority assignment in fixed priority scheduling, Information Processing Letters, Vol. 79, Iss. 1, pp. 39-44, 2001.
[5] Rob Davis, Alan Burns, Robust priority assignment for fixed priority real-time systems, Real-Time Systems Symposium (RTSS), 2007.
[6] Shuai Zhao, A FIFO spin-based resource control framework for symmetric multiprocessing, PhD Dissertation, University of York, 2018.

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Paper Submission Deadlines

ISPD'20 – ACM Int'l Symposium on Physical Design
San Francisco, CA
Deadline: Oct 7, 2019 (Abstracts due: Sep 30, 2019)
Mar 29 - Apr 1, 2020
http://www.ispd.cc

ISCAS'20 – IEEE Int'l Symposium on Circuits and Systems
Seville, Spain
Deadline: Oct 20, 2019
May 17-20, 2020
http://iscas2020.org

HOST'20 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
San Jose, CA
Deadline: Nov 15, 2019
May 4-7, 2020
http://www.hostsymposium.org

ISCA'20 – Int'l Symposium on Computer Architecture

Valencia, Spain
Deadline: Nov 26, 2019 (Abstracts due: Nov 19, 2019)
May 30 – Jun 3, 2020
https://iscaconf.org

DAC'20 – Design Automation Conference
San Francisco, CA
Deadline: Nov 27, 2019 (Abstracts due: Nov 21, 2019)
Jul 19-23, 2020
http://www.dac.com/

TAU'20 – ACM Int'l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems
Monterey, CA
Deadline: Dec 1, 2019
Mar 19-20, 2020
http://www.tauworkshop.com

ISVLSI'19 – IEEE Computer Society Annual Symposium on VLSI
Limassol, Cyprus
Deadline: Feb 20, 2010
Jul 6-8, 2020
http://www.isvlsi.org

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Upcoming Symposia, Conferences and Workshops

BodyNets'19 – Int'l Conference on Body Area Networks
Florence, Italy
Oct 2-3, 2019
http://www.bodynets.org

VLSI-SoC'19 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Cuzco, Peru
Oct 6-9, 2019
www.vlsi-soc.com

MEMOCODE'19 – ACM/IEEE Int'l Conference on Formal Methods and Models for Codesign
San Diego, CA
Oct 9-11, 2019
https://memocode.github.io/2019

MICRO'19 – IEEE/ACM Int'l Symposium on Microarchitecture
Columbus, OH
Oct 12-16, 2019
http://www.microarch.org/micro52

ESWEEK'19 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)
New York, NY
Oct 13-18, 2019
http://www.esweek.org

NOCS'19 – IEEE/ACM Int'l Symposium on Networks-on-Chip
New York, NY
Oct 17-18, 2019
https://www.engr.colostate.edu/nocs2019

BIOCAS'19 – Biomedical Circuits and Systems Conference
Nara, Japan
Oct 17-19, 2019
http://www.biocas2018.org

ICCAD'19 – IEEE/ACM Int'l Conference on Computer-Aided Design
Westminster, CO
Nov 4-7, 2019

http://www.iccad.com

WOSET'19 – Workshop on Open Source EDA Technology (co-located with ICCAD'19)
Westminster, CO
Nov 7, 2019
http://woset.org

ICPADS'19 – IEEE Int'l Conference on Parallel and Distributed Systems
Tianjin, China
Dec 4-6, 2019
http://www.icpads2019.cn

FPT'19 - Int'l Conference on Field-Programmable Technology
Tianjin, China
Dec 9-13, 2019
http://icfpt.org

ISED'19 – Int'l Symposium on Electronic System Design
Kollam, India
Dec 13-15, 2019
http://isedconf.org

iSES'19 – IEEE Int'l Symposium on Smart Electronic Systems
Rourkela, India
Dec 16-18, 2019
http://www.ieee-ises.org

HiPC'19 – IEEE Int'l Conference on High Performance Computing
Hyderabad, India
Dec 17-20, 2019
http://www.hipc.org

VLSID'20 – Embedded and VLSI Design Conference
Bengaluru, India
Jan 4-8, 2020
http://www.vlsidesignconference.org

ASP-DAC'20 - Asia and South Pacific Design Automation Conference
Beijing, China
Jan 13-16, 2020
www.aspdac.com

HiPEAC'20: Int'l Conference on High Performance Embedded Architectures & Compilers
Balogna, Italy
Jan 20-22, 2020
https://www.hipeac.net

ISSCC'20 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Feb 16-20, 2020
http://isscc.org

FPGA'20 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Seaside, CA
Feb 24-26, 2020
http://www.isfpga.org

DATE'20 - Design Automation and Test in Europe
Grenoble, France
Mar 9-13, 2020
http://www.date-conference.com

ISQED'20 - Int'l Symposium on Quality Electronic Design
Santa Clara, CA
Mar 25-26, 2020
http://www.isqed.org

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Call for Participation: ESWEEK 2019

EMBEDDED SYSTEMS WEEK
Call for Participation

CASES * CODES+ISSS * EMSOFT * IoMT * NoCs * Workshops * Tutorials

New York City, USA, October 13 - 18, 2019
www.esweek.org

About Embedded Systems Week (ESWEEK)

Embedded Systems Week (ESWEEK) is the premier event covering all aspects of embedded systems and software. By bringing together three leading conferences (CASES, CODES+ISSS, EMSOFT), a special track on Internet of Medical Things (IoMT), a symposium (NOCS) and several workshops and tutorials, ESWEEK allows attendees to benefit from a wide range of topics covering the state of the art in embedded systems research and development.

Preliminary program: https://esweek.org/program
Registration: https://esweek.org/registration
Advanced Registration Deadline: Sep. 20

Registered attendees are entitled to attend sessions of all conferences CASES, CODES+ISSS, EMSOFT, and the IoMT Day. Symposium, workshops, and tutorials require separate registration.

Timeline
* September 9, 2019: "Child-Care Travel Support Program" extended application deadline
* Details: https://www.esweek.org/child-care-travel-support-program
* September 14, 2019: "ESWEEK Student Travel Grant" application deadline
* Details: https://www.esweek.org/esweek-student-travel-grant
* September 20, 2019: Advanced Registration Deadline
* Registration page: https://esweek.org/registration
* October 13 - 18, 2019: ESWEEK in New York City, USA

Keynotes
* Monday Keynote: "High Performance Computing in a World of Embedded Intelligence"
https://esweek.org/event-details?id=281--102-
Speaker: Steve Keckler - NVIDIA
* Tuesday Keynote: "Health Monitoring with Machine Learning and Wireless Sensors"
https://esweek.org/event-details?id=281--103-
Speaker: Dina Katabi - MIT
* Wednesday Keynote: "Cyber-Physical-Human Systems: Opportunities and Challenges"
https://esweek.org/event-details?id=281--104-
Speaker: Pramod Khargonekar - UC Irvine

Conferences and Special Track
* CASES: International Conference on Compilers, Architecture, and Synthesis for Embedded Systems
https://esweek.org/cases/about
Program Chairs: Akash Kumar, Technical University of Dresden, DE
Partha Pande, Washington State University, US
* CODES+ISSS: International Conference on Hardware/Software Codesign and System Synthesis
https://esweek.org/codes/about
Program Chairs: Sudeep Pasricha, Colorado State University, US
Roman Lysecky, University of Arizona, US
* EMSOFT: International Conference on Embedded Software
https://esweek.org/emsoft/about
Program Chairs: Sriram Sankaranarayanan, Univ. of Colorado Boulder, US

Timothy Bourke, Inria Paris, FR
* IoMT Day: Internet of Medical Things (IoMT)
https://esweek.org/iomt/about
IoMT Chair: Insup Lee, University of Pennsylvania, US
Paul Bogdan, University of Southern California, US

Symposium
* NOCS: International Symposium on Networks-on-Chip
https://esweek.org/nocs-about

Tutorials: https://esweek.org/events/2019-10-13
* Machine Learning for Design and Optimization of Embedded Systems
* Machine Learning Security
* Industry Tutorial: The Open Source ACRN Hypervisor on an Intel Embedded Platform
* Open-Source Hardware: Heterogeneous System Integration with Embedded Scalable Platforms
* HW/SW Modeling and Performance Analysis of Heterogeneous Safety-Critical Systems
* Industry Tutorial: PYNQ: Python Productivity for Zynq
* Hardware Design in the 21st Century with the Object Oriented and Functional Language Chisel

Workshops: https://esweek.org/workshops
* Accelerating AI for Embedded Autonomy (AAIEA)
* CyberCardia Workshop on Medical CPS (CyberCardia)
* Model-Based Design of Cyber Physical Systems (CyPhy)
* Embedded Operating Systems Workshop (EWiLi)
* International Workshop on Highly Efficient Neural Processing (HENP)
* INTelligent Embedded Systems Architectures and Applications (INTESA)
* International Workshop on Rapid System Prototyping (RSP)
* Workshops on Embedded Systems Education (WESE)

ESWEEK Student Travel Grant & Child-Care Travel Support Program
ESWEEK 2019 is happy to announce the ACM SIGBED, ACM SIGDA, IEEE CEDA, and NSF ESWEEK Opportunity Programs dedicated to supporting student participation at the event. The Programs offer travel support to a limited number of students. Preference will be given to students being an author or co-author of a paper accepted at one of the conferences of
ESWEEK 2019, and be in need for financial support. Details: https://esweek.org/esweek-student-travel-grant

Would you like to attend ESWEEK, but cannot because the cost of child-care is prohibitive? SIGBED provides funds for a limited number of grants that support child care for members that would like to participate in ESWEEK but are unable to do so without this support. SIGBED provides financial assistance to subsidize a variety of child-care options. Details: https://esweek.org/child-care-travel-support-program

Organization: https://esweek.org/committees/esweek/2019
Petru Eles, Linkˆping University, SE (General Chair)
Tulika Mitra, National University of Singapore, SG (Vice General Chair)
Soonhoi Ha, Seoul National University, KR (Past Chair)

ESWEEK Local Arrangement Chairs:
Ramesh Karri, New York University, US (Conference Chair)
Siddarth Garg, New York University, US

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Call for Participation: NOCS 2019

13th IEEE/ACM International Symposium on Networks-on-Chip
Oct 17-18, 2019; co-located with ESWEEK 2019, New York, NY, USA
https://www.engr.colostate.edu/nocs2019/

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to interdisciplinary research on on-chip, package-scale, chip-to-chip, and datacenter rack-scale communication technology, architecture, design methods, applications and systems. NOCS brings together scientists and engineers working on NoC innovations and applications from inter-related research communities, including discrete optimization and algorithms, computer

architecture, networking, circuits and systems, packaging, embedded systems, and design automation.

Registration for NOCS 2019 is open at: https://esweek.org/registration

The conference program includes several keynotes, tutorials, special sessions and regular paper session with participants from industry and academia. We hope you are able to attend!

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Call for Participation: MLCAD

1st ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)

The workshop focuses on Machine Learning (ML) methods for all aspects of CAD and electronic system design. The predecessor of this workshop was held at the Design, Automation and Test in Europe (DATE) Conference in March 2019. The workshop is sponsored by both IEEE Council on Electronic Design Automation (CEDA) and ACM Special Interest Group on Design Automation (SIGDA). Around one third of the workshop program will consist of invited and keynote speakers from major CAD and Industrial Companies, who will present their vision on machine learning for CAD.

Workshop: September 3-4, 2019
Register and attend: http://mlcad.itec.kit.edu

General Chairs
Marilyn Wolf, Georgia Institute of Technology
Jörg Henkel, Karlsruhe Institute of Technology

Industry Chairs
Ulf Schlichtmann, TU Munich
Paul Franzon, North Carolina State U.

Program Chairs
Hussam Amrouch, Karlsruhe Institute of Technology
Bei Yu, Chinese University of Hong Kong

Finance Chair
Hai Li, Duke University

Contact: henkel@kit.edu
http://mlcad.itec.kit.edu

SPONSORS: ACM SIGDA, IEEE CEDA

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Call for Papers: WOSET 2019

Second Workshop on Open-Source EDA Technology (http://woset.org).
Co-located with ICCAD 2019, Nov 7,The Westin Westminster, Westminster CO.

This one-day workshop aims to galvanize the open-source EDA movement. The workshop will bring together EDA researchers who are committed to open-source principles to share their experiences and coordinate efforts towards developing a reliable, fully open- source EDA flow. The workshop will feature presentations that overview existing open-source tools, along with sessions and posters describing future planned EDA tools. The workshop will include a panel to brainstorm the current status and future challenges for open-source EDA, and to coordinate efforts and ensure quality and interoperability across open-source tools.

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Call for Papers: ACM TECS Special Issue on LCTES 2019

ACM Transactions on Embedded Computing Systems
Special issue on Languages Compilers Tools and Theory of Embedded Systems

The special issue in the ACM Transactions on Embedded Computing Systems will consider peer-reviewed journal versions of top papers from LCTES 2019, as well as other papers received from the open call. This special issue solicits papers presenting original work on programming languages, compilers, tools, theory, and architectures that help in overcoming these challenges. Research papers on innovative techniques are welcome, as well as experience papers on insights obtained by experimenting with real-world systems and applications. We solicit original papers on the following topics of interest related to LCTES:
Programming languages
Compilers
Tools for analysis, specification, design, and implementation
Theory and foundations of embedded systems
Novel embedded architectures
Mobile systems and IoT
Industrial case studies

IMPORTANT DATES
Open for submissions in ScholarOne Manuscripts: August 15, 2019
Closed for submissions: October 15, 2019
Results of first round of reviews: January 01, 2020
Submission of revised manuscripts: March 01, 2020
Results of second round of reviews: May 01, 2020
Publication materials due: August 15, 2020

SUBMISSION GUIDELINES: Prospective authors are invited to submit their manuscripts electronically after the "open for submissions" date, adhering to the ACM Transactions on Embedded Computing Systems guidelines (tecs.acm.org/authors.cfm). Please submit your papers through the online system (mc.manuscriptcentral.com/tecs) and be sure to select the "SI:LCTES2019" option for the paper-type. Also, please indicate that you are submitting to the Special issue on LCTES 2019 in author's cover letter. Manuscripts should not be published or currently submitted for publication elsewhere. Extended versions of conference papers (including LCTES 2019) are acceptable with at least 30% new content. Any questions on this special issue should be addressed to Aviral Shrivastava (Aviral.Shrivastava@asu.edu).

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Call for Papers: IEEE Design and Test - Special issue on Open-Source EDA

Aim and Scope:
In the 80s the academic community produced several very high-quality EDA tools that spawned the EDA industry. Tools like Spice, Espresso, and SIS became the foundation of EDA companies. Open-source tools enable rapid innovation and create an ecosystem for scientific development. In recent years, the cost and difficulty of IC design in advanced nodes have stifled hardware design innovation and have raised unprecedented barriers to bringing new design ideas to the marketplace. Unlike the thriving software community, which enjoys a large number of open-source operating systems, compilers, libraries and applications, the hardware community lacks such a modern ecosystem. With the advent of Open Silicon IP Ecosystems like RISCV, Chips Alliance, and Free Silicon Foundation, the time has come to reinvigorate the open-source movement in EDA tools. The EDA open-source landscape is fragmented and a full open-source EDA flow is lacking. Recent programs from governmental agencies aim to jump-start development of open-source EDA tools to reduce the cost and turnaround time of hardware design. Open-source development also leads to special challenges such as physical design kit support and tool maintenance and support.
Topics of Interest:

Specific topics of interest include but are not limited to the following:
SoC architecture and design tools
Simulation tools
Automatic accelerator and high-level synthesis
Tools for security and system verification
Logic synthesis
P & R tools (Floorplanning, Placement, Physical synthesis, Clock tree synthesis, Global and detailed Routing and Layout finishing)
Analysis tools: parasitics, timing, power, IR drop and thermal
Pervasive machine learning for EDA flows
Automated analog design
Design for emerging technologies

Submission Guidelines:
Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at https://mc.manuscriptcentral.com/dandt

A specific special issue category will be available and selectable from a menu. All articles will undergo the standard IEEE Design & Test review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere.

Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Resources for links to Submission Guidelines Basics and Electronic Submission Guidelines and requirements.

Accepted articles must meet the following three criteria:
Technical novelty: all articles must meet the standard criteria of technical contribution, in terms of novel methodologies and algorithms with demonstrated superiority over existing methods.
Open-source and interoperability: all submissions must include a link to their open-source code. All open-source tools must use standard input and output file formats or databases to ensure interoperability in EDA flow.
High impact on EDA flows: acceptance priority will be given to articles that address missing or critical needs within the existing open-source ecosystem.

Submissions that heavily overlap with prior conference publications by the same authors will be given low acceptance priority.

Schedule:
Initial Submission Deadline: 15 January 2020
Notification First Round: 1 March 2020
Revision Submission: 1 April 2020
Final Notification: 1 May 2020
Final Version Due: 15 May 2020

Guest Editors:
Sherief Reda, Brown University, sherief_reda@brown.edu
Leon Stok, IBM, leonstok@us.ibm.com
Pierre-Emmanuel Gaillardon, University of Utah, pierre-emmanuel.gaillardon@utah.edu

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Call for Participation: SEC 2019

Dear Colleagues,

Join us on November 7 - 9, 2019 at the Hilton Crystal City at Washington Reagan National Airport in Arlington, VA to learn about the latest research related to edge computing.
The preliminary program is now available, featuring an outstanding combination of 2 keynotes, 1 panel, 20 peer-reviewd papers, 24 posters/demos, 3 workshops (ArchEdge, EdgeSP, HotWot), a PhD Student forum, a Women-in-Computing forum,
social networking & recruiting events, all packed into 3 intense days. The coverage and discussions on edge computing, vehicular edge system, and deep learning in edge systems will energize
you with new ideas and business possibilities.

Early Registration Deadline is Oct 10, 2019!

Check out the Keynotes and Panels at http://acm-ieee-sec.org/2019/keynote%20and%20panel.php

Student travel grants from US NSF and IEEE Technical Committee on the Internet (TCI) are available at http://acm-ieee-sec.org/2019/index.php

We look forward to meeting you at SEC 2019!

General Co-Chairs
Songqing Chen, George Mason University
Ryokichi Onishi, Toyota

Program Co-Chairs
Ganesh Ananthanarayanan, Microsoft Research

Qun Li, College of William & Mary
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Notice to Authors

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
Circulation: 2,700