sig da Special Interest Group Design Automation
The resource for EDA Professionals

1 August 2019, Vol. 49, No. 8
Online archive: http://www.sigda.org/newsletter

Comments from the Editors

Dear ACM/SIGDA member,

We are excited to present to you the August e-newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from upcoming conference and funding deadlines, hot research topics to news from our community. Get involved and contact us if you want to contribute an article or announcement.

The newsletter is evolving, let us know what you think.

Happy reading!

Aida Todri-Sanial
Yu Wang
Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit http://www.acm.org/renew or call between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or 1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org

"SIGDA E-News Editorial Board:"

'"Aida Todri-Sanial"', E-Newsletter co Editor-in-Chief

'"Yu Wang"', E-Newsletter co Editor-in-Chief

'"Xiang Chen"', E-Newsletter Associate Editor for SIGDA News column

'"Yanzhi Wang"', E-Newsletter Associate Editor for SIGDA Local chapter news column

'"Pingqiang Zhou"', E-Newsletter Associate Editor for SIGDA Awards column

'"Yuan-Hao Chang"', E-Newsletter Associate Editor for SIGDA What is column

'"Wenchao Li"', E-Newsletter Associate Editor for SIGDA What is column

'"Debjit Sinha"', E-Newsletter Associate Editor for for SIGDA Paper submission deadline column

'"Pingqiang Zhou"', E-Newsletter Associate Editor for SIGDA Awards column

'"Jayita Das"', E-Newsletter Associate Editor for SIGDA Funding opportunities column

'"Qinru Qiu"', E-Newsletter Associate Editor for SIGDA Live column

'"Yiyu Shi"', E-Newsletter Associate Editor for SIGDA Live column

'"Rajsaktish Sankaranarayanan"', E-Newsletter Associate Editor for SIGDA Researcher spotlight column

Back to Contents

Note from the Editors

(1) "Apple to Buy Intel's Modem Business for $1 Billion'"
[https://www.eetimes.com/document.asp?doc_id=1334964]

Apple will pay about $1 billion to acquire Intel's smartphone modem business, signaling that, despite a settlement reached with longtime supplier Qualcomm in April, Apple still has designs on its own silicon for 5G.

(2) "Alibaba Reveals 16-core RISC-V Chip"
[https://www.eetimes.com/document.asp?doc_id=1334966]

Alibaba Group's chip subsidiary, Pingtouge Semiconductor, this week announced what it claims is the most powerful

RISC-V based processor, the Xuantie 910, targeting infrastructure for artificial intelligence (AI), 5G, and internet of things (IoT) as well as autonomous vehicles.

(3) "SoftBank Launches $108B Vision Fund 2 Targeting AI"
[https://www.eetimes.com/document.asp?doc_id=1334968]

Softbank has today launched its Vision Fund 2 to facilitate investment in late-stage artificial intelligence (AI) companies. The fund, for which $108 billion has been committed so far, will include participation from Apple, Foxconn, Microsoft, various banks from Japan and Kazakhstan, plus major participants from Taiwan.

(4) "As Trade Talks Resume, China Advances 5G"
[https://www.eetimes.com/document.asp?doc_id=1334879]

For the global semiconductor industry, the just-revealed truce in the “trade war” between U.S. President Donald Trump and China’s president, Xi Jinping is welcome news but hardly the end of a poorly scripted economic melodrama that continues to pose dire consequences for the American semiconductor market.

(5) "What the Japan-Korea Trade War Means to the World"
[https://www.eetimes.com/author.asp?section_id=36&doc_id=1334926]

By restricting exports of key chemical materials to South Korea, Japan has already done irreparable harm to the global electronics industry, at a price both incalculable and unnecessary.

(6) "TSMC Sees 5G Driving Strong Demand for 7nm"
[https://www.eetimes.com/document.asp?doc_id=1334951]

Taiwan Semiconductor Manufacturing Co. (TSMC) sees 5-nm and 7-nm demand improving from its earlier expectations, as the worldwide 5G development accelerates.

(7) "For Mass-Market Cars, Forget L3-L5 Autonomy"
[https://www.eetimes.com/author.asp?section_id=36&doc_id=1334845]

Let's apply the SAE automation levels to the mass-market cars. Nobody should be surprised how the future of autonomous vehicles looks a lot different in Detroit, Stuttgart and Tokyo.

(8) "Startup Puts AI Core in SSDs"
[https://www.eetimes.com/document.asp?doc_id=1334982]

Startup InnoGrit debuted a set of three controllers for solid-state drives (SSDs), including one for data centers that embeds a neural-network accelerator. They enter a crowded market with claims of power and performance advantages over rivals.

(9) "Battery Research Advances Quantum Computing Capabilities"
[https://www.eetimes.com/document.asp?doc_id=1334967]

Research in battery chemistry is getting a boost from quantum computing that in turn is furthering research to improve quantum computing.

(10) "STEM: It’s Time to Add an ‘A’"
[https://www.eetimes.com/document.asp?doc_id=1334730]

Yes, the world needs more people versed in STEM, but the growing imperative for STEM workers is hardening into dogma that isn’t good for anybody, including companies in the technology industry. As STEM skills are becoming increasingly exalted, non-technical skills are being not only minimized but denigrated. The problem is encapsulated in the tension between the two jokes above.

Back to Contents

SIGDA News

We are pleased to announce that Design Automation Conference (DAC) has been promoted to Rank-A conference by China Computer Federation (CCF). The CCF webpage is https://www.ccf.org.cn/. Now DAC is CCF-A conference now!

Thanks for the faculty members and researchers that have contributed to this.

Back to Contents

SIGDA Local Chapter News

Awards at ACM/SIGDA Sponsored Events

DAC 2019: The 56th Design Automation Conference, https://dac.com

1. Best Paper Award

"DREAMPLACE: Deep Learning Toolkit-enabled GPU Acceleration for Modern VLSI Placement" by Yibo Lin (Univ. of Texas at Austin), Shounak Dhar (Univ. of Texas at Austin), Wuxi Li (Univ. of Texas at Austin), Haoxing Ren (NVIDIA Corp., Austin), Brucek Khailany (NVIDIA Corp., Austin) and David Z. Pan (Univ. of Texas at Austin).

2. 2018 Phil Kaufman Award for Distinguished Contributions to Electronic Systems Design

Thomas W. Williams, Synopsys (retired, fellow): "For overall impact on electronic industry through contributions to scan design for testability, related test automation".

3. ACM IEEE A. Richard Newton Technical Impact Award in Electronic Design Automation

Edward B. Eichelberger (IBM retired fellow, IEEE fellow) and Thomas W. Williams (Synopsys retired fellow): for the paper "A Logic Design Structure for LSI Testability," in Proc. of the 14th Design Automation Conference, 1977.

4. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems Donald O. Pederson Best Paper Award

“Caffeine: Towards Uniformed Representation and Acceleration for Deep Convolutional Neural Networks,” by Chen Zhang (Microsoft Research Asia), Guangyu Sun (Peking University), Zhenman Fang (Simon Fraser Univ.), Peipei Zhou (University of California at Los Angeles), Peichen Pan (Falcon Computing), and Jason Cong (University of California at Los Angeles).

5. 2019 ACM TODAES Best Paper Award

"Security in Automotive Networks: Lightweight Authentication and Authorization," by Philipp Mundhenk (TUM CREATE Limited, Singapore), Andrew Paverd (Aalto University, Finland), Artur Mrowca (TUM CREATE Limited, Singapore), Sebastian Steinhorst (TUM CREATE Limited, Singapore), MArtin Lukasiewycz (TUM CREATE Limited, Singapore), Suhaib A. Fahmy(University of Warwick, United Kingdom) and Samarjit Chakraborty (Technische Universita¨t Mu¨nchen, Germany).

6. ACM SIGDA Outstanding Ph.D. Dissertation Award

"Distributed Timing Analysis," by Tsung-Wei Huang, Advisor: Martin D. F. Wong (Univ. of Illinois at Urbana-Champaign).

Back to Contents

SIGDA Award

What is Formal Security Micro-Contract in Computer Systems Design

Michel A. Kinsy
Assistant Professor
Adaptive and Secure Computing Systems (ASCS) Laboratory
Boston University

With the emergence of new applications like computation outsourcing and the ongoing discovery of new hardware-level security vulnerabilities, there is a renewed effort in designing more secure computer architectures. However, the prevailing secure processor design methodology thus far has been the “secure enclave” approach. The National Institute of Standards and Technology defines an enclave as “a set of system resources that operate in the same security domain

and that share the protection of a single, common, continuous security perimeter." Although, there are many "secure enclave" definitions, implementations, and security guarantees, their core design principle is a mechanism to provide initial state attestation and to ensure the integrity and privacy of the execution from an adversarial entity.

Secure enclaves present two key challenges. On one hand, they can lead to a blanketed system partitioning where the enclaves act more like co-processors with substantial redundancies and overheads. On the other hand, attempts to closely integrate the enclave into the rest of the computing system or to enable tightly coupled resources sharing, often result in the creation of security gaps. This is tension between performance/efficiency and process isolation is the root cause. In other words, in multicore architectures, runtime interactions can be exceedingly complex, and therefore it may be impossible for a designer to anticipate all of them. This can result in untrusted applications circumventing the chips' built-in security measures and accessing resources of the system that should, in theory, be off-limits to such applications.

One potential solution may be the use of "formal micro-contracts". The "security micro-contract" or simply "micro-contract" paradigm is a secure computer systems design approach through minimal contracts — micro-contracts — between adjacent layers or modules of the architecture. These contracts have strict structures that contain security-relevant details of each connected layer and the secure properties that have to be preserved to assure confidentiality, integrity and availability of the data of interest [1]. Where secure enclaves take a wholesale approach to processor security, micro-contracts provide a retail approach.

Instead of specifying a whole program or computational task that must execute in a secure enclave to implicitly guarantee some security property or condition, micro-contracts allow for the explicit specification and verification of the security condition that should be maintained.

There are two aspects to guaranteeing that the constraints from a micro-contract are preserved: validation and enforcement. With validation, the computing system, data flow, minimal security invariants, and resource usage scenario are formally modeled and validated. Enforcement mechanisms are implemented on each involved layer and must preserve their own integrity. These enforcement mechanisms can be static/design-time (e.g., Verilog level, compiler passes) or runtime (e.g., execution policy enforcement units in hardware, secure OS runtime systems). The role of the enforcement aspect is to ensure that all the layers faithfully reflect the micro-contracts implementation and runtime guarantees. Validation and enforcement are both necessary. Alone, one is not a sufficient condition for establishing a system security guarantee. Micro-contracts can be used as (i) basic formalism for proving security properties of computing systems both in the software and hardware layers and across them or (ii) a template for specifying the usage model of a piece of data or resources, and (iii) run time security policy checks.

[1] Michel A. Kinsy and Novak Boskov: "Secure Computing Systems Design Through Formal Micro-Contracts". In the 29th edition of the ACM Great Lakes Symposium on VLSI (GLSVLSI), May 2019.

Back to Contents

"What is" Column

Hello readers,

In this edition of Researcher Spotlight column, we meet Prof. Hai (Helen) Li. She is the Clare Boothe Luce Associate Professor of Electrical and Computer Engineering at Duke University where she is leading the effort on Brain-inspired Computing and Emerging Memory Technologies. She received the B.S and M.S. degrees in Electrical Engineering from Tsinghua University and PhD in Electrical and Computer Engineering from Purdue University.

1. Can you share with us some of the research areas you are interested in?

I have been always interested in the advanced circuit and architecture designs for high performance and high energy efficiency. My research in this area started with conventional memory and processor designs, back to when I was a PhD student at Purdue University. After graduation, I extended my study to emerging technologies (e.g., spintronic memory, resistive memory, etc.), novel architecture such as brain-inspired computing (a.k.a., neuromorphic computing) systems. Currently, my research mainly focuses on two areas. First, I am enthusiastic about developing the neuromorphic computing systems that mimics Human Brain's structure and behaviour. Advanced nanotechnology like memristor (a.k.a., resistive memory or ReRAM) is leveraged in our design for its high density data storage and in-situ information processing. In addition, I am working on the deployment of machine learning and deep neural network algorithms on traditional hardware platforms, with the focus on acceleration and security.

2. Currently there is notable research and industry interest in brain-inspired computing. To readers unfamiliar with this, could you kindly share a few key principles or suggest pointers to a good start?

The human neocortex system naturally possesses a massively parallel architecture with closely coupled memory and computing as well as unique analog domain operations. The simple unified building blocks (i.e., neurons) follow integrate-and-fire mechanisms, leading to an ultra-high computing performance beyond 100 TFLOPs (Trillion FLoating-point Operations Per Second) and a power consumption of mere 20 Watt. By imitating such structure, neuromorphic computing systems are anticipated to be superior to conventional computer systems across various application areas. Many critical problems across multiple domains may interest our readers, e.g., the understanding and modelling of Human Brain mechanism, the mathematical representations/abstracts that provide different data processing capabilities, various hardware approaches at circuit and architectural levels, the use of emerging devices and their new features, etc.

3. Traditional computing (say, microprocessor computing) has evolved from its earliest days aided by a variety of applications. Recent research in brain inspired computing has gained momentum to some extent by the abundance of data availability and pattern recognition problems. What are the challenges in widening the reach of brain-inspired computing?

From hardware development perspective, the efficiency and adaptivity of neuromorphic systems remain as a major challenge. To accommodate the abundance of data availability, the energy-efficient implementation for online, real-time learning and inference is necessary. The evolving of hardware design, however, is far behind the rapid growth of data generation. Moreover, it'd be expected that a system can be to adapted to various applications in the same domain or even extended to multiple domains. How to enable such a capability is still under investigation. Another major challenge is the lack of support in design automation of neuromorphic systems, including functionality verification, robustness evaluation and chip testing and debugging. The data processing in neuromorphic systems usually is represented as probability functions. Traditional design automation method based on deterministic operations cannot satisfy the development of neuromorphic systems in large scale and with high quality.

4. Research in brain-inspired computing leverages resistive device technology like ReRAM and memristor owing to these devices offering some functionality similar to biological neurons and ease of scaling the level of parallelism. However, mainstream silicon technology is largely driven by CMOS today. This can potentially lead to divergent paths. In your view, what needs to happen to bridge the possible gap?

Synaptic weighting and neuron activations, as the most resource-consuming part in neuromorphic algorithms, are normally processed by hardware accelerators. A number of large-scale neuromorphic projects have emerged, taking the approach to unprecedented scales and capabilities. Examples include IBM's TrueNorth chip, the SpiNNaker machine, the BrainScaleS neuromorphic system, Intel's Loihi, etc. The discovery of memristor technology triggered a new revolution branch in neuromorphic computing system design: synaptic behavior is easily mimicked by the historical recording property of the memristor while the crossbar array structure offers the highest integration density in 2/3-D design. As can be seen that these neuromorphic systems, no matter driven by CMOS or emerging device technologies, share the same goal of realizing computing systems in large scale and high efficiency while diverse in detailed design techniques. I anticipant that the future computing systems will integrate these technologies and take their advantages.

5. Energy-cost of switching a transistor is now within comparable magnitudes to that of a biological neuron. What are the challenges in adopting such a technology to go closer to implementing more brain-like functionality?

The hardware complexity and cost have been and will continue to be the main challenge. Compared to a transistor, a biological neuron presents a much more complex functionality. It collects and processes the information from other neurons/synapses. A traditional CMOS design requires 20+ transistor to roughly approximates the similar functionality. Moreover, a biological neuron can reach out more than 10,000 neurons. The structure and strengths of these connections change over time. A technology for implementing more brain-like functionality shall have a simple structure, support high-density storage and a large volume of connectivity, and provide a certain degree of time dependent plasticity.

6. Academia often takes a pristine view of research unencumbered by business priorities. In that spirit, where should the line be drawn on the topic of say, How much of biological/neural inspiration to derive' towards technology?

How much of biological/neural inspiration to derive' has been related to how much we know about the biological systems and how well the software and hardware can support the operation. For instance, the high-level abstract of neural network demonstrated its significance in inference applications. Training, however, remains problematic, especially when model and dataset increase rapidly. It has been seen that the temporal operation can dramatically reduce the network scale and enable the self and continuous learning. However, the implementation cost of the temporal operation is high and how to integrate the temporal operations into applications of interests need further exploration. How much of biological/neural inspiration to derive' is also application-specific. Brain-inspired computing advances in cognitive applications. However, it might not be able to compete with quantum computer in scientific computation.

Rajsaktish Sankaranarayanan

Associate Editor
Back to Contents

Researcher Spotlight

ISED'19 – Int'l Symposium on Electronic System Design
Kollam, India
Deadline: Aug 18, 2019
Dec 13-15, 2019
http://isedconf.org

WOSET'19 – Workshop on Open Source EDA Technology (co-located with ICCAD'19)
Westminster, CO
Deadline: Sep 6, 2019
Nov 7, 2019
http://woset.org

DATE'20 - Design Automation and Test in Europe
Grenoble, France
Deadline: Sep 8, 2019
Mar 9-13, 2020
http://www.date-conference.com

ISSCC'20 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Deadline: Sep 9, 2019
Feb 16-20, 2020
http://isscc.org

ISQED'20 - Int'l Symposium on Quality Electronic Design
Santa Clara, CA
Deadline: Sep 14, 2019
Mar 25-26, 2020
http://www.isqed.org

FPGA'20 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Seaside, CA
Deadline: Sep 16, 2019
Feb 24-26, 2020
http://www.isfpga.org

Back to Contents

Paper Submission Deadlines

PACT'19 - Int'l Conference on Parallel Architectures and Compilation Techniques
Seattle, WA
Sep 21-25, 2019
http://www.pactconf.org

BodyNets'19 – Int'l Conference on Body Area Networks
Florence, Italy
Oct 2-3, 2019
http://www.bodynets.org

VLSI-SoC'19 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Cuzco, Peru
Oct 6-9, 2019
www.vlsi-soc.com

MEMOCODE'19 – ACM/IEEE Int'l Conference on Formal Methods and Models for Codesign
San Diego, CA
Oct 9-11, 2019
https://memocode.github.io/2019

MICRO'19 – IEEE/ACM Int'l Symposium on Microarchitecture
Columbus, OH
Oct 12-16, 2019
http://www.microarch.org/micro52

ESWEEK'19 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)
New York, NY
Oct 13-18, 2019
http://www.esweek.org

NOCS'19 – IEEE/ACM Int'l Symposium on Networks-on-Chip
New York, NY
Oct 17-18, 2019
https://www.engr.colostate.edu/nocs2019

BIOCAS'19 – Biomedical Circuits and Systems Conference
Nara, Japan
Oct 17-19, 2019
http://www.biocas2018.org

ICCAD'19 – IEEE/ACM Int'l Conference on Computer-Aided Design
Westminster, CO
Nov 4-7, 2019
http://www.iccad.com

ICPADS'19 – IEEE Int'l Conference on Parallel and Distributed Systems
Tianjin, China
Dec 4-6, 2019
http://www.icpads2019.cn

FPT'19 - Int'l Conference on Field-Programmable Technology
Tianjin, China
Dec 9-13, 2019
http://icfpt.org

iSES'19 – IEEE Int'l Symposium on Smart Electronic Systems
Rourkela, India
Dec 16-18, 2019
http://www.ieee-ises.org

HiPC'19 – IEEE Int'l Conference on High Performance Computing
Hyderabad, India
Dec 17-20, 2019
http://www.hipc.org

VLSID'20 – Embedded and VLSI Design Conference
Bengaluru, India
Jan 4-8, 2020
http://www.vlsidesignconference.org

ASP-DAC'20 - Asia and South Pacific Design Automation Conference
Beijing, China
Jan 13-16, 2020
www.aspdac.com

HiPEAC'20: Int'l Conference on High Performance Embedded Architectures & Compilers
Bologna, Italy

Jan 20-22, 2020
https://www.hipeac.net

Back to Contents

Upcoming Symposia, Conferences and Workshops

'''North America'''

Keck Foundation
Deadline: various
http://www.wmkeck.org/grant-programs/research/

USDA Foundational Program
Deadline: various
http://www.grants.gov/web/grants/view-opportunity.html?oppId=283836

NATO: Science for Peace and Security
Deadline: Proposals accepted anytime; reviews take place February 1 and May 15
http://www.nato.int/cps/en/natolive/87260.htm

Air Force Research Laboratory: Research Collaboration Program (BAA-RQKM-2013-0005)
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=212295

Federal Aviation Administration Grants for Aviation Research (FAA-12-01)
Deadline: open to December 2019
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=134953

AFRL RD/RV University Cooperative Agreement
Deadline: open to Nov 23, 2020
http://www.grants.gov/web/grants/view-opportunity.html?oppId=280237

NASA Fellowship Programs
Deadline: Various
http://science.nasa.gov/researchers/sara/fellowship-programs/

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Students-Etudiants/PG-CS/index_eng.asp

Mitacs Accelerate PhD Fellowship: Ontario Business Grants Program
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/...

Collaborative Research and Development Grants
(including DND/NSERC Research Partnership Grants)
http://www.nserc-crsng.gc.ca/Professors-Professeurs/RPP-PP/CRD-RDC_eng.asp

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Professors-Professeurs/CFS-PCP/index_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Engage-Mobiliser_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Collaborate-Collaborer_eng.asp
Research and Development Funding for Business Innovation (Multiple Organizations)
Deadline: Various
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/

'''Europe'''

Horizon 2020
Deadline: Various
http://goo.gl/geBouC

German Academic Exchange Service (DAAD)
Deadline: Various
https://www.daad.org/scholarship

German Research Foundation (DFG)
Deadline: Various
http://www.dfg.de/en

Helmholtz Association
Deadline: Various
https://www.helmholtz.de/en

Leibniz Association
Deadline: Various
http://www.leibniz-gemeinschaft.de/en/home

Leopoldina
Deadline: Various
https://www.leopoldina.org/en/about-us

Max Planck Society
Deadline: Various
https://www.mpg.de/en

Swiss National Science Foundation
Deadline: Various
http://www.snf.ch/en/

'"Asia"'

Korea:

National Research Foundation of Korea
Deadline: Various
http://www.nrf.re.kr/nrf_eng_cms/show.jsp?show_no=90&check_no=89&c_relation=0&c_...

China:

National Natural Science Foundation of China
Deadline: Various
http://www.nsfc.gov.cn/publish/portal1/

Singapore:

National Research Foundation (NRF) Singapore
http://www.nrf.gov.sg
RIE 2020 plan
Deadline: Various
http://www.nrf.gov.sg/rie2020

India:

inistry of Electronics and Information Technology
Deadline: Various
http://meity.gov.in/content/research-development

Department of Science and Technology (Nano Mission)
Deadline: Various
http://nanomission.gov.in/

University Grants Commission
Deadline: Various
http://www.ugc.ac.in/

inistry of Education Academic Research Fund
Deadline: Various
https://www.olga.moe.gov.sg/default.aspx

Agency for Science Technology and Research (A*STAR) Science and Engineering Research Council (SERC)
Deadline: Various
https://www.a-star.edu.sg/Research/Funding-Opportunities/Grants-Sponsorship.aspx

Multiple Funding
Deadline: Various
http://www.computerscienceonline.org/cs-scholarships/

'"Oceania/Polynesia"'

Polynesian Cultural Center (Hawaii) - International Student Scholarship Program
For studying in BYU Hawaii
http://www.polynesia.com/students.html

New Zealand:

inistry of Business, Innovation and Employment
Deadline: Various
http://www.mbie.govt.nz/

Australia:

Premier's Research and Industry Fund
Deadline: Various
http://www.statedevelopment.sa.gov.au/science/premiers-research-and-industry-fun...

Australian Research Council
Deadline: Various
http://www.arc.gov.au

'"South America"'

Brazil:

Coordination for the Improvement of Higher Education Personnel (CAPES)
Deadline: Various
http://www.iie.org/programs/capes#.WAu2kJMrJPM

Ministry of Science, Technology, Innovation and Communications (CNPq)
Deadline: Various
http://www.cnpq.br/

'"Africa"'

Other scholarships for African Students (list of over 30 different scholarships)
Deadline: Various
http://www.afterschoolafrica.com/12264/list-annual-engineering-scholarships-afri...

Nigeria:

Bilateral Education Agreement (BEA) Awards (both Undergraduate and Post Graduate)
Deadline: Nomination interview - March'17
http://www.fsb.gov.ng/index.php/scholarship/menu-styles/bilateral-agreement

Federal Scholarship Board
Deadline: Various
http://www.fsb.gov.ng/index.php

Back to Contents

Funding Opportunities

Frontiers in Analog CAD
International Workshop on Design Automation for Analog and Mixed-Signal Circuits
Thursday, November 7, 2019, The Westin Westminster, Westminster, CO, USA
Co-located with International Conference on Computer-Aided Design

Growing digitization of integrated circuits has contributed to making system-on-chips ever more complex. Yet, a substantial portion of a chip consists of analog and mixed-signal (AMS) circuits that provide critical functionality like clock generation, voltage regulation, interface with the external world, etc. Aggressive scaling of IC technologies as well as advancing the integration of heterogeneous physical domains on chip, substantially complicates the design of AMS components. On the one hand, their modeling and design becomes extremely complex. On the other hand, their interplay with the rest of the system-on-chip challenges design, verification and test. These new technology trends bring enormous challenges and opportunities for AMS design automation. This is reflected by an increase in research activity on AMS CAD worldwide. The purpose of this workshop is to bring together academic and industrial researchers from both design and CAD communities to report recent advances and motivate new research topics and directions in this area.

Topics of interest include (but are not limited to):
- Behavioral and performance modeling at circuit & system levels
- Simulation and formal verification
- Model checking and theorem-proving methods
- Circuit optimization, synthesis and design space exploration
- PVT variations and reliability
- Testing, diagnosis and post-silicon validation
- Physical design
- Benchmark circuits
- Hardware security involving AMS ICs
- Machine learning algorithms and methodologies for AMS CAD
- Emerging design methodologies for ultra-low power/voltage AMS ICs, neuromorphic computing, IoT, automobile, etc.

Abstracts that address any of the aforementioned topics are invited. Abstracts addressing AMS CAD issues outside of these areas will also be of great interest to the workshop. They will be considered equally relevant in review process. The workshop will NOT publish official proceedings.

Submission Instructions:
Abstracts should be submitted to Dr. Xin Li (xinli.ece@duke.edu) via email. Abstracts should be in PDF form, up to 2 pages in length with 1-inch margins and at least 10-point font size, and may contain up to two figures. Abstracts should list the full names, affiliations, and contact information of all authors, and the submission should indicate whether the abstract will be presented as a poster, orally, or both. Abstracts will be reviewed by the Program Committee. Those that are selected for oral and poster presentations will be distributed to workshop participants.

Important Dates:
Submission of Abstract: August 15, 2019
Notification of Acceptance: September 15, 2019

Co-Chairs:
Xin Li, Duke University, USA
Chandramouli Kashyap, Intel, USA

Contact:
Dr. Xin Li
Email: xinli.ece@duke.edu

Back to Contents

Call for Papers: Frontiers in Analog CAD

Nominations of SIGDA Pioneering Achievement Award

Deadline: August 31, 2019

Description: To honor a person for lifetime, outstanding contributions within the scope of electronic design automation, as evidenced by ideas pioneered in publications, industrial products, or other relevant contributions. The award is based on the impact of the contributions throughout the nominee's lifetime.

Background: The ACM Special Interest Group on Design Automation sponsors or co-sponsors the ACM Transactions on Design Automation of Electronic Systems Best Paper Award, the William McCalla Award for best paper at the International Conference on Computer-Aided Design, and the ACM/IEEE A. Richard Newton Technical Impact in Electronic Design Automation Award which is given to authors of a publication authored at least ten years earlier and that has had an outstanding contribution to the field of EDA. In addition, SIGDA sponsors the ACM Outstanding Ph.D. Dissertation Award in Electronic Design Automation which is given each year to a graduating Ph.D. student in recognition of his/her thesis contributions to advancement in the EDA field. The Pioneering Achievement Award complements these awards and is intended for contributors whose impact is typically recognized over a lifetime of outstanding achievements.

Eligibility: Open to researchers in the field of electronic design automation who have had outstanding contributions in the field during their lifetime. Current members of the Board of the ACM Special Interest Group on Design Automation, or members of the Award Selection Committee are ineligible for the award. The awardee is invited to give a lecture at a SIGDA-sponsored event.

Award Items: A plaque for the awardee, a citation, and $1000 honorarium. The honorarium will be funded by the SIGDA annual budget.

Nominee Solicitation: The call for nominees will be published by email to members of SIGDA, on the web site of ACM's Special Interest Group on Design Automation, and in the SIGDA newsletter. The nomination should be proposed by someone other than the nominee. The nomination materials should be emailed to SIGDA-Award@acm.org (Subject: ACM/SIGDA Pioneering Achievement Award). Nominations for the award should include:
A nomination letter that gives: a 100-word description of the nominee's contribution and its impact; a 750-word detailed description of up to 10 of the nominee's major products (papers, patents, software, etc.), the contributions embodied in those products, and their impact; a list of at most 10 citations to the major products discussed in the description.
Three letters of recommendation (not including the nominator or nominee).
Contact information of the nominator.
In addition to the evidence of impact, the nomination form will include biographical information (including education and employment), professional activities, publications, and recognition. Three endorsements attesting to the impact of the work may be included.

Award Committee: Selection will be made by the ACM Special Interest Group in Design Automation Executive Committee based on the recommendation of a Pioneer Award committee. The Committee will meet to review nominations, review the recommendations of the Pioneer Award Committee, and make a selection. After selection, the committee will contact the recipient to ensure that the award will be accepted and he or she will be able to deliver the talk at the SIGDA Annual Member Meeting and Dinner at ICCAD.

All standard conflict of interest regulations as stated in ACM policy will be applied (see https://awards.acm.org/conflict-of-interest). Any awards committee members will recuse themselves from consideration of any candidates where a conflict of interest may exist.

Schedule: The call for nominees will be published annually. The nomination deadline is Aug 31st. The award will be announced at one or more subsequent SIGDA events and the awardee will be invited to give a talk on his/her work at the SIGDA Annual Member Meeting and Dinner at ICCAD.

Selection/Basis for Judging: This award honors an individual who has made an outstanding technical contribution in the scope of electronic design automation throughout his or her lifetime. The award is based on the impact of the contributions as indicated above. Nominees from universities, industry, and government worldwide will be considered and encouraged. The award is not a best paper or initial original contribution award. Instead, it is intended for lifetime, outstanding contributions within the scope of electronic design automation, throughout the nominee's lifetime.

Presentation: The award will be presented annually at the SIGDA Annual Member Meeting and Dinner at ICCAD.

For more details and previous winners,

https://www.sigda.org/awards/pioneer/

Back to Contents

Call for Nominations: SIGDA Pioneering Achievement Award

1st ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)

The workshop focuses on Machine Learning (ML) methods for all aspects of CAD and electronic system design. The predecessor of this workshop was held at the Design, Automation and Test in Europe (DATE) Conference in March 2019. The workshop is sponsored by both IEEE Council on Electronic Design Automation (CEDA) and ACM Special Interest Group on Design Automation (SIGDA). Around one third of the workshop program will consist of invited and keynote speakers from major CAD and Industrial Companies, who will present their vision on machine learning for CAD.

Registration Deadline: Aug. 4th 2019
Workshop: September 3-4, 2019
Register and attend: http://mlcad.itec.kit.edu

General Chairs
arilyn Wolf, Georgia Institute of Technology
Jörg Henkel, Karlsruhe Institute of Technology

Industry Chairs
Ulf Schlichtmann, TU Munich
Paul Franzon, North Carolina State U.

Program Chairs
Hussam Amrouch, Karlsruhe Institute of Technology
Bei Yu, Chinese University of Hong Kong

Finance Chair
Hai Li, Duke University

Contact: henkel@kit.edu
http://mlcad.itec.kit.edu

SPONSORS: ACM SIGDA, IEEE CEDA

Back to Contents

Call for Participation: MLCAD

The CAD Contest at ICCAD (http://iccad-contest.org/) is a challenging, multi-month, research and development competition, focusing on advanced, real-world problems in the field of Electronic Design Automation (EDA). It is open to multi-person teams world-wide. Each year the organizing committee announce three challenging problems in different topic areas provided by industrial companies. Contestants can participate in one or more problems. The prizes will be awarded at an ICCAD special session dedicated to this contest.

Since its inaugural year of 2012, the CAD Contest at ICCAD has been attracting more than a hundred teams per year (112 teams from 12 regions in 2015, 135 teams from 11 regions in 2016, and 123 teams from 10 regions in 2017, 136 teams from 11 regions in 2018), fostering productive industry-academia collaborations, and leading to hundreds of publications in top-tier conferences and journals. The contest undoubtedly boosts EDA research and keeps enhancing its impact.

YOU ARE INVITED TO PARTICIPATE!!!

Contest Problems
Problem A: Logic Regression on High Dimensional Boolean Space (Cadence Design Systems, Inc.)
Problem B: System-level FPGA Routing with Timing Division Multiplexing Technique (Synopsys, Inc.)
Problem C: LEF/DEF Based Open-Source Global Router (Mentor Graphics & University of California San Diego)

Tentative Contest Schedule
Registration deadline: May 10, 2019
Alpha test submission: June 21, 2019
Beta test submission: July 26, 2019

Final submission: August 30, 2019
Award ceremony: November 4, 2019 (at ICCAD)
Awards for each problem
1st Place Award: NTD 50,000 / team (approx. US$ 1,650), Certificate / person, Open-source bonus for Problem C: US$ 5,500 / team
2nd Place Award: NTD 30,000 / team (approx. US$ 1,000), Certificate / person, Open-source bonus for Problem C: US$ 1,500 / team
3rd Place Award: NTD 30,000 / team (approx. US$ 1,000), Certificate / person, Open-source bonus for Problem C: US$ 500 / team
Honorable Mentions: Certificate / person

Organizing Committee
Contest chair: Ulf Schlichtmann (Technical University of Munich, Germany)
Contest co-chairs: Sabya Das (Synopsys, Inc., USA) Ing-Chao Lin (National Cheng Kung University, Taiwan) Mark Po-Hung Lin (National Chung Cheng University, Taiwan)
Topic chairs: Ching-Yi Huang, Chi-An (Rocky) Wu, Tung-Yuan Lee, and Chih-Jen (Jacky) Hsu (Cadence Design Systems Inc.) Yu-Hsuan Su, Emplus Huang, Hung-Hao Lai, and Yi-Cheng Zhao (Synopsys Inc.) Alexander Volkov, Sergei Dolgov (Mentor Graphics) Lutong Wang, Bangqi Xu (University of California San Diego)

Back to Contents

Call for Participation: CAD Contest at ICCAD 2019

SIGDA has initiated a new travel grant specifically for students from under represented groups (URP) to travel to SIGDA sponsored conferences.
- Support include registration fee and travelling (USD100, USD400 or USD800, depending on the distance)
- No need to have papers in the conference
- Support letter from supervisor
- Write a report of not less than 800 words after the conference
- Deadline: August 31, 2020 and at least one month before the event (SIGDA sponsored conferences held Oct 1, 2019 to Sept 30, 2020)
- Applicants are encouraged to join the SIGDA membership
- For more information, visit https://www.sigda.org/diversity/

Back to Contents

SIGDA Diversity Advancement Grant 2019-2020

Second Workshop on Open-Source EDA Technology (http://woset.org).
Co-located with ICCAD 2019, Th Nov 7,The Westin Westminster, Westminster CO.

This one-day workshop aims to galvanize the open-source EDA movement. The workshop will bring together EDA researchers who are committed to open-source principles to share their experiences and coordinate efforts towards developing a reliable, fully open- source EDA flow. The workshop will feature presentations that overview existing open-source tools, along with sessions and posters describing future planned EDA tools. The workshop will include a panel to brainstorm the current status and future challenges for open-source EDA, and to coordinate efforts and ensure quality and interoperability across open-source tools.

Submissions (2-4 pages):
Overview of an existing or under-development open-source EDA tool.
Overview of support infrastructure (e.g. EDA databases and design benchmarks).
Open-source cloud-based EDA tools
Position statements (e.g. critical gaps, blockers/obstacles)

Important dates:
Sept 6th 2019: submission due date.
Sept 15th 2019: notification due date.

Submission URL:
https://easychair.org/conferences/?conf=woset19

For inquires: please contact sherief_reda@brown.edu

Back to Contents

Call for Papers: WOSET 2019

By submitting your article for distribution in this Special Interest Group publication, you hereby grant to ACM the following non-exclusive, perpetual, worldwide rights: to publish in print on condition of acceptance by the editor; to digitize and post your article in the electronic version of this publication; to include the article in the ACM Digital Library and in any Digital Library related services; and to allow users to make a personal copy of the article for noncommercial, educational or research purposes. However, as a contributing author, you retain copyright to your article and ACM will refer requests for republication directly to you.

Back to Contents

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
Circulation: 2,700

This ACM/SIGDA E-NEWSLETTER is being sent to all persons on the ACM/SIGDA mailing list. To unsubscribe, send an email to listserv@listserv.acm.org with "signoff sigda-announce" (no quotes) in the body of the message. Please make sure to send your request from the same email as the one by which you are subscribed to the list.