sigda Special Interest Group
Design Automation
The resource for EDA Professionals

1 July 2019, Vol. 49, No. 7
Online archive: http://www.sigda.org/newsletter

Comments from the Editors

Dear ACM/SIGDA member,

We are excited to present to you the July e-newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from upcoming conference and funding deadlines, hot research topics to news from our community.
Get involved and contact us if you want to contribute an article or announcement.

Happy reading!

Aida Todri-Sanial
Yu Wang
Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit http://www.acm.org/renew or call between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or 1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org

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'"Rajsaktish Sankaranarayanan"', E-Newsletter Associate Editor for SIGDA Researcher spotlight column

Back to Contents

SIGDA News

(1) "DAC Keynoter: ‘Let’s Secure the Future’"
[https://www.eetimes.com/document.asp?doc_id=1334789]

Hunt, a Microsoft distinguished engineer and managing director of the company’s Azure Sphere Linux-based operating system for IoT, was in his office in Redmond, Washington, when a colleague came in and showed him a floorplan for a chip to be used in an Xbox controller, which combined a microcontroller and radio on a single die. It was the first time that he had ever seen such a device.

(2) "AI Gets Inference Benchmarks"
[https://www.eetimes.com/document.asp?doc_id=1334852]

The MLPerf consortium released benchmarks to measure inference tasks on servers and client systems. Tools to run MLPerf Inference v0.5 are available on the group’s Web site, but vendors are not expected to start posting results using the metrics until October.

(3) "Embedded Benchmark Calls for Support"
[https://www.eetimes.com/document.asp?doc_id=1334784]

A benchmark in the works for embedded processors aims to provide a free, open-source alternative to the well-established suite of EEMBC benchmarks created by paying members. A small group of mainly academics are calling for support for EmBench, which they hope to release in a 0.5 version before the end of the year.

(4) "AMD Details 7nm Processors, Intel Brings AI to PCs"
[https://www.eetimes.com/document.asp?doc_id=1334764]

AMD certainly got an edge over Intel at Computex in Taipei this week, announcing pricing and availability of the third generation Ryzen processors, which are based on its 7nm Zen 2 core. Meanwhile, Intel announced shipments of its 10nm Intel Core Ice Lake processor and that it is bringing artificial intelligence (AI) to the PC. And, Nvidia revealed its EGX edge AI platform.

(5) "Mediatek Claims 5G Silicon Parity"
[https://www.eetimes.com/document.asp?doc_id=1334756]

In recent years, Mediatek has risen to become the No. 2 supplier in the baseband processor market in terms of market share, mostly by offering lower-cost chips for low- and mid-tier smartphones. It was still a distant No. 2, though.

(6) "Volvo Group to use Nvidia AI for Autonomous Trucks"
[https://www.eetimes.com/document.asp?doc_id=1334847]

As the industry hype over autonomous vehicles moves into the realms of reality, or what's really possible in the near term, one area where it could really have great immediate impact is in the freight industry. Recognizing this, Volvo Group and Nvidia have partnered to use the latter's artificial intelligence (AI) platform to deploy autonomous trucks.

(7) "AMD Details 7nm Processors, Intel Brings AI to PCs"
[https://www.eetimes.com/document.asp?doc_id=1334764]

AMD certainly got an edge over Intel at Computex in Taipei this week, announcing pricing and availability of the third generation Ryzen processors, which are based on its 7nm Zen 2 core. Meanwhile, Intel announced shipments of its 10nm Intel Core Ice Lake processor and that it is bringing artificial intelligence (AI) to the PC. And, Nvidia revealed its EGX edge AI platform.

(8) "Flexible RFID ICs To Tackle Counterfeit Consumer Goods"
[https://www.eetimes.com/document.asp?doc_id=1334853]

Chinese packaging materials firm BSN intends to use flexible electronics firm PragmatIC's RFID ICs in a new printing facility focused on anti-counterfeit solutions for fast-moving consumer goods (FMCG), online sales, and pharmaceutical drugs.

(9) "iBASEt & Amazon Collaborate on Aerospace & Defense Manufacturing Platform"
[https://www.eetimes.com/document.asp?doc_id=1334840]

Software vendor iBASEt is collaborating collaboration with AWS, as part of Amazon Web Services' Smart Factory program, to bring a cloud-based Digital Manufacturing suite for aerospace and defense manufacturers using AWS. "iBASEt is working with AWS to bring the iBASEt Manufacturing Suite on AWS GovCloud where more stringent requirements are in place to protect the data," Sung Kim, chief technology officer of iBASEt told EETimes.

(10) "TSMC, Purdue Team Up to Enhance Chip Security"
[https://www.eetimes.com/document.asp?doc_id=1334823]

Taiwan's Taiwan Semiconductor Manufacturing Co. (TSMC) and Purdue University in the U.S. announced the establishment of a center at the university to enhance semiconductor security, via a press statement last week. The Center for Secured Microelectronics Ecosystem is aimed at safeguarding the semiconductor and tool supply chain from the foundry stage to packaging.

Back to Contents

SIGDA Local Chapter News

We are pleased to announce that Design Automation Conference (DAC) has been promoted to Rank-A conference by China Computer Federation (CCF). The CCF webpage is https://www.ccf.org.cn/. Now DAC is CCF-A conference now! Thanks for the faculty members and researchers that have contributed to this.

Back to Contents

SIGDA Award

Awards at ACM/SIGDA Sponsored Events

DAC 2019: The 56th Design Automation Conference, https://dac.com

1. Best Paper Award

"DREAMPLACE: Deep Learning Toolkit-enabled GPU Acceleration for Modern VLSI Placement" by Yibo Lin (Univ. of Texas at Austin), Shounak Dhar (Univ. of Texas at Austin), Wuxi Li (Univ. of Texas at Austin), Haoxing Ren (NVIDIA Corp., Austin), Brucek Khailany (NVIDIA Corp., Austin) and David Z. Pan (Univ. of Texas at Austin).

2. 2018 Phil Kaufman Award for Distinguished Contributions to Electronic Systems Design

Thomas W. Williams, Synopsys (retired, fellow): "For overall impact on electronic industry through contributions to scan design for testability, related test automation".

3. ACM IEEE A. Richard Newton Technical Impact Award in Electronic Design Automation

Edward B. Eichelberger (IBM retired fellow, IEEE fellow) and Thomas W. Williams (Synopsys retired fellow): for the paper "A Logic Design Structure for LSI Testability," in Proc. of the 14th Design Automation Conference, 1977.

4. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems Donald O. Pederson Best Paper Award

“Caffeine: Towards Uniformed Representation and Acceleration for Deep Convolutional Neural Networks,” by Chen Zhang (Microsoft Research Asia), Guangyu Sun (Peking University), Zhenman Fang (Simon Fraser Univ.), Peipei Zhou (University of California at Los Angeles), Peichen Pan (Falcon Computing), and Jason Cong (University of California at Los Angeles).

5. 2019 ACM TODAES Best Paper Award

"Security in Automotive Networks: Lightweight Authentication and Authorization," by Philipp Mundhenk (TUM CREATE Limited, Singapore), Andrew Paverd (Aalto University, Finland), Artur Mrowca (TUM CREATE Limited, Singapore), Sebastian Steinhorst (TUM CREATE Limited, Singapore), MArtin Lukasiewycz (TUM CREATE Limited, Singapore), Suhaib A. Fahmy(University of Warwick, United Kingdom) and Samarjit Chakraborty (Technische Universita¨t Mu¨nchen, Germany).

6. ACM SIGDA Outstanding Ph.D. Dissertation Award

"Distributed Timing Analysis," by Tsung-Wei Huang, Advisor: Martin D. F. Wong (Univ. of Illinois at Urbana-Champaign).

Back to Contents

"What is" Column

What is Multiprocessor Real-Time Task Scheduling?

Che-Wei Chang, Chang Gung University, Taiwan

Since multiprocessor systems have been proven as an effective way to reduce the energy consumption and thermal problems when high computing throughput is demanded, including multiple processors or cores in a real-time system is also a promising approach to simultaneously run several real-time tasks so as to improving the schedulability for meeting task deadlines. However, such multiprocessor designs make the real-time scheduling problems more complicated, in which task assignment onto processors and task scheduling on each processor have to be jointly considered. When memory and other resources are further allowed to be shared among multiple processors, the memory and shared-resource contentions make the multiprocessor teal-time task scheduling more challenging.

Basically, there are two major types of multiprocessor real-time task scheduling: global scheduling [1] and partitioned scheduling [2]. Regarding global scheduling, when a real-time task is ready for its execution, the task instance is put into a global queue. When a processor is available, a global scheduler picks up a task instance from the global queue

according to some criteria, e.g., the earliest-deadline-first policy, and assigns the task to the available processor. Regarding partitioned scheduling, real-time tasks are statically partitioned onto processors according to some attributes, e.g., computing workloads, memory footprints, and shared resources, of the tasks. When any task is ready for its execution, it can run on only the designated processor. When multiple tasks on a processor are ready, a local task scheduler is needed for the task scheduling on the core. There are also some hybrid solutions, such as semi-partitioned scheduling [3], in which a task can be partitioned into several subtasks, and the subtasks can run on different processor at different time slots, i.e., two subtasks of a task can not run on two processors simultaneously.

To share resources, e.g., kernel data structures and peripherals, that require mutual exclusive accesses, semaphores or mutex locks are needed to guard the resource using, and synchronization protocols or policies are then developed to properly manage semaphores and mutex locks. The Priority Ceiling Protocol (PCP) for static priorities and the Stack Resource Policy (SRP) for dynamic priorities are two milestones for real-time scheduling with shared resources. With the consideration of multiprocessor systems, PCP and SRP have been extended to the Multiprocessor Priority Ceiling Protocol (MPCP) [4] and the Multiprocessor Stack Resource Policy (MSRP) [5], respectively. Task scheduling on multiprocessor systems with MPCP or MSRP are then studied in some recent research [6, 7] ([6] is for MPCP and [7] is for MSRP).

When more and more cores are included in a chip, and more and more processors are placed in a system, the performance bottleneck of multiprocessor systems might be moved from the computing throughput of computing units to the latency and bandwidth of memory devices. Cluster computers serve as a good example of deploying both local and remote memory devices in the cost and performance tradeoff to support large-scale applications. Scheduling a real-time task onto a core of a processor consumes not only the computing time of the core but also the local memory space of the processor. Thus, the memory allocation and task scheduling have to be jointly managed [8] for real-time systems with multiple cores and heterogeneous memory. To better estimate the memory access latency, some real-time systems further partition memory banks and buses for real-time tasks [9] so as to avoid some memory bank/bus contentions among tasks.

References

[1] M. Bertogna, M. Cirinei, and G. Lipar, “Schedulability Analysis of Global Scheduling Algorithms on Multiprocessor Platforms,” in IEEE Transactions on Parallel and Distributed Systems (TPDS), Volume 20, Number 4, 2009.

[2] J.-J. Chen and S. Chakraborty, “Resource Augmentation Bounds for Approximate Demand Bound Functions,” in IEEE Real-Time Systems Symphony (RTSS), 2011.

[3] S. Kato, N. Yamasaki, and Y. Ishikawa, “Semi-Partitioned Scheduling of Sporadic Task Systems on Multiprocessors,” in Euromicro Conference on Real-Time Systems (ECRTS), 2009

[4] R. Rajkumar, “Real-Time Synchronization Protocols for Shared Memory Multiprocessors,” in International Conference on Distributed Computing Systems (ICDCS), 1990.

[5] P. Gai, G. Lipari, and M. D. Natale, “Minimizing Memory Utilization of Real-Time Task Sets in Single and Multi-Processor Systems-on-a-chip,” in IEEE Real-Time Systems Symposium (RTSS), 2001.

[6] F. Nemati, T. Nolte, and M. Behnam, “Partitioning Teal-Time Systems on Multiprocessors with Shared Resources,” in International Conference on Principles of Distributed Systems (OPODIS), 2010.

[7] A. Wieder and B. B. Brandenburg, “Efficient Partitioning of Sporadic Real-Time Tasks with Shared Resources and Spin Locks,” in International Symposium on Industrial Embedded Systems (SIES), 2013.

[8] Che-Wei Chang, Jian-Jia Chen, Tei-Wei Kuo, and Heiko Falk, “Real-Time Task Scheduling on Island-Based Multi-Core Platforms,” in IEEE Transactions on Parallel and Distributed Systems (TPDS), Volume 26, Number 2, 2015

[9] S.-W. Cheng, J.-J. Chen, J. Reineke, and T.-W. Kuo, “Memory Bank Partitioning for Fixed-Priority Tasks in a Multi-Core System,” in IEEE Real-Time Systems Symphony (RTSS), 2017.

Back to Contents

Paper Submission Deadlines

ASP-DAC'20 - Asia and South Pacific Design Automation Conference
Beijing, China

Deadline: Jul 12, 2019
Jan 13-16, 2020
www.aspdac.com

VLSID'20 – Embedded and VLSI Design Conference
Bengaluru, India
Deadline: Jul 15, 2019 (Abstracts due: Jul 7, 2019)
Jan 4-8, 2020
http://www.vlsidesignconference.org

iSES'19 – IEEE Int'l Symposium on Smart Electronic Systems
Rourkela, India
Deadline: Jul 19, 2019
Dec 16-18, 2019
http://www.ieee-ises.org

ICPADS'19 – IEEE Int'l Conference on Parallel and Distributed Systems
Tianjin, China
Deadline: Jul 21, 2019 (Abstracts due: Jul 14, 2019)
Dec 4-6, 2019
http://www.icpads2019.cn

FPT'19 - Int'l Conference on Field-Programmable Technology
Tianjin, China
Deadline: Jul 22, 2019 (Abstracts due: Jul 15, 2019)
Dec 9-13, 2019
http://icfpt.org

ISED'19 – Int'l Symposium on Electronic System Design
Kollam, India
Deadline: Aug 18, 2019
Dec 13-15, 2019
http://isedconf.org

WOSET'19 – Workshop on Open Source EDA Technology (co-located with ICCAD'19)
Westminster, CO
Deadline: Sep 6, 2019
Nov 7, 2019
http://woset.org

DATE'20 - Design Automation and Test in Europe
Grenoble, France
Deadline: Sep 8, 2019
ar 9-13, 2020
http://www.date-conference.com

ISSCC'20 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Deadline: Sep 9, 2019
Feb 16-20, 2020
http://isscc.org

ISQED'20 - Int'l Symposium on Quality Electronic Design
Santa Clara, CA
Deadline: Sep 14, 2019
ar 2019
http://www.isqed.org

FPGA'20 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Seaside, CA
Deadline: Sep 16, 2019
Feb 24-26, 2020
http://www.isfpga.org

Back to Contents

Upcoming Symposia, Conferences and Workshops

ICDCS'19 – IEEE Int'l Conference on Distributed Computing Systems
Dallas, TX
Jul 7-10, 2019
https://theory.utdallas.edu/ICDCS2019

IWBDA'19 - Int'l Workshop on Bio-Design Automation
Cambridge, England
Jul 9-12, 2019
http://www.iwbdaconf.org/2019

ISVLSI'19 – IEEE Computer Society Annual Symposium on VLSI
iami, FL
Jul 15-17, 2019
http://www.isvlsi.org

AHS'19 - NASA/ESA Conference on Adaptive Hardware and Systems
Colchester, UK
Jul 22-24, 2019
http://www.ahs-conf.org

ISLPED'19 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
Lausanne, Switzerland
Jul 29-31, 2019
http://www.islped.org

PACT'19 - Int'l Conference on Parallel Architectures and Compilation Techniques
Seattle, WA
Sep 21-25, 2019
http://www.pactconf.org

BodyNets'19 – Int'l Conference on Body Area Networks
Florence, Italy
Oct 2-3, 2019
http://www.bodynets.org

VLSI-SoC'19 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Cuzco, Peru
Oct 6-9, 2019
www.vlsi-soc.com

EMOCODE'19 – ACM/IEEE Int'l Conference on Formal Methods and Models for Codesign
San Diego, CA
Oct 9-11, 2019
https://memocode.github.io/2019

ICRO'19 – IEEE/ACM Int'l Symposium on Microarchitecture
Columbus, OH
Oct 12-16, 2019
http://www.microarch.org/micro52

ESWEEK'19 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)
New York, NY
Oct 13-18, 2019
http://www.esweek.org

NOCS'19 – IEEE/ACM Int'l Symposium on Networks-on-Chip

New York, NY
Oct 17-18, 2019
https://www.engr.colostate.edu/nocs2019

BIOCAS'19 – Biomedical Circuits and Systems Conference
Nara, Japan
Oct 17-19, 2019
http://www.biocas2018.org

ICCAD'19 – IEEE/ACM Int'l Conference on Computer-Aided Design
Westminster, CO
Nov 4-7, 2019
http://www.iccad.com

HiPC'19 – IEEE Int'l Conference on High Performance Computing
Hyderabad, India
Dec 17-20, 2019
http://www.hipc.org

HiPEAC'20: Int'l Conference on High Performance Embedded Architectures & Compilers
Balogna, Italy
Jan 20-22, 2020
https://www.hipeac.net

Back to Contents

Funding Opportunities

'"North America"'

Keck Foundation
Deadline: various
http://www.wmkeck.org/grant-programs/research/

USDA Foundational Program
Deadline: various
http://www.grants.gov/web/grants/view-opportunity.html?oppId=283836

NATO: Science for Peace and Security
Deadline: Proposals accepted anytime; reviews take place February 1 and May 15
http://www.nato.int/cps/en/natolive/87260.htm

Air Force Research Laboratory: Research Collaboration Program (BAA-RQKM-2013-0005)
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=212295

Federal Aviation Administration Grants for Aviation Research (FAA-12-01)
Deadline: open to December 2019
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=134953

AFRL RD/RV University Cooperative Agreement
Deadline: open to Nov 23, 2020
http://www.grants.gov/web/grants/view-opportunity.html?oppId=280237

NASA Fellowship Programs
Deadline: Various
http://science.nasa.gov/researchers/sara/fellowship-programs/

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Students-Etudiants/PG-CS/index_eng.asp

itacs Accelerate PhD Fellowship: Ontario Business Grants Program
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/...

Collaborative Research and Development Grants
(including DND/NSERC Research Partnership Grants)
http://www.nserc-crsng.gc.ca/Professors-Professeurs/RPP-PP/CRD-RDC_eng.asp

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Professors-Professeurs/CFS-PCP/index_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Engage-Mobiliser_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Collaborate-Collaborer_eng.asp
Research and Development Funding for Business Innovation (Multiple Organizations)
Deadline: Various
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/

'''Europe'''

Horizon 2020
Deadline: Various
http://goo.gl/geBouC

German Academic Exchange Service (DAAD)
Deadline: Various
https://www.daad.org/scholarship

German Research Foundation (DFG)
Deadline: Various
http://www.dfg.de/en

Helmholtz Association
Deadline: Various
https://www.helmholtz.de/en

Leibniz Association
Deadline: Various
http://www.leibniz-gemeinschaft.de/en/home

Leopoldina
Deadline: Various
https://www.leopoldina.org/en/about-us

ax Planck Society
Deadline: Various
https://www.mpg.de/en

Swiss National Science Foundation
Deadline: Various
http://www.snf.ch/en/

'''Asia'''

Korea:

National Research Foundation of Korea
Deadline: Various
http://www.nrf.re.kr/nrf_eng_cms/show.jsp?show_no=90&check_no=89&c_relation=0&c_...

China:

National Natural Science Foundation of China
Deadline: Various
http://www.nsfc.gov.cn/publish/portal1/

Singapore:

National Research Foundation (NRF) Singapore
http://www.nrf.gov.sg
RIE 2020 plan
Deadline: Various
http://www.nrf.gov.sg/rie2020

India:

inistry of Electronics and Information Technology
Deadline: Various
http://meity.gov.in/content/research-development

Department of Science and Technology (Nano Mission)
Deadline: Various
http://nanomission.gov.in/

University Grants Commission
Deadline: Various
http://www.ugc.ac.in/

inistry of Education Academic Research Fund
Deadline: Various
https://www.olga.moe.gov.sg/default.aspx

Agency for Science Technology and Research (A*STAR) Science and Engineering Research Council (SERC)
Deadline: Various
https://www.a-star.edu.sg/Research/Funding-Opportunities/Grants-Sponsorship.aspx

ultiple Funding
Deadline: Various
http://www.computerscienceonline.org/cs-scholarships/

'"Oceania/Polynesia"'

Polynesian Cultural Center (Hawaii) - International Student Scholarship Program
For studying in BYU Hawaii
http://www.polynesia.com/students.html

New Zealand:

inistry of Business, Innovation and Employment
Deadline: Various
http://www.mbie.govt.nz/

Australia:

Premier's Research and Industry Fund
Deadline: Various
http://www.statedevelopment.sa.gov.au/science/premiers-research-and-industry-fun...

Australian Research Council
Deadline: Various
http://www.arc.gov.au

'"South America"'

Brazil:

Coordination for the Improvement of Higher Education Personnel (CAPES)
Deadline: Various
http://www.iie.org/programs/capes#.WAu2kJMrJPM

inistry of Science, Technology, Innovation and Communications (CNPq)
Deadline: Various
http://www.cnpq.br/

'"Africa"'

Other scholarships for African Students (list of over 30 different scholarships)
Deadline: Various
http://www.afterschoolafrica.com/12264/list-annual-engineering-scholarships-afri...

Nigeria:

Bilateral Education Agreement (BEA) Awards (both Undergraduate and Post Graduate)
Deadline: Nomination interview - March'17
http://www.fsb.gov.ng/index.php/scholarship/menu-styles/bilateral-agreement

Federal Scholarship Board
Deadline: Various
http://www.fsb.gov.ng/index.php

Back to Contents

CALL for Abstracts / Participation: MLCAD

1st ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)

The workshop focuses on Machine Learning (ML) methods for all aspects of CAD and electronic system design. The predecessor of this workshop was held at the Design, Automation and Test in Europe (DATE) Conference in March 2019. The workshop is sponsored by both IEEE Council on Electronic Design Automation (CEDA) and ACM Special Interest Group on Design Automation (SIGDA). Around one third of the workshop program will consist of invited and keynote speakers from major CAD and Industrial Companies, who will present their vision on machine learning for CAD.

*** DATES ***
Abstract Submission: July 7, 2019
Author Notification: July 15, 2019
Registration Deadline: July 22, 2019
Workshop: September 3-4, 2019

Two Ways to Attend:
1. Presenter: Submit a half page abstract ~500 words incl. title and authors and submit PDF to https://easychair.org/conferences/?conf=mlcad2019. Accepted submissions entitle to a talk at the workshop and a full paper submission to the 1st ACM/IEEE Workshop on MLCAD post workshop proceedings (for full info check mlcad.itec.kit.edu).
2. Attendee: We encourage senior researchers as well as PhD students to be part of this first workshop. Participation is limited to maintain the creative open discussion atmosphere of the workshop. Registration deadline is July 22nd 2019. Registration will be handled on a first-come, first-serve basis.

Post-Workshop ACM/IEEE Proceedings
Formal shared ACM/IEEE proceedings will be published after the workshop. All speakers are invited to submit full papers about two months after the workshop.
Venue
LCAD 2019 is held at the Solara Resort & Spa, which is located in Canmore, (Banff area), Alberta, Canada. The location is near to the Canadian Rocky Mountains and the beautiful Banff National Park of Canada. The location is reachable with flights to Calgary International Airport (YYC), which is about one hour drive away.

ore info: http://mlcad.itec.kit.edu

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Back to Contents

Call for Participation: CAD Contest at ICCAD 2019

The CAD Contest at ICCAD (http://iccad-contest.org/) is a challenging, multi-month, research and development competition, focusing on advanced, real-world problems in the field of Electronic Design Automation (EDA). It is open to multi-person teams world-wide. Each year the organizing committee announce three challenging problems in different topic areas provided by industrial companies. Contestants can participate in one or more problems. The prizes will be awarded at an ICCAD special session dedicated to this contest.

Since its inaugural year of 2012, the CAD Contest at ICCAD has been attracting more than a hundred teams per year (112 teams from 12 regions in 2015, 135 teams from 11 regions in 2016, and 123 teams from 10 regions in 2017, 136 teams from 11 regions in 2018), fostering productive industry-academia collaborations, and leading to hundreds of publications in top-tier conferences and journals. The contest undoubtedly boosts EDA research and keeps enhancing its impact.

YOU ARE INVITED TO PARTICIPATE!!!

Contest Problems
Problem A: Logic Regression on High Dimensional Boolean Space (Cadence Design Systems, Inc.)
Problem B: System-level FPGA Routing with Timing Division Multiplexing Technique (Synopsys, Inc.)
Problem C: LEF/DEF Based Open-Source Global Router (Mentor Graphics & University of California San Diego)

Tentative Contest Schedule
Registration deadline: May 10, 2019
Alpha test submission: June 21, 2019
Beta test submission: July 26, 2019
Final submission: August 30, 2019
Award ceremony: November 4, 2019 (at ICCAD)
Awards for each problem
1st Place Award: NTD 50,000 / team (approx. US$ 1,650), Certificate / person, Open-source bonus for Problem C: US$ 5,500 / team
2nd Place Award: NTD 30,000 / team (approx. US$ 1,000), Certificate / person, Open-source bonus for Problem C: US$ 1,500 / team
3rd Place Award: NTD 30,000 / team (approx. US$ 1,000), Certificate / person, Open-source bonus for Problem C: US$ 500 / team
Honorable Mentions: Certificate / person

Organizing Committee
Contest chair: Ulf Schlichtmann (Technical University of Munich, Germany)
Contest co-chairs: Sabya Das (Synopsys, Inc., USA) Ing-Chao Lin (National Cheng Kung University, Taiwan) Mark Po-Hung Lin (National Chung Cheng University, Taiwan)
Topic chairs: Ching-Yi Huang, Chi-An (Rocky) Wu, Tung-Yuan Lee, and Chih-Jen (Jacky) Hsu (Cadence Design Systems Inc.) Yu-Hsuan Su, Emplus Huang, Hung-Hao Lai, and Yi-Cheng Zhao (Synopsys Inc.) Alexander Volkov, Sergei Dolgov (Mentor Graphics) Lutong Wang, Bangqi Xu (University of California San Diego)
Back to Contents

Call for Papers: ASP-DAC 2020

https://aspdac2020.github.io/aspdac20/index.html

Areas of Interest:
Original papers in, but not limited to, the following areas are invited.

1. System-Level Modeling and Design Methodology:
1.1. HW/SW co-design, co-simulation and co-verification
1.2. System-level design exploration, synthesis and optimization
1.3. System-level formal verification
1.4. System-level modeling, simulation and validation tools/methodology
2. Embedded Systems and Cyberphysical Systems:
2.1. Many- and multi-core SoC architecture
2.2. IP/platform-based SoC design
2.3. Domain-specific architecture
2.4. Dependable architecture
2.5. Cyber physical system
2.6. Internet of things
3. Embedded Systems Software:
3.1. Kernel, middleware and virtual machine
3.2. Compiler and toolchain
3.3. Real-time system
3.4. Resource allocation for heterogeneous computing platform
3.5. Storage software and application
3.6. Human-computer interface
4. Memory Architecture and Near/In Memory Computing:
4.1. Storage system and memory architecture
4.2. On-chip memory architectures and management: Scratchpads, compiler, controlled memories, etc.
4.3. Memory and storage hierarchies with emerging memory technologies
4.4. Near-memory and in-memory computing
4.5. Memory architecture and management for emerging memory technologies
5. Neural Network and Neuromorphic Computing:
5.1. Hardware and devices for neuromorphic and neural network computing
5.2. Design method for learning on a chip
5.3. Systems for neural computing (including deep neural networks)
5.4. Neural network acceleration techniques including GPGPU, FPGA and dedicated ASICs
5.5. CAD for bio-inspired and neuromorphic systems
6. Analog, RF, Mixed Signal, and Photonics:
6.1. Analog/mixed-signal/RF synthesis
6.2. Analog layout, verification, and simulation techniques
6.3. High-frequency electromagnetic simulation of circuit
6.4. Mixed-signal design consideration
6.5. Communication architectures using nanophotonics, RF, 3D, etc.
6.6. Networks-on-chip and NoC-based system design
7. Lower Power Design and Approximate Computing:
7.1. Power modeling, analysis and simulation
7.2. Low-power design and methodology
7.3. Thermal aware design
7.4. Energy harvesting and battery management
7.5. Hardware techniques for approximate/stochastic computing
8. Logic/High-Level Synthesis and Optimization:
8.1. High-level synthesis tool and methodology
8.2. Combinational, sequential and asynchronous logic synthesis
8.3. Logic synthesis and physical design technique for FPGA
8.4. Technology mapping
9. Physical Design:
9.1. Floorplanning, partitioning and placement
9.2. Interconnect planning and synthesis
9.3. Placement and routing optimization
9.4. Clock network synthesis

9.5. Post layout and post-silicon optimization
9.6. Package/PCB/3D-IC routing
10. Design for Manufacturability and Reliability:
10.1. Reticle enhancement, lithography-related design and optimization
10.2. Resilience under manufacturing variation
10.3. Design for manufacturability, yield, and defect tolerance
10.4. Reliability, aging and soft error analysis
10.5. Design for reliability, aging, and robustness
10.6. Machine learning for smart manufacturing and process control
11. Timing and Signal/Power Integrity:
11.1. Deterministic/statistical timing and performance analysis and optimization
11.2. Power/ground and package modeling, analysis and optimization
11.3. Signal/power integrity, EM modeling and analysis
11.4. Extraction, TSV and package modeling
11.5. 2D/3D on-chip power delivery network analysis and optimization
12. Testing, Validation, Simulation, and Verification:
12.1. ATPG, BIST and DFT
12.2. System test and 3D IC test
12.3. Online test and fault tolerance
12.4. Memory test and repair
12.5. RTL and gate-leveling modeling, simulation, and verification
12.6. Circuit-level formal verification
12.7. Device/circuit-level simulation tool and methodology
13. Hardware and Embedded Security:
13.1. Hardware-based security
13.2. Detection and prevention of hardware Trojans
13.3. Side-channel attacks, fault attacks and countermeasures
13.4. Design and CAD for security
13.5. Cyberphysical system security
13.6. Nanoelectronic security
13.7. Supply chain security and anti-counterfeiting
14. Emerging Technologies and Applications:
14.1. Biomedical, biochip, and biodata processing
14.2. Big/thick data, datacenter
14.3. Advanced multimedia application
14.4. Energy-storage/smart-grid/smart-building design and optimization
14.5. Automotive system design and optimization
14.6. New transistor/device and process technology: spintronic, phase-change, single-electron etc.
14.7. Nanotechnology, MEMS, quantum computing etc.
Please note that each paper shall be accompanied by at least one different conference registration at the speaker's registration rate (e.g., two speaker registrations are needed for presenting two accepted papers). But any registered co-author can present the work at the conference. ACM and IEEE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author of the paper. ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals.

Submission of Papers:

Deadline for submission: 5 PM AOE (Anywhere on earth) July 12 (Fri), 2019 (extended)
Notification of acceptance: Sep. 9 (Mon), 2019
Deadline for final version: 5 PM AOE (Anywhere on earth) Nov. 4 (Mon), 2019
Please submit regular papers via http://tsys.jp/aspdac/cgi/submit_top.cgi
Please submit university design contest papers via http://tsys.jp/aspdac-udc/cgi/submit_top.cgi

Back to Contents

SIGDA Diversity Advancement Grant 2019-2020

SIGDA has initiated a new travel grant specifically for students from under represented groups (URP) to travel to SIGDA sponsored conferences.
- Support include registration fee and travelling (USD100, USD400 or USD800, depending on the distance)
- No need to have papers in the conference

- Support letter from supervisor
- Write a report of not less than 800 words after the conference
- Deadline: August 31, 2020 and at least one month before the event (SIGDA sponsored conferences held Oct 1, 2019 to Sept 30, 2020)
- Applicants are encouraged to join the SIGDA membership
- For more information, visit https://www.sigda.org/diversity/

Back to Contents

Call for Papers: WOSET 2019

Second Workshop on Open-Source EDA Technology (http://woset.org).
Co-located with ICCAD 2019, Th Nov 7,The Westin Westminster, Westminster CO.

This one-day workshop aims to galvanize the open-source EDA movement. The workshop will bring together EDA researchers who are committed to open-source principles to share their experiences and coordinate efforts towards developing a reliable, fully open- source EDA flow. The workshop will feature presentations that overview existing open-source tools, along with sessions and posters describing future planned EDA tools. The workshop will include a panel to brainstorm the current status and future challenges for open-source EDA, and to coordinate efforts and ensure quality and interoperability across open-source tools.

Submissions (2-4 pages):
Overview of an existing or under-development open-source EDA tool.
Overview of support infrastructure (e.g. EDA databases and design benchmarks).
Open-source cloud-based EDA tools
Position statements (e.g. critical gaps, blockers/obstacles)

Important dates:
Sept 6th 2019: submission due date.
Sept 15th 2019: notification due date.

Submission URL:
https://easychair.org/conferences/?conf=woset19

For inquires: please contact sherief_reda@brown.edu

Back to Contents

Notice to Authors

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
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