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da Design Automation
The resource for EDA Professionals

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Comments from the Editors

Dear ACM/SIGDA member,

We are excited to present to you the May e-newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from upcoming conference and funding deadlines, hot research topics to news from our community.
Get involved and contact us if you want to contribute an article or announcement.

Happy reading!

Aida Todri-Sanial
Yu Wang
Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit http://www.acm.org/renew or call

between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or
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"'Rajsaktish Sankaranarayanan'", E-Newsletter Associate Editor for SIGDA Researcher spotlight column

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SIGDA News

(1) "MIPS R6 Architecture Now Available for Open Use"
[https://www.eetimes.com/document.asp?doc_id=1334489]

MIPS 32-bit and 64-bit architecture – the most recent version, release 6 – will become available Thursday (March 28) for anyone to download at MIPS Open web page.

(2) "Samsung Ready with 5-nm EUV"
[https://www.eetimes.com/document.asp?doc_id=1334567]

Samsung announced that it has completed work and is taking orders for a 5-nm foundry process using extreme ultraviolet lithography. It will offer 25% greater density and either 10% more performance or 20% less power consumption than its 7-nm node with EUV announced in October.

(3) "GPUs Holding Back AI Innovation"
[https://www.eetimes.com/document.asp?doc_id=1334579]

GPUs are widely used to accelerate AI computing, but are the limitations of GPU technology slowing down innovation in the development of neural networks?

(4) "5G Needs More Memory to Compute"
[https://www.eetimes.com/document.asp?doc_id=1334512]

Today’s cellphone networks aren’t your dad’s cellphone networks. In fact, 5G not only represents a vast leap in communications compared to the flip phone days of 3G, it’s also going to be more memory hungry.

(5) "Qualcomm Targets AI Inferencing in the Cloud"
[https://www.eetimes.com/document.asp?doc_id=1334548]

Qualcomm is taking another stab at the server, throwing its hat into what is rapidly becoming a crowded ring — AI inference processing for the data center.

(6) "AI Research Targets Nvidia, Mobile"
[https://www.eetimes.com/document.asp?doc_id=1334533]

A researcher from the University of Texas at Austin described a chip for training deep neural networks that he said can outperform an Nvidia V100 — even using low-cost mobile DRAM. At the same event, Arm discussed research on a chip that can significantly increase efficiency for computer vision jobs run on mobile systems.

(7) "AI Inferencing Chip Targets Edge Servers"
[https://www.eetimes.com/document.asp?doc_id=1334550]

Flex Logix — best known as a supplier of embedded FPGAs and other IP — is marketing its first chip, an edge inference co-processor targeting edge applications.

(8) "Intel & Lockheed Martin Collaborate to Launch New Hardened Security Solution"
[https://www.eetimes.com/document.asp?doc_id=1334582]

Lockheed Martin has collaborated with chip maker Intel to deliver a hardened security solution based on Intel's second-generation Intel Xeon Scalable processors that deliver more sophistication than software-only solutions. The solution, which is designed for use in the data center, aims to address the ever-increasing complexity of cyber threats while providing more consistent service performance.

(9) "Apple, Q'comm Deal Leaves Open Questions"
[https://www.eetimes.com/document.asp?doc_id=1334570]

Apple and Qualcomm announced that they have dropped all litigation in a multi-billion-dollar patent licensing dispute that has dragged on for more than two years across courts in China, Germany, and the U.S. However, the sketchy details of the settlement leave many unanswered questions.

(10) "AVs Need New Compute Platforms"
[https://www.eetimes.com/document.asp?doc_id=1334583]

While autonomous vehicle (AV) development dominates discussion in the electronics industry, firms are a long way off from having the right computing platforms, safety certification standards and regulations, says a new survey highlighting current thinking on exactly where we are on the path to autonomy.

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SIGDA Award

Awards at ACM/SIGDA Sponsored Events

ISPD 2019: The 2019 International Symposium on Physical Design, http://www.ispd.cc

ISPD Lifetime Achievement Award: This award is given to individuals who have made outstanding contributions to the field of physical design automation over multiple decades. The purpose is to recognize their lifetime of achievements and contributions in terms of research work, education, and professional service. This year the award goes to '"Prof. Alberto Sangiovanni-Vincentelli"' (University of California at Berkeley).

Best Paper Award: "Pin Access-Driven Design Rule Clean and DFM Optimized Routing of Standard Cells under Boolean Constraints", by Nikolay Ryzhenko, Steven Burns, Anton Sorokin, Mikhail Talalay (Intel Corporation).

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"What is" Column

What is Software-Defined Storage?

Yung-Feng Lu, National Taichung University of Science and Technology, Taiwan

With the rapid growth of data centers and the unprecedented increase in storage demands, we need a quick and easy way to manage and store data. The Software-Defined Storage (SDS) is one of the solutions for this issue by abstracting the storage control operations from the storage devices and set it inside a centralized controller in the software layer. The

primary goal for any software defined system (e.g., SDN, SDS) is to hide all the complexities of the management and control functionality of the system resources from the end users. These resources may refer to any system component like the components and devices that store and process the data. SDS facilitates and simplifies system complexity, and maintain an acceptable level of QoS [1]. It addresses all the challenges of traditional storage systems.

SDS decouples storage software from the underlying storage devices. It does this by creating a virtualized software management layer that operates above the storage hardware. Typically, key components of SDS architecture consists of three layers: infrastructure layer, control layer, and application layer. The infrastructure layer combines various storage devices that store raw data. The controller in the control layer is considered to be the most critical element in SDS. This is where the storage resources in the infrastructure layer interact with the application layer. The control layer converts different policies to different instructions within the system. The last layer in this architecture is the application layer, which contains different applications and allows end users to interact with storage devices.

SDS has some characteristics distinguishing it from other systems, especially traditional storage systems [2], [3], [4]:

(1) Abstraction: Abstraction of logical storage services and functions from the underlying physical storage system and, in some cases, aggregate across multiple different implementations. SDS collects all underlying hardware on a single centralized unit. This unit captures all the resources in the system. As a result, any event that occurs in any part of the system can be easily recognized and handled.

(2) Automation: The operations on the SDS are done automatically in response to user requests in case they need to configure storage space in the system. SDS replaces technical details with automated, policy-driven storage configurations and service level agreements.

(3) Commodity hardware: Commodity hardware with storage logic is abstracted into a software layer. Whether it is considered commodity storage hardware or network communication resources, the system uses the available resources to build the infrastructure. Therefore, if there is a need to scale the system or any change, then the hardware is ready to be added without any impact on system performance and work.

(4) Programmability: Many APIs are available to provide visual control for the resources that integrate several system components to enable the system automation. The programmability handles the resource management and change services to meet the applications needs.

(5) Policy Driven: One of the most important features in SDS is the ability to control and process all policies in the system. The control is separated into two control layers, user and storage layer. Where availability, reliability, latency, and other issues are specified by user layer.

(6) Scale-out architecture: The resources in the SDS can be dynamically inserted and deleted to increase the capacity of the SDS in a scale up and out fashion.

(7) Resource pooling: SDS is based on the concept of virtualization since all system resources are collected or abstracted on a single logical place and clustered into multiple groups called pools controlled by centralized control unit. This reduces the overhead of administrators allocating resources because the allocation or deallocation of resources is done dynamically on-demand.

Many excellent SDS systems have been proposed in the past five years. IOFlow [5] was the first complete SDS architecture. IOFlow supports end-to-end policies to specify the processing of IO streams from VMs to shared storage. Retro [6] is the framework for implementing resource management strategies in a multi-tenant distributed system. It can be thought of as an incarnation of SDS, which separates the controller from the mechanisms needed to implement it.

Now, let’s illustrate an excellent SDS, Crystal, in more details. Tinedo et al. [7] presented the first SDS architecture (named Crystal) whose core objective is to efficiently support multitenancy in object stores. In a Crystal’s architecture, which consists of control plane and data plane. In control plane, Crystal provides administrators with a system-agnostic DSL (Domain-Specific Language) to define SDS services via high-level policies. In data plane, Crystal’s data plane has two core extension points: Inspection triggers and filters.

In Crystal SDS, the flexibility of developing control policy, such as using the popular IFTTT (If-This-Then-That) service, provides an easier way to develop application-aware storage systems, automatic parameters tuning, policy-based management, movement, and protection of systems and information. To achieve this, Crystal separates high-level policies from the mechanisms that implement them at the data plane, to avoid hard-coding the policies in the system itself. To do so, it uses three abstractions: filter, metric, and controller, in addition to policies.
- Filter: A filter is a piece of code that a system administrator can inject into the data plane to perform custom computations on incoming object requests.

- Inspection trigger: This abstraction represents information accrued from the system to automate the execution of filters.
- Controller: In Crystal, a controller represents an algorithm that manages the behavior of the data plane based on monitoring metrics.
- Policy: The policies should be extensible for really allowing the system to satisfy evolving requirements. This means that the policy structure must help to incorporate new filters, triggers and controllers.

[1] Fenggang Wu and G. Sun, “Software-defined storage,” University of Minnesota, Report, Dec 2013.

[2] J. Mace, P. Bodik, R. Fonseca, and M. Musuvathi. Retro: Targeted resource management in multitenant distributed systems. In USENIX NSDI’15, 2015.

[3] “The fundamentals of software-defined storage “simplicity at scale for cloud architectures”,” Coraid Inc, Technical Report, 2013.

[4] A. Darabseh, M. Al-Ayyoub, Y. Jararweh, E. Benkhelifa, M. Vouk and A. Rindos, "SDStorage: A Software Defined Storage Experimental Framework," 2015 IEEE International Conference on Cloud Engineering, Tempe, AZ, 2015, pp. 341-346.

[5] E. Thereska, H. Ballani, G. O’Shea, T. Karagiannis, A. Rowstron, T. Talpey, R. Black, and T. Zhu. Ioflow: a software-defined storage architecture. In ACM SOSP’13, pages 182–196, 2013.

[6] J. Mace, P. Bodik, R. Fonseca, and M. Musuvathi. Retro: Targeted resource management in multitenant distributed systems. In USENIX NSDI’15, 2015.

[7] Raúl Gracia-Tinedo, Josep Sampé, Edgar Zamora, Marc Sánchez-Artigas, Pedro García-López, Yosef Moatti, and Eran Rom. 2017. Crystal: Software-Dened Storage for Multi-Tenant Object Stores. In 15th USENIX Conference on File and Storage Technologies. USENIX Association, Santa Clara, CA, 243–256. https://www.usenix.org/conference/fast17/technical-sessions/presentation/gracia-tinedo

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Paper Submission Deadlines

IWBDA'19 - Int'l Workshop on Bio-Design Automation
Cambridge, England
Deadline: May 10, 2019
Jul 9-12, 2019
http://www.iwbdaconf.org/2019

NOCS'19 – IEEE/ACM Int’l Symposium on Networks-on-Chip
New York, NY
Deadline: May 17, 2019 (Abstracts due: May 10, 2019)
Oct 17-18, 2019
https://www.engr.colostate.edu/nocs2019

MEMOCODE'19 – ACM/IEEE Int’l Conference on Formal Methods and Models for Codesign
San Diego, CA
Deadline: Jun 7, 2019 (Abstracts due: May 31, 2019)
Oct 9-11, 2019
https://memocode.github.io/2019

HiPC'19 – IEEE Int'l Conference on High Performance Computing
Hyderabad, India
Deadline: Jun 14, 2019 (Abstracts due: Jun 7, 2019)
Dec 17-20, 2019
http://www.hipc.org

iSES’19 – IEEE Int’l Symposium on Smart Electronic Systems
Rourkela, India
Deadline: Jul 19, 2019

Dec 16-18, 2019
http://www.ieee-ises.org

FPT'19 - Int'l Conference on Field-Programmable Technology
Tianjin, China
Deadline: Jul 22, 2019 (Abstracts due: Jul 15, 2019)
Dec 9-13, 2019
http://icfpt.org

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Upcoming Symposia, Conferences and Workshops

HOST'19 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
Tysons Corner, VA
May 6-10, 2019
http://www.hostsymposium.org

GLSVLSI'19 – ACM Great Lakes Symposium on VLSI
Washington D.C., USA
May 9-11, 2019
http://www.glsvlsi.org

ASYNC'19 – IEEE Int'l Symposium on Asynchronous Circuits and Systems
Hirosaki, Japan
May 12-15, 2019
http://asyncsymposium.org

NATW'19 – IEEE North Atlantic Test Workshop
Essex, Vermont
May 13-15, 2019
http://natw.ieee.org

ISCAS'19 – IEEE Int'l Symposium on Circuits and Systems
Sapporo, Japan
May 26-29, 2019
http://iscas2019.org

DAC'19 – Design Automation Conference
Las Vegas, NV
Jun 2-6, 2019
http://www.dac.com/

SLIP'19 – ACM/IEEE International Workshop on System-Level Interconnect Prediction [co-located with DAC'19]
Las Vegas, NV
Jun 2, 2019
http://sliponline.org

LCTES'19 – Int'l Conference on Languages Compilers, Tools and Theory of Embedded Systems
Phoenix, AZ
Jun 22, 2019
https://conf.researchr.org/home/LCTES-2019

ISCA'19 – Int'l Symposium on Computer Architecture
Phoenix, AZ
Jun 22-26, 2019
https://iscaconf.org

ICDCS'19 – IEEE Int'l Conference on Distributed Computing Systems
Dallas, TX
Jul 7-10, 2019
https://theory.utdallas.edu/ICDCS2019

ISVLSI'19 – IEEE Computer Society Annual Symposium on VLSI
Miami, FL
Jul 15-17, 2019
http://www.isvlsi.org

AHS'19 - NASA/ESA Conference on Adaptive Hardware and Systems
Colchester, UK
Jul 22-24, 2019
http://www.ahs-conf.org

ISLPED'19 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
Lausanne, Switzerland
Jul 29-31, 2019
http://www.islped.org

PACT'19 - Int'l Conference on Parallel Architectures and Compilation Techniques
Seattle, WA
Sep 21-25, 2019
http://www.pactconf.org

BodyNets'19 – Int'l Conference on Body Area Networks
Florence, Italy
Oct 2-3, 2019
http://www.bodynets.org

VLSI-SoC'19 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Cuzco, Peru
Oct 6-9, 2019
www.vlsi-soc.com

MICRO'19 – IEEE/ACM Int'l Symposium on Microarchitecture
Columbus, OH
Oct 12-16, 2019
http://www.microarch.org/micro52

ESWEEK'19 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)
New York, NY
Oct 13-18, 2019
http://www.esweek.org

BIOCAS'19 – Biomedical Circuits and Systems Conference
Nara, Japan
Oct 17-19, 2019
http://www.biocas2018.org

ICCAD'19 – IEEE/ACM Int'l Conference on Computer-Aided Design
Westminster, CO
Nov 4-7, 2019
http://www.iccad.com

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Funding Opportunities

'"North America"'

Keck Foundation
Deadline: various
http://www.wmkeck.org/grant-programs/research/

USDA Foundational Program

Deadline: various
http://www.grants.gov/web/grants/view-opportunity.html?oppId=283836

NATO: Science for Peace and Security
Deadline: Proposals accepted anytime; reviews take place February 1 and May 15
http://www.nato.int/cps/en/natolive/87260.htm

Air Force Research Laboratory: Research Collaboration Program (BAA-RQKM-2013-0005)
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=212295

Federal Aviation Administration Grants for Aviation Research (FAA-12-01)
Deadline: open to December 2019
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=134953

AFRL RD/RV University Cooperative Agreement
Deadline: open to Nov 23, 2020
http://www.grants.gov/web/grants/view-opportunity.html?oppId=280237

NASA Fellowship Programs
Deadline: Various
http://science.nasa.gov/researchers/sara/fellowship-programs/

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Students-Etudiants/PG-CS/index_eng.asp

itacs Accelerate PhD Fellowship: Ontario Business Grants Program
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/...

Collaborative Research and Development Grants
(including DND/NSERC Research Partnership Grants)
http://www.nserc-crsng.gc.ca/Professors-Professeurs/RPP-PP/CRD-RDC_eng.asp

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Professors-Professeurs/CFS-PCP/index_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Engage-Mobiliser_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Collaborate-Collaborer_eng.asp
Research and Development Funding for Business Innovation (Multiple Organizations)
Deadline: Various
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/

'"Europe"'

Horizon 2020
Deadline: Various
http://goo.gl/geBouC

German Academic Exchange Service (DAAD)
Deadline: Various
https://www.daad.org/scholarship

German Research Foundation (DFG)
Deadline: Various
http://www.dfg.de/en

Helmholtz Association
Deadline: Various
https://www.helmholtz.de/en

Leibniz Association
Deadline: Various

http://www.leibniz-gemeinschaft.de/en/home

Leopoldina
Deadline: Various
https://www.leopoldina.org/en/about-us

Max Planck Society
Deadline: Various
https://www.mpg.de/en

Swiss National Science Foundation
Deadline: Various
http://www.snf.ch/en/

'''Asia'''

Korea:

National Research Foundation of Korea
Deadline: Various
http://www.nrf.re.kr/nrf_eng_cms/show.jsp?show_no=90&check_no=89&c_relation=0&c_...

China:

National Natural Science Foundation of China
Deadline: Various
http://www.nsfc.gov.cn/publish/portal1/

Singapore:

National Research Foundation (NRF) Singapore
http://www.nrf.gov.sg
RIE 2020 plan
Deadline: Various
http://www.nrf.gov.sg/rie2020

India:

Ministry of Electronics and Information Technology
Deadline: Various
http://meity.gov.in/content/research-development

Department of Science and Technology (Nano Mission)
Deadline: Various
http://nanomission.gov.in/

University Grants Commission
Deadline: Various
http://www.ugc.ac.in/

Ministry of Education Academic Research Fund
Deadline: Various
https://www.olga.moe.gov.sg/default.aspx

Agency for Science Technology and Research (A*STAR) Science and Engineering Research Council (SERC)
Deadline: Various
https://www.a-star.edu.sg/Research/Funding-Opportunities/Grants-Sponsorship.aspx

Multiple Funding
Deadline: Various
http://www.computerscienceonline.org/cs-scholarships/

'''Oceania/Polynesia'''

Polynesian Cultural Center (Hawaii) - International Student Scholarship Program
For studying in BYU Hawaii
http://www.polynesia.com/students.html

New Zealand:

inistry of Business, Innovation and Employment
Deadline: Various
http://www.mbie.govt.nz/

Australia:

Premier's Research and Industry Fund
Deadline: Various
http://www.statedevelopment.sa.gov.au/science/premiers-research-and-industry-fun...

Australian Research Council
Deadline: Various
http://www.arc.gov.au

'"South America"'

Brazil:

Coordination for the Improvement of Higher Education Personnel (CAPES)
Deadline: Various
http://www.iie.org/programs/capes#.WAu2kJMrJPM

Ministry of Science, Technology, Innovation and Communications (CNPq)
Deadline: Various
http://www.cnpq.br/

'"Africa"'

Other scholarships for African Students (list of over 30 different scholarships)
Deadline: Various
http://www.afterschoolafrica.com/12264/list-annual-engineering-scholarships-afri...

Nigeria:

Bilateral Education Agreement (BEA) Awards (both Undergraduate and Post Graduate)
Deadline: Nomination interview - March'17
http://www.fsb.gov.ng/index.php/scholarship/menu-styles/bilateral-agreement

Federal Scholarship Board
Deadline: Various
http://www.fsb.gov.ng/index.php
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Call for Participation: CAD Contest at ICCAD 2019

The CAD Contest at ICCAD (http://iccad-contest.org/) is a challenging, multi-month, research and development competition, focusing on advanced, real-world problems in the field of Electronic Design Automation (EDA). It is open to multi-person teams world-wide. Each year the organizing committee announce three challenging problems in different topic areas provided by industrial companies. Contestants can participate in one or more problems. The prizes will be awarded at an ICCAD special session dedicated to this contest.

Since its inaugural year of 2012, the CAD Contest at ICCAD has been attracting more than a hundred teams per year (112 teams from 12 regions in 2015, 135 teams from 11 regions in 2016, and 123 teams from 10 regions in 2017, 136 teams from 11 regions in 2018), fostering productive industry-academia collaborations, and leading to hundreds of publications in top-tier conferences and journals. The contest undoubtedly boosts EDA research and keeps enhancing its

impact.

YOU ARE INVITED TO PARTICIPATE!!!

Contest Problems
Problem A: Logic Regression on High Dimensional Boolean Space (Cadence Design Systems, Inc.)
Problem B: System-level FPGA Routing with Timing Division Multiplexing Technique (Synopsys, Inc.)
Problem C: LEF/DEF Based Open-Source Global Router (Mentor Graphics & University of California San Diego)

Tentative Contest Schedule
Registration deadline: May 10, 2019
Alpha test submission: June 21, 2019
Beta test submission: July 26, 2019
Final submission: August 30, 2019
Award ceremony: November 4, 2019 (at ICCAD)
Awards for each problem
1st Place Award: NTD 50,000 / team (approx. US$ 1,650), Certificate / person, Open-source bonus for Problem C: US$ 5,500 / team
2nd Place Award: NTD 30,000 / team (approx. US$ 1,000), Certificate / person, Open-source bonus for Problem C: US$ 1,500 / team
3rd Place Award: NTD 30,000 / team (approx. US$ 1,000), Certificate / person, Open-source bonus for Problem C: US$ 500 / team
Honorable Mentions: Certificate / person

Organizing Committee
Contest chair: Ulf Schlichtmann (Technical University of Munich, Germany)
Contest co-chairs: Sabya Das (Synopsys, Inc., USA) Ing-Chao Lin (National Cheng Kung University, Taiwan) Mark Po-Hung Lin (National Chung Cheng University, Taiwan)
Topic chairs: Ching-Yi Huang, Chi-An (Rocky) Wu, Tung-Yuan Lee, and Chih-Jen (Jacky) Hsu (Cadence Design Systems Inc.) Yu-Hsuan Su, Emplus Huang, Hung-Hao Lai, and Yi-Cheng Zhao (Synopsys Inc.) Alexander Volkov, Sergei Dolgov (Mentor Graphics) Lutong Wang, Bangqi Xu (University of California San Diego)
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Call for Papers: HiPC 2019

26th IEEE International Conference on High Performance Computing, Data, and Analytics
December 17-20, 2019, Hyderabad, India
https://hipc.org/

HiPC 2019 will be the 26th edition of the IEEE International Conference on High Performance Computing, Data, Analytics and Data Science. HiPC serves as a forum to present current work by researchers from around the world as well as highlight activities in Asia in the areas of high performance computing and data science. The meeting focuses on all aspects of high performance computing systems, and data science and analytics, and their scientific, engineering, and commercial applications.

Authors are invited to submit original unpublished research manuscripts that demonstrate current research in all areas of high performance computing, and data science and analytics, covering all traditional areas and emerging topics including from machine learning, big data analytics and blockchain. Each submission should be submitted to one of the tracks listed under the two broad themes of High Performance Computing and Data Science.

High Performance Computing tracks:

Algorithms: This track invites papers that describe original research on developing new parallel and distributed computing algorithms, and related advances. Examples of topics that are of interest include (but not limited to):
* New parallel and distributed algorithms and design techniques;
* Advances in enhancing algorithmic properties or providing guarantees (e.g., fault tolerance, resilience, concurrency, data locality, communication-avoiding);
* Classical and emerging computation models (e.g., parallel/distributed models, quantum computing, neuromorphic and other bioinspired models);
* Provably efficient parallel and distributed algorithms for advanced scientific computing and irregular applications (e.g., numerical linear algebra, graph algorithms, computational biology); and
* Algorithmic techniques for resource allocation and optimization (e.g., scheduling, load balancing, resource management);

Architectures: This track invites papers that describe original research on the design and evaluation of high performance computing architectures, and related advances. Examples of topics of interest include (but not limited to):
* Design and evaluation of high performance processing architectures (e.g., reconfigurable, system-on-chip, manycores, vector processors);
* Design and evaluation of networks for high performance computing platforms (e.g., interconnect topologies, network-on-chip);
* Design and evaluation of memory, cache and storage architectures (e.g., 3D, photonic, Processing-In-Memory, NVRAM, burst buffers, parallel I/O);
* Approaches to improve architectural properties (e.g., energy/power efficiency, reconfigurable, resilience/fault tolerance, security/privacy); and
* Emerging computational architectures (e.g., quantum computing, neuromorphic and other bioinspired architectures).

Applications: This track invites papers that describe original research on the design and implementation of scalable applications for execution on parallel and distributed platforms, and related advances. Examples of topics of interest include (but not limited to):
* Design and implementation of shared and distributed memory parallel applications (e.g., scientific computing and industry applications, emerging applications in IoT and life sciences - biology, medicine, chemistry, etc.);
* Design and simulation methodologies for scaling applications on peta- and exascale platforms (e.g., co-design approaches, hardware/software co-design, heterogeneous and hybrid programming);
* Hardware acceleration of parallel applications (e.g., CPU/GPUs, multi-GPU clusters, FPGA, vector processors, manycore); and
* Design of application benchmarks for parallel and distributed platforms.

Systems Software: This track invites papers that describe original research on the design, implementation and evaluation of systems software for high performance computing platforms, and related advances. Examples of topics of interest include (but not limited to):
* Scalable systems and software architectures for high performance computing (e.g., middleware, operating systems, I/O services);
* Techniques to enhance parallel performance (e.g., compiler/runtime optimization, learning from application traces, profiling);
* Techniques to enhance parallel application development and productivity (e.g., Domain-Specific Languages, programming environments, performance/correctness checking and debugging);
* Techniques to deal with uncertainties, hardware/software resilience, and fault tolerance;
* Software for cloud, data center, and exascale platforms (e.g., middleware tools, schedulers, resource allocation, data migration, load balancing); and
* Software and programming paradigms for heterogeneous platforms (e.g., libraries for CPU/GPU, multi-GPU clusters, and other accelerator platforms);

Data Science tracks:

Scalable Algorithms and Analytics: This track invites papers that describe original research on developing scalable algorithms for data analysis at scale, and related advances. Examples of topics of interest include (but not limited to):
* New scalable algorithms for fundamental data analysis tasks (supervised, unsupervised learning, and pattern discovery);
* Scalable algorithms that are designed to address the characteristics of different data sources and settings (e.g., graphs, social networks, sequences, data streams);
* Scalable algorithms and techniques to reduce complexity of large-scale data (e.g., streaming, sublinear data structures, summarization, compressive analytics);
* Scalable algorithms that are designed to address requirements in different data-driven application domains (e.g., life sciences, business, agriculture); and
* Scalable algorithms that ensure the transparency and fairness of the analysis.

Scalable Systems and Software: This track invites papers that describe original research on developing scalable systems and software for handling data at scale, and related advances. Examples of topics of interest include (but not limited to):
* Design of scalable system software to support various applications (e.g., recommendation systems, web search, crowdsourcing applications, streaming applications)
* Design of scalable system software for various architectures (e.g., OpenPower, GPUs, FPGAs).
* Architectures and systems software to support various operations in large data frameworks (e.g., storage, retrieval, automated workflows, data organization, visualization, visual analytics, human-in-the-loop);
* Design and implementation of systems software for distributed data frameworks (e.g., distributed file system, virtualization, cloud services, resource optimization, scheduling); and
* Standards and protocols for enhancing various aspects of data analytics (e.g., open data standards, privacy preserving

and secure schemes).

One or more best paper awards will be given for outstanding contributed papers.

IMPORTANT DATES
Abstract Submission: Friday, June 7, 2019
Paper Submission: Friday, June 14, 2019
Reviews for Rebuttals: Monday, July 29, 2019
Rebuttals due: Monday, August 5, 2019
Initial Submission Decision: Monday, August 19, 2019
Revisions Due: Friday, September 20, 2019
Author Notification: Monday, September 30, 2019
Camera Ready: Monday, October 14, 2019

Easychair Submission link: https://easychair.org/conferences/?conf=hipc2019

Manuscript Guidelines
Submitted manuscripts should be structured as technical papers and may not exceed ten (10) single-spaced double-column pages using 10-point size font on 8.5x11 inch pages (IEEE conference style), including figures, tables, and references. See IEEE style templates at this page for details.

Journal Special Issue: Authors of selected high quality papers in HiPC 2019 will be invited to submit extended version of their papers for possible publication in a special issue of Journal of Parallel and Distributed Computing.

PROGRAM CHAIRS
Ananth Kalyanaraman, Washington State University, USA
George Karypis, University of Minnesota, USA

PROGRAM VICE-CHAIRS
HPC Tracks:
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Data Science Tracks:
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Call for Nominations of Service Awards

SIGDA CALLS FOR NOMINATIONS OF SERVICE AWARDS
(Deadline May 5, 2019)

SIGDA has restructured its service awards, and will be giving two annual service awards.

Distinguished Service Award: The SIGDA Distinguished Service Award is given to individuals who have dedicated many years of their career in extraordinary services to promoting, leading, or creating ACM/SIGDA programs or events.
Meritorious Service Award: The SIGDA Meritorious Service Award is given to individuals who have performed professional services above and beyond traditional service to promoting, leading, or creating ACM/SIGDA programs or events.

At any given year, the number of Distinguished Service Award will be up to 2, and the number of Meritorious Service Award will be up to 4.

Nominations should consist of:
Award type being nominated.
Name, address, phone number and email of person making the nomination.
Name, affiliation, address, email, and telephone number of the nominee for whom the award is recommended.
A statement (between 200 and 500 words long) explaining why the nominee deserves the award. Note that the award is given for service that goes above and beyond traditional services.
Up to 2 additional letters of support. Include the name, affiliation, email address, and telephone number of the letter writer(s). Supporters of multiple candidates are strongly encouraged to compare the candidates in their letters.

Note that the nominator and reference shall come from active SIGDA volunteers. Deadline of the nomination every year: March 1 (Except 2019, May 5)

Please send all your nomination materials as one pdf file to SIGDA-Award@acm.org before the deadline.
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Call for Papers: NOCS 2019

13th IEEE/ACM International Symposium on Networks-on-Chip

October 17 – 18, 2019, New York, USA (Co-located with Embedded Systems Week 2019)

https://www.engr.colostate.edu/nocs2019/

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to interdisciplinary research on on-chip, package-scale, chip-to-chip, and datacenter rack-scale communication technology, architecture, design methods, applications and systems. NOCS brings together scientists and engineers working on network-on-chip (NoC) innovations and applications from inter-related research communities, including discrete optimization and algorithms, computer architecture, networking, circuits and systems, packaging, embedded systems, and design automation. Topics of interest include, but are not limited to:

NoC Architecture and Implementation
- Network architecture (topology, routing, arbitration)
- Timing, synchronous/asynchronous communication
- NoC reliability issues and solutions
- Security issues and solutions in NoC architectures
- Power/thermal issues at NoC un-core and system-level
- Network interface issues and solutions
- Signaling and circuit design for NoC links and routers

Communication Analysis, Optimization, & Verification
- NoC performance analysis and Quality of Service
- Modeling, simulation, and synthesis of NoC
- Verification, debug and test of NoC
- NoC design and simulation methodologies and tools
- Benchmarks, experiences on NoC-based hardware
- Communication-efficient algorithms
- Communication workload characterization & evaluation

Novel NoC Technologies
- Optical, wireless, CNT, and other emerging technologies
- NoC for 2.5D and 3D packages
- Package-specific NoC design
- Network coding and compression solutions
- Approximate computing for NoC and NoC-based systems

NoC for Intelligent Physical Systems
- NoC design for Deep Learning
- Mapping of existing and emerging applications onto NoC
- NoC case studies, application-specific NoC design
- NoC for FPGA, structured ASIC, CMP and MPSoC
- NoC designs for heterogeneous systems
- NoC for CPU-GPU and data-center-on-a-chip (DCoC)
- Scalable modeling of NoC

- Machine learning for NoC and NoC-based Systems

NoC at the Un-Core and System-level
- Design of memory subsystem (un-core) including memory controllers, caches, cache coherence protocols in NoC
- NoC for new memory/storage technologies
- NoC support for processing-in-memory
- OS support for NoC
- Programming models for NoCs
- Interactions between large-scale systems (datacenter, edge and fog computing) and NoC-based building blocks

Inter/Intra-Chip and Rack-Scale Network
- Unified inter/intra-chip networks
- Hybrid chip-scale and datacenter rack-scale networks
- All aspects of inter-chip and rack-scale network design

Electronic paper submission requires a full paper, up to 8 double-column ACM (sigconf) format pages, including figures and references. The program committee will use a double-blind review process to evaluate papers based on scientific merit, innovation, relevance, and presentation. Submitted papers must describe original work that has not been published before or is under review by another conference or journal at the same time. Each submission will be checked for any significant similarity to previously published works or for simultaneous submission to other archival venues, and such papers will be rejected. Proposals for special sessions and demos are invited. Paper submissions and demo proposals by industry researchers or engineers to share their experiences and perspectives are also welcome. A percentage of accepted papers will be recommended for publication in an IEEE journal after revision according to the reviewers' comments. Please find the detailed submission instructions for paper submission, special session, and demo proposals at the submission webpage.

Important Dates (Anywhere on Earth)
Abstract registration: May 10, 2019
Full paper submission: May 17, 2019
Notification of acceptance: July 8, 2019
Final version due: July 22, 2019

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Notice to Authors

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
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