Special Interest Group
Design Automation
The resource for EDA Professionals

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Online archive: http://www.sigda.org/newsletter

Comments from the Editors

Dear ACM/SIGDA member,

We are excited to present to you the April e-newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from upcoming conference and funding deadlines, hot research topics to news from our community.
Get involved and contact us if you want to contribute an article or announcement.

Happy reading!

[Aida Todri-Sanial](#)
Yu Wang
Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit http://www.acm.org/renew or call between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or 1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org

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SIGDA News

(1) "Nvidia Mum on 7-nm GPU"
[https://www.eetimes.com/document.asp?doc_id=1334447]

Nvidia's annual graphics event attracted some 8,000 attendees here, but one expected guest couldn't make it — a 7-nm GPU.

(2) "UNH-IOL Adds NVMe over TCP Testing"
[https://www.eetimes.com/document.asp?doc_id=1334432]

The University of New Hampshire Interoperability Lab (UNH-IOL) has expanded its Non-Volatile-Memory-Express-over-Fabric (NVMe-oF) testing capabilities to include NVMe over TCP. Ratified in November 2018, the NVMe/TCP spec adds Transmission Control Protocol to the list of NVMe transport protocols, which previously included Fibre Channel, remote direct memory access (RDMA), and PCIe.

(3) "Intel CPU Shortage Opens Door for AMD"
[https://www.eetimes.com/document.asp?doc_id=1334472]

An ongoing shortage of Intel PC processors is opening the door for AMD, setting the stage for a battle between the two longtime rivals in the second half of the year, according to one market watcher.

(4) "AI Trolls for Data Center Woes"
[https://www.eetimes.com/document.asp?doc_id=1334423]

Hewlett-Packard Enterprise is using neural networks to predict failures on some of the 4 million hard disk drives that it is

InfoSight service monitors. The project taught HPE that using neural networks takes time, specialized expertise, and some big iron.

(5) "Sensors, Networks Enable Precision Agriculture"
[https://www.eetimes.com/document.asp?doc_id=1334454]

Two powerful trends – the Internet of Things (IoT) and data analytics – are generating lots of press for their industrial and infrastructure applications. But there is another application space that is quietly gaining momentum in the application of these technologies: food production.

(6) "Lidar Startup Uses Metamaterials to Steer Beams"
[https://www.eetimes.com/document.asp?doc_id=1334450]

Lumotive, a Seattle-based, venture-backed startup, is unveiling Wednesday a lidar technology based on metamaterials, a relatively new and exotic technological approach that few if any of its competitors have adopted.

(7) "What's Next for Human-Machine Interface: Touchless Control"
[https://www.eetimes.com/document.asp?doc_id=1334460]

There's a race on to market the first devices with touchless / gesture control. LG led the pack at MWC, and Google and Apple appear very close on its heels. Those two could possibly introduce products featuring this kind of human-machine interface (HMI) before 2019 is out.

(8) "6G Kicks Off with Trump Tweets, FCC Action, and a Summit"
[https://www.eetimes.com/document.asp?doc_id=1334466]

Interest in 6G has picked up momentum in recent weeks, even more so after US President Donald Trump's tweet saying American companies must step up their efforts towards it. Now the Federal Communications Commission (FCC) has created a new category of experimental licenses for use of frequencies between 95 GHz and 3 THz.

(9) "U.S. Court Finds Apple Infringed Qualcomm IP"
[https://www.eetimes.com/document.asp?doc_id=1334446]

A U.S. federal court found that several iPhone models infringe on patents held by Qualcomm, a major setback for Apple in the patent fight between the two companies that has been unfolding in several jurisdictions throughout the world.

(10) "Tsinghua Lures SMIC Co-CEO Zhao to Bolster DRAM"
[https://www.eetimes.com/document.asp?doc_id=1334471]

China's Tsinghua Unigroup, the state-owned holding company that controls most of the nation's semiconductor assets, may snatch a co-CEO from Semiconductor Manufacturing International Corp. (SMIC) to revive a plan to build a domestic DRAM industry.

SIGDA Award

Best Paper Awards at ACM/SIGDA Sponsored Events

DATE 2019: The Design, Automation and Test in Europe, https://www.date-conference.com/proceedings-archive/2019/html/bestpaper.html

D Track: "Enhancing Reliability of STT-MRAM Caches by Eliminating Read Disturbance Accumulation", by Elham Cheshmikhani (Sharif University of Technology), Hamed Farbeh (Amirkabir University of Technology) and Hossein Asadi (Sharif University of Technology).

A Track: "When Capacitors Attack: Formal Method Driven Design and Detection of Charge-Domain Trojans", by Xiaolong Guo (University of Florida), Huifeng Zhu (Washington University in St. Louis), Yier Jin (University of Florida) and Xuan Zhang (Washington University in St. Louis).

T Track: "Error-Shielded Register Renaming Subsystem for a Dynamically Scheduled Out-of-Order Core", by Ron Gabor (Intel), Yiannakis Sazeides (University of Cyprus), Arkady Bramnik (Intel), Alexandros Andreou (University of Cyprus), Chrysostomos Nicopoulos (University of Cyprus), Karyofyllis Patsidis (Democritus University of Thrace),

Dimitris Konstantinou (Democritus University of Thrace) and Giorgos Dimitrakopoulos (Democritus University of Thrace).

E Track: "Data Subsetting: A Data-Centric Approach to Approximate Computing", by Younghoon Kim (Purdue University), Swagath Venkataramani (IBM T. J. Watson Research Center), Nitin Chandrachoodan (Indian Institute of Technology Madras) and Anand Raghunathan (Purdue University).

"What is" Column

What is Automotive Design Automation?

Chung-Wei Lin, National Taiwan University

Automotive design, especially of software and electronics, has become more complex than ever due to the development of advanced driver assistance systems (ADAS), autonomous functions, and connected applications. This complexity poses significant challenges to automotive industry and its predominantly manual approach to design. Thus, design automation plays an increasingly important role in assisting system designers to verify design correctness, improving design quality, accelerating design development, reducing design cost, and preventing redesign or recall.

Similar to electronic design automation, one of the fundamental concepts in automotive design automation is the V model [1]. In a design process, there are decomposition (e.g., from system requirements to component specifications) and composition (e.g., from implemented components to integrated systems), and we need automatic, or at least semi-automatic, design tools to continuously optimize, analyze, verify, and validate the design. As a special case of embedded systems and cyber-physical systems, automotive design automation can also be categorized into three core parts [2]: modeling, design (including synthesis and optimization), and analysis (including verification, simulation, and testing). The following paragraphs give an example comparing placement in electronic design automation and task allocation in automotive design automation from the perspectives of modeling, design, and analysis.

(1) Modeling. Placement in electronic design automation is based on models (not fabricated chips). A netlist can be modeled by a graph, where a vertex represents a logic gate, an edge represents the connection between logic gates, and a vertex comes with attributes such as size, shape, and delay of the corresponding logic gate. Similarly, task allocation in automotive design automation is based on models (not manufactured cars). A function from sensing and perception to control and actuation can be modeled by a graph, where a vertex represents a task, an edge represents the signal between tasks, and a vertex comes with attributes such as size, period and priority of the corresponding task.

(2) Design. Placement aims to place logic gates onto the given area, and is accompanied by detailed routing to connect the logic gates. Similarly, task allocation is to allocate tasks onto computational units, such as electronic control units, connected by networks, and is accompanied by scheduling to decide how to propagate the signals between tasks on the networks. Here, placement, routing, task allocation, and scheduling are usually optimization problems, and they can be solved in many different ways such as mathematical programming or heuristic search.

(3) Analysis. Timing analysis, as an example, can be applied to both cases. With timing models of logic gates and routing wires, the timing properties of placement and routing, i.e., physical design, can be analyzed. With timing models of computational units and networks, the timing properties of task allocation and scheduling can be analyzed. If any requirement is violated, a redesign is triggered.

It is worth mentioning that modeling, design, and analysis are not sequential steps. On the contrary, there are often interactions between them. For example, analysis can guide design in achieving better solution quality. In conclusion, we believe that techniques inspired and created in electronic design automation can help address similar design challenges in the automotive industry, and are applicable to an even wider spectrum of design problems in embedded systems, cyber-physical systems, and other complex systems.

[1] https://en.wikipedia.org/wiki/V-Model

[2] Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, IT Press, ISBN 978-0-262-53381-2, 2017.

Paper Submission Deadlines

ICCAD'19 – IEEE/ACM Int'l Conference on Computer-Aided Design
Westminster, CO
Deadline: Apr 8, 2019 (Abstracts due: Apr 1, 2019)
Nov 4-7, 2019
http://www.iccad.com

ESWEEK'19 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)
New York, NY
Deadline: Apr 12, 2019 (Abstracts due: Apr 5, 2019)
Oct 13-18, 2019
http://www.esweek.org

BodyNets'19 – Int'l Conference on Body Area Networks
Florence, Italy
Deadline: Apr 15, 2019
Oct 2-3, 2019
http://www.bodynets.org

VLSI-SoC'19 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Cuzco, Peru
Deadline: Apr 25, 2019 (Abstracts due: Apr 18, 2019)
Oct 6-9, 2019
www.vlsi-soc.com

IWBDA'19 - Int'l Workshop on Bio-Design Automation
Cambridge, England
Deadline: May 10, 2019
Jul 9-12, 2019
http://www.iwbdaconf.org/2019

FPT'19 - Int'l Conference on Field-Programmable Technology
Tianjin, China
Deadline: Jul 22, 2019 (Abstracts due: Jul 15, 2019)
Dec 9-13, 2019
http://icfpt.org

Upcoming Symposia, Conferences and Workshops

ISPD'19 – ACM Int'l Symposium on Physical Design
San Francisco, CA
Apr 14-17, 2019
http://www.ispd.cc

HOST'19 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
Tysons Corner, VA
May 6-10, 2019
http://www.hostsymposium.org

GLSVLSI'19 – ACM Great Lakes Symposium on VLSI
Washington D.C., USA
May 9-11, 2019
http://www.glsvlsi.org

ASYNC'19 – IEEE Int'l Symposium on Asynchronous Circuits and Systems
Hirosaki, Japan
May 12-15, 2019
http://asyncsymposium.org

NATW'19 – IEEE North Atlantic Test Workshop
Essex, Vermont
May 13-15, 2019
http://natw.ieee.org

ISCAS'19 – IEEE Int'l Symposium on Circuits and Systems
Sapporo, Japan
May 26-29, 2019
http://iscas2019.org

DAC'19 – Design Automation Conference
Las Vegas, NV
Jun 2-6, 2019
http://www.dac.com/

SLIP'19 – ACM/IEEE International Workshop on System-Level Interconnect Prediction [co-located with DAC'19]
Las Vegas, NV
Jun 2, 2019
http://sliponline.org

LCTES'19 – Int'l Conference on Languages Compilers, Tools and Theory of Embedded Systems
Phoenix, AZ
Jun 22, 2019
https://conf.researchr.org/home/LCTES-2019

ISCA'19 – Int'l Symposium on Computer Architecture
Phoenix, AZ
Jun 22-26, 2019
https://iscaconf.org

ISVLSI'19 – IEEE Computer Society Annual Symposium on VLSI
Miami, FL
Jul 15-17, 2019
http://www.isvlsi.org

AHS'19 - NASA/ESA Conference on Adaptive Hardware and Systems
Colchester, UK
Jul 22-24, 2019
http://www.ahs-conf.org

ISLPED'19 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
Lausanne, Switzerland
Jul 29-31, 2019
http://www.islped.org

BIOCAS'19 – Biomedical Circuits and Systems Conference
Nara, Japan
Oct 17-19, 2019
http://www.biocas2018.org

Funding Opportunities

'''North America'''

Keck Foundation
Deadline: various
http://www.wmkeck.org/grant-programs/research/

USDA Foundational Program
Deadline: various
http://www.grants.gov/web/grants/view-opportunity.html?oppId=283836

NATO: Science for Peace and Security
Deadline: Proposals accepted anytime; reviews take place February 1 and May 15
http://www.nato.int/cps/en/natolive/87260.htm

Air Force Research Laboratory: Research Collaboration Program (BAA-RQKM-2013-0005)
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=212295

Federal Aviation Administration Grants for Aviation Research (FAA-12-01)
Deadline: open to December 2019
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=134953

AFRL RD/RV University Cooperative Agreement
Deadline: open to Nov 23, 2020
http://www.grants.gov/web/grants/view-opportunity.html?oppId=280237

NASA Fellowship Programs
Deadline: Various
http://science.nasa.gov/researchers/sara/fellowship-programs/

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Students-Etudiants/PG-CS/index_eng.asp

itacs Accelerate PhD Fellowship: Ontario Business Grants Program
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/...

Collaborative Research and Development Grants
(including DND/NSERC Research Partnership Grants)
http://www.nserc-crsng.gc.ca/Professors-Professeurs/RPP-PP/CRD-RDC_eng.asp

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Professors-Professeurs/CFS-PCP/index_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Engage-Mobiliser_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Collaborate-Collaborer_eng.asp
Research and Development Funding for Business Innovation (Multiple Organizations)
Deadline: Various
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/

'''Europe'''

Horizon 2020
Deadline: Various
http://goo.gl/geBouC

German Academic Exchange Service (DAAD)
Deadline: Various
https://www.daad.org/scholarship

German Research Foundation (DFG)
Deadline: Various
http://www.dfg.de/en

Helmholtz Association
Deadline: Various
https://www.helmholtz.de/en

Leibniz Association
Deadline: Various
http://www.leibniz-gemeinschaft.de/en/home

Leopoldina
Deadline: Various
https://www.leopoldina.org/en/about-us

Max Planck Society
Deadline: Various
https://www.mpg.de/en

Swiss National Science Foundation
Deadline: Various
http://www.snf.ch/en/

'''Asia'''

Korea:

National Research Foundation of Korea
Deadline: Various
http://www.nrf.re.kr/nrf_eng_cms/show.jsp?show_no=90&check_no=89&c_relation=0&c_...

China:

National Natural Science Foundation of China
Deadline: Various
http://www.nsfc.gov.cn/publish/portal1/

Singapore:

National Research Foundation (NRF) Singapore
http://www.nrf.gov.sg
RIE 2020 plan
Deadline: Various
http://www.nrf.gov.sg/rie2020

India:

Ministry of Electronics and Information Technology
Deadline: Various
http://meity.gov.in/content/research-development

Department of Science and Technology (Nano Mission)
Deadline: Various
http://nanomission.gov.in/

University Grants Commission
Deadline: Various
http://www.ugc.ac.in/

Ministry of Education Academic Research Fund
Deadline: Various
https://www.olga.moe.gov.sg/default.aspx

Agency for Science Technology and Research (A*STAR) Science and Engineering Research Council (SERC)
Deadline: Various
https://www.a-star.edu.sg/Research/Funding-Opportunities/Grants-Sponsorship.aspx

Multiple Funding
Deadline: Various
http://www.computerscienceonline.org/cs-scholarships/

'''Oceania/Polynesia'''

Polynesian Cultural Center (Hawaii) - International Student Scholarship Program

For studying in BYU Hawaii
http://www.polynesia.com/students.html

New Zealand:

inistry of Business, Innovation and Employment
Deadline: Various
http://www.mbie.govt.nz/

Australia:

Premier's Research and Industry Fund
Deadline: Various
http://www.statedevelopment.sa.gov.au/science/premiers-research-and-industry-fun...

Australian Research Council
Deadline: Various
http://www.arc.gov.au

'''South America'''

Brazil:

Coordination for the Improvement of Higher Education Personnel (CAPES)
Deadline: Various
http://www.iie.org/programs/capes#.WAu2kJMrJPM

Ministry of Science, Technology, Innovation and Communications (CNPq)
Deadline: Various
http://www.cnpq.br/

'''Africa'''

Other scholarships for African Students (list of over 30 different scholarships)
Deadline: Various
http://www.afterschoolafrica.com/12264/list-annual-engineering-scholarships-afri...

Nigeria:

Bilateral Education Agreement (BEA) Awards (both Undergraduate and Post Graduate)
Deadline: Nomination interview - March'17
http://www.fsb.gov.ng/index.php/scholarship/menu-styles/bilateral-agreement

Federal Scholarship Board
Deadline: Various
http://www.fsb.gov.ng/index.php

Call for Papers: ASAP 2019

The 30th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2019)
Cornell Tech, New York, USA, July 15-17, 2019
Website: asap2019.csl.cornell.edu

The 30th IEEE International Conference on Application-specific Systems, Architectures and Processors 2019 will take place in Cornell Tech, New York, United States.

The history of the event traces back to the International Workshop on Systolic Arrays, organized in 1986 in Oxford, UK. It later developed into the International Conference on Application Specific Array Processors. With its current title, it was organized for the first time in Chicago, USA in 1996. Since then it has alternated between Europe and North-America. The conference will cover the theory and practice of application-specific systems, architectures, and processors. The 2019

conference will build upon traditional strengths in areas such as computer arithmetic, cryptography, compression, signal and image processing, network processing, reconfigurable computing, application-specific instruction-set processors, and hardware accelerators.

TOPICS OF INTEREST (but not limited to)
Big data analytics
Cloud computing infrastructures and acceleration
Heterogeneous computing in data centers
Accelerating data center workloads
FPGA-based deep learning
Embedded systems and domain-specific solutions (digital media, gaming, automotive applications)
Accelerating genomic computations
Acceleration of data analytics
Reconfigurable computing in the IoT era
Applications in finance
Wireless and mobile systems
Application-aware controller synthesis
Emerging technologies (optical models, 3D Interconnects, devices)
Reconfigurable accelerators
Hardware and software architectures for cyber-physical systems
Distributed systems & networks
Critical issues (security, energy efficiency, fault-tolerance)
Autonomous and semi-autonomous large-scale CPS
Autonomic computing systems
High-level design methods (hardware/software co-design, compilers)
Simulations and prototyping (performance analysis, verification tools)
Socio-technical systems

IMPORTANT DATES
Abstract deadline: April 9, 2019
Full paper deadline: April 15, 2019
Decision notification: May 6, 2019
Camera ready version: May 29, 2019

SUBMISSION OF PAPERS
All manuscripts will be reviewed by at least three members of the program committee. Submissions should be a complete manuscript or, in special cases, may be a summary of relevant work. Manuscript for full paper should not exceed 8 single-space, double-column pages using 10-point size font on 8.5x11 inch pages (IEEE conference style) including references, figures, and tables. Manuscript for short papers should not exceed 4 single-space, double-column pages. Manuscripts for posters should not exceed 2 single-spaced, double-column pages. Submitted papers should not have appeared in or be under submission for a different workshop, conference or journal. It is also expected that all accepted papers (full, short or poster) will be presented at ASAP by one of the authors. Accepted full and short papers will be included in the proceedings and published in IEEE Xplore. Failure to present will result in the removal of the submission from the proceedings before publication. All papers must be submitted electronically in PDF format.

Submission website: https://asap2019.csl.cornell.edu/submission/

Call for Participation: HOST 2019

IEEE International Symposium on Hardware Oriented Security and Trust (HOST) 2019
http://www.hostsymposium.org/
May 6-10, 2019
The Hiton, Tysons Corner, USA

Important dates:
Early registration is available by March 29, 2019, 11:59 p.m. (PST). The registration link is as below.
http://www.hostsymposium.org/registration.php

Hilton Tysons Corner CONFERENCE HOTEL Reservations
Hotel room block deadline at special conference rate: April 12, 2019 at 5:00 p.m. Eastern time (or until filled)

Student travel support applications
- HOST main program
To apply, please complete the <http://www.hostsymposium.org/form> and email to HOSTStudentTravel@gmail.com with subject line "Joe Smith: Student Travel Grant" (replacing Joe Smith with your name) by Monday, April 8, 2019. The decision will be announced no later than Friday April 12, 2019. More details will be available on http://www.hostsymposium.org/>
-WISE workshop
Application requirements can be found http://www.wise-workshop.org/Support.html

HOST is an annual symposium which aims to facilitate the rapid growth of hardware-based security research and development. HOST 2019 Conference Program is available now. Major highlights include:
8 Tutorials
- Security and Trust in the Analog/Mixed-Signal/RF Domain: A Survey and a Perspective
- Property Driven Hardware Security
- Circuit Techniques for Energy-efficient Hardware Security
- System-on-Chip Platform Security Assurance: Architecture, Implementation, Validation, and Deployment
- Side Channel Attacks and Countermeasures
- Enabling a Secure Development Lifecycle for Hardware
- Secure Processor Architectures in the Era of Spectre and Meltdown
- CAD for Security
3 Keynote talks
3 Visionary talks
2 Panels
Panel I: Hardware Security Beyond the Digital Domain
Panel II: The Impact of Machine Learning on Hardware Security Research
25 Technical papers
30+ Hardware Demos
3 Workshops
WISE: The 3rd Workshop for Women in Hardware and Systems Security (WISE)
TAME: Trusted and Assured MicroElectronics Forum
ESSA: Workshop on Energy-Secure System Architectures
More information about the conference program can be found at https://easychair.org/smart-program/HOST2019. We encourage you to share it with colleagues who are interested in learning more about the exciting area of hardware and systems security.

Call for Participation: CAD Contest at ICCAD 2019

The CAD Contest at ICCAD (http://iccad-contest.org/) is a challenging, multi-month, research and development competition, focusing on advanced, real-world problems in the field of Electronic Design Automation (EDA). It is open to multi-person teams world-wide. Each year the organizing committee announce three challenging problems in different topic areas provided by industrial companies. Contestants can participate in one or more problems. The prizes will be awarded at an ICCAD special session dedicated to this contest.

Since its inaugural year of 2012, the CAD Contest at ICCAD has been attracting more than a hundred teams per year (112 teams from 12 regions in 2015, 135 teams from 11 regions in 2016, and 123 teams from 10 regions in 2017, 136 teams from 11 regions in 2018), fostering productive industry-academia collaborations, and leading to hundreds of publications in top-tier conferences and journals. The contest undoubtedly boosts EDA research and keeps enhancing its impact.

YOU ARE INVITED TO PARTICIPATE!!!

Contest Problems
Problem A: Logic Regression on High Dimensional Boolean Space (Cadence Design Systems, Inc.)
Problem B: System-level FPGA Routing with Timing Division Multiplexing Technique (Synopsys, Inc.)
Problem C: LEF/DEF Based Open-Source Global Router (Mentor Graphics & University of California San Diego)

Tentative Contest Schedule
Registration deadline: May 10, 2019
Alpha test submission: June 21, 2019
Beta test submission: July 26, 2019
Final submission: August 30, 2019

Award ceremony: November 4, 2019 (at ICCAD)
Awards for each problem
1st Place Award: NTD 50,000 / team (approx. US$ 1,650), Certificate / person, Open-source bonus for Problem C: US$ 5,500 / team
2nd Place Award: NTD 30,000 / team (approx. US$ 1,000), Certificate / person, Open-source bonus for Problem C: US$ 1,500 / team
3rd Place Award: NTD 30,000 / team (approx. US$ 1,000), Certificate / person, Open-source bonus for Problem C: US$ 500 / team
Honorable Mentions: Certificate / person

Organizing Committee
Contest chair: Ulf Schlichtmann (Technical University of Munich, Germany)
Contest co-chairs: Sabya Das (Synopsys, Inc., USA) Ing-Chao Lin (National Cheng Kung University, Taiwan) Mark Po-Hung Lin (National Chung Cheng University, Taiwan)
Topic chairs: Ching-Yi Huang, Chi-An (Rocky) Wu, Tung-Yuan Lee, and Chih-Jen (Jacky) Hsu (Cadence Design Systems Inc.) Yu-Hsuan Su, Emplus Huang, Hung-Hao Lai, and Yi-Cheng Zhao (Synopsys Inc.) Alexander Volkov, Sergei Dolgov (Mentor Graphics) Lutong Wang, Bangqi Xu (University of California San Diego)

Call for Papers: HiPC 2019

26th IEEE International Conference on High Performance Computing, Data, and Analytics
December 17-20, 2019, Hyderabad, India
https://hipc.org/

HiPC 2019 will be the 26th edition of the IEEE International Conference on High Performance Computing, Data, Analytics and Data Science. HiPC serves as a forum to present current work by researchers from around the world as well as highlight activities in Asia in the areas of high performance computing and data science. The meeting focuses on all aspects of high performance computing systems, and data science and analytics, and their scientific, engineering, and commercial applications.

Authors are invited to submit original unpublished research manuscripts that demonstrate current research in all areas of high performance computing, and data science and analytics, covering all traditional areas and emerging topics including from machine learning, big data analytics and blockchain. Each submission should be submitted to one of the tracks listed under the two broad themes of High Performance Computing and Data Science.

High Performance Computing tracks:

Algorithms: This track invites papers that describe original research on developing new parallel and distributed computing algorithms, and related advances. Examples of topics that are of interest include (but not limited to):
* New parallel and distributed algorithms and design techniques;
* Advances in enhancing algorithmic properties or providing guarantees (e.g., fault tolerance, resilience, concurrency, data locality, communication-avoiding);
* Classical and emerging computation models (e.g., parallel/distributed models, quantum computing, neuromorphic and other bioinspired models);
* Provably efficient parallel and distributed algorithms for advanced scientific computing and irregular applications (e.g., numerical linear algebra, graph algorithms, computational biology); and
* Algorithmic techniques for resource allocation and optimization (e.g., scheduling, load balancing, resource management);

Architectures: This track invites papers that describe original research on the design and evaluation of high performance computing architectures, and related advances. Examples of topics of interest include (but not limited to):
* Design and evaluation of high performance processing architectures (e.g., reconfigurable, system-on-chip, manycores, vector processors);
* Design and evaluation of networks for high performance computing platforms (e.g., interconnect topologies, network-on-chip);
* Design and evaluation of memory, cache and storage architectures (e.g., 3D, photonic, Processing-In-Memory, NVRAM, burst buffers, parallel I/O);
* Approaches to improve architectural properties (e.g., energy/power efficiency, reconfigurable, resilience/fault tolerance, security/privacy); and
* Emerging computational architectures (e.g., quantum computing, neuromorphic and other bioinspired architectures).

Applications: This track invites papers that describe original research on the design and implementation of scalable

applications for execution on parallel and distributed platforms, and related advances. Examples of topics of interest include (but not limited to):
* Design and implementation of shared and distributed memory parallel applications (e.g., scientific computing and industry applications, emerging applications in IoT and life sciences - biology, medicine, chemistry, etc.);
* Design and simulation methodologies for scaling applications on peta- and exascale platforms (e.g., co-design approaches, hardware/software co-design, heterogeneous and hybrid programming);
* Hardware acceleration of parallel applications (e.g., CPU/GPUs, multi-GPU clusters, FPGA, vector processors, manycore); and
* Design of application benchmarks for parallel and distributed platforms.

Systems Software: This track invites papers that describe original research on the design, implementation and evaluation of systems software for high performance computing platforms, and related advances. Examples of topics of interest include (but not limited to):
* Scalable systems and software architectures for high performance computing (e.g., middleware, operating systems, I/O services);
* Techniques to enhance parallel performance (e.g., compiler/runtime optimization, learning from application traces, profiling);
* Techniques to enhance parallel application development and productivity (e.g., Domain-Specific Languages, programming environments, performance/correctness checking and debugging);
* Techniques to deal with uncertainties, hardware/software resilience, and fault tolerance;
* Software for cloud, data center, and exascale platforms (e.g., middleware tools, schedulers, resource allocation, data migration, load balancing); and
* Software and programming paradigms for heterogeneous platforms (e.g., libraries for CPU/GPU, multi-GPU clusters, and other accelerator platforms);

Data Science tracks:

Scalable Algorithms and Analytics: This track invites papers that describe original research on developing scalable algorithms for data analysis at scale, and related advances. Examples of topics of interest include (but not limited to):
* New scalable algorithms for fundamental data analysis tasks (supervised, unsupervised learning, and pattern discovery);
* Scalable algorithms that are designed to address the characteristics of different data sources and settings (e.g., graphs, social networks, sequences, data streams);
* Scalable algorithms and techniques to reduce complexity of large-scale data (e.g., streaming, sublinear data structures, summarization, compressive analytics);
* Scalable algorithms that are designed to address requirements in different data-driven application domains (e.g., life sciences, business, agriculture); and
* Scalable algorithms that ensure the transparency and fairness of the analysis.

Scalable Systems and Software: This track invites papers that describe original research on developing scalable systems and software for handling data at scale, and related advances. Examples of topics of interest include (but not limited to):
* Design of scalable system software to support various applications (e.g., recommendation systems, web search, crowdsourcing applications, streaming applications)
* Design of scalable system software for various architectures (e.g., OpenPower, GPUs, FPGAs).
* Architectures and systems software to support various operations in large data frameworks (e.g., storage, retrieval, automated workflows, data organization, visualization, visual analytics, human-in-the-loop);
* Design and implementation of systems software for distributed data frameworks (e.g., distributed file system, virtualization, cloud services, resource optimization, scheduling); and
* Standards and protocols for enhancing various aspects of data analytics (e.g., open data standards, privacy preserving and secure schemes).

One or more best paper awards will be given for outstanding contributed papers.

IMPORTANT DATES
Abstract Submission: Friday, June 7, 2019
Paper Submission: Friday, June 14, 2019
Reviews for Rebuttals: Monday, July 29, 2019
Rebuttals due: Monday, August 5, 2019
Initial Submission Decision: Monday, August 19, 2019
Revisions Due: Friday, September 20, 2019
Author Notification: Monday, September 30, 2019
Camera Ready: Monday, October 14, 2019

Manuscript Guidelines
Submitted manuscripts should be structured as technical papers and may not exceed ten (10) single-spaced double-column pages using 10-point size font on 8.5x11 inch pages (IEEE conference style), including figures, tables, and references. See IEEE style templates at this page for details.

Journal Special Issue: Authors of selected high quality papers in HiPC 2019 will be invited to submit extended version of their papers for possible publication in a special issue of Journal of Parallel and Distributed Computing.

PROGRAM CHAIRS
Ananth Kalyanaraman, Washington State University, USA
George Karypis, University of Minnesota, USA

PROGRAM VICE-CHAIRS
HPC Tracks:
Algorithms: Bora Uçar, CNRS and École normale supérieure de Lyon, France
Applications: Alba Cristina M.A. de Melo, University of Brasilia, Brazil
Architecture: Smruti Ranjan Sarangi, Indian Institute of Technology Delhi, India
System Software: Sriram Krishnamoorthy, Pacific Northwest National Laboratory, USA
Data Science Tracks:
Scalable Algorithms and Analytics: Srinivasan Parthasarathy, Ohio State University, USA
Scalable Systems and Software: Gagan Agrawal, Ohio State University, USA

Contact Information
* High Performance Computing tracks:
Ananth Kalyanaraman, Washington State University, USA, ananth@wsu.edu
* Data Science tracks:
George Karypis, University of Minnesota, USA, karypis@umn.edu

Call for Submissions: ACM SIGDA Ph.D. Forum 2019

ACM SIGDA Ph.D. Forum
Las Vegas, NV, June 2019

The Ph.D. Forum at the Design Automation Conference is a poster session hosted by ACM SIGDA for Ph.D. students to present and discuss their dissertation research with people in the EDA community. It has become one of the premier forums for Ph.D. students in design automation to get feedback on their research and for industry to see academic work in progress: hundreds of people attended the last forums. Participation in the forum is competitive with acceptance rate of around 30%. Limited funds will be available for travel assistance, based on financial needs. The forum is open to all members of the design automation community and is free-of-charge. It is co-located with DAC to attract the large DAC audience, but DAC registration is not required in order to attend this event.

Eligibility
- Students with at least one published or accepted conference, symposium or journal paper.
- Students within 1-2 years of dissertation completion and students who have completed their dissertation during the 2018-2019 academic year.
- Dissertation topic must be relevant to the DAC community.
- Previous forum presenters are not eligible.
- Students who have presented previously at the DATE and ASP-DAC Ph.D. forums are eligible, but will be less likely to receive travel assistance.

Important Dates
Abstract Submission: April 8, 2019
Submission Link: https://easychair.org/conferences/?conf=daforum19
Notification Date: April 29, 2019
Forum Presentation Time: Tuesday, June 4. 7-9pm
Location: Design Automation Conference, Las Vegas, NV

Submission Requirements

A two-page PDF abstract of the dissertation (in two-column format, using 10-11 pt. fonts and single-spaced lines), including name, institution, advisor, contact information, estimated (or actual) graduation date, whether the work has been presented at ASP-DAC Ph.D. Forum or DATE Ph.D. Forum, as well as figures, and bibliography (if applicable). The two-page limit on the abstract will be strictly enforced: any material beyond the second page will be truncated before sending to the reviewers. Please include a description of the supporting paper, including the publication forum. A list of all papers authored or co-authored by the student, related to the dissertation topic and included in the two-page abstract, will strengthen the submission.

The submission should also include a published (or accepted) paper, in support of the submitted dissertation abstract. The paper must be related to the dissertation topic and the publication forum must have a valid ISBN number. It will be helpful, but is not required, to include your name and the publication forum on the first page of the paper. Papers on topics unrelated to the dissertation abstract or not yet accepted will not be considered during the review process.

Please Note:
- The abstract is the key part of your submission. Write the abstract for someone familiar with your technical area, but entirely unfamiliar with your work. Clearly indicate the motivation of your Ph.D. dissertation topic, the uniqueness of your approach, as well as the potential impact your approach may have on the topic.
- In the beginning of the abstract, please indicate to which track your submission belongs to.
- Proper spelling, grammar, and coherent organization are critical: remember that the two pages may be the only information about yourself and your PhD research available to the reviewers.
- All submissions must be made electronically.
- Please include the supporting paper with the abstract in one PDF file and submit the single file. There are many free utilities available online which can merge multiple PDF files into a single file if necessary.

Topics of Interest
- System-level Design, Synthesis and Optimization (including network-on-chip, system-on-chip and multi/many-core, HW/SW co-design, embedded software issues, modeling and simulation)
- Internet of Things (IoT)
- Autonomous Systems
- High Level Synthesis, Logic Level Synthesis
- Power and Reliability Analysis and Optimization (including power management from system level to circuit level, thermal management, process variability management)
- Timing Analysis, Circuit and Interconnect Simulation
- Physical Design and Manufacturability
- Signal Integrity and Design Reliability
- Verification, Testing, Pre- and Post-Silicon Validation, Failure Analysis
- Reconfigurable and Adaptive Systems
- Analog/Mixed Signals and RF
- Hardware Security
- Machine learning/AI
- Emerging Design, Technologies, and Computing Methods (carbon nanotubes, molecular electronics, MEMS, microfluidic system, biologically-inspired systems, quantum computing, etc.)

Contact Information
For questions not addressed on this page, please send e-mail to Dr. Hai Li:(hai.li@duke.edu) or Dr. Ogras (umit@asu.edu). Please include "DAC Ph.D Forum" in the subject line of your email.

Organizing Committee
Hai Li, University of Pittsburgh (Chair)
Umit Ogras, Arizona State University
Rasit Topaloglu, IBM
Yiyu Shi, University of Notre Dame (SIGDA Representative)

Call for Papers: ESWEEK 2019

EMBEDDED SYSTEMS WEEK
Call for Papers, Workshops, Tutorials, and Special Sessions
CASES * CODES+ISSS * EMSOFT * IoMT * Symposia * Workshops * Tutorials
New York City, USA, October 13 - 18, 2019
www.esweek.org

Embedded Systems Week (ESWEEK) is the premier event covering all aspects of embedded systems and software. By bringing together three leading conferences (CASES, CODES+ISSS, EMSOFT), a special IoMT Day, a symposium (NOCS), and hot-topic workshops and tutorials, ESWEEK presents attendee a wide range of topics unveiling the state of the art in embedded systems design and HW/SW architectures.

https://esweek.org/sites/default/files/ESWEEK2019_CfP_1.pdf

Registered attendees are entitled to attend sessions of all conferences CASES, CODES+ISSS, EMSOFT, and the IoMT Day. Symposia, workshops, and tutorials require separate registration.

Journal Track:
- Abstract Submission: April 5, 2019
- Full Paper Submission: April 12, 2019 (firm)
- Notification of Acceptance: July 10, 2019

Work-in-Progress Track:
- Paper Submission: June 7, 2019 (firm)
- Notification of Acceptance: July 10, 2019

Workshop Proposals: April 18, 2019
Tutorial Proposals: April 30, 2019
Special Session Proposals: April 30, 2019

Paper Process
ESWEEK 2019 continues a dual publication model comprising the Journal track and the Work-in-Progress (WiP) track. Journal track papers, which are full-length (10-page) papers describing mature work, will be published in the ACM Transactions on Embedded Computing Systems (TECS). The WiP track papers, which are short (2-page) papers representing not- yet-mature but promising research, will be published in the ESWEEK proceedings and will be listed as regular publications within the IEEE and/or ACM digital libraries. Authors of WiP papers have the opportunity to publish the extended form of their work in any conference or journal they prefer. Journal and WiP papers are mutually exclusive, i.e., a work can only be in submission in one of the two tracks. For more information, please refer to:
https://www.esweek.org/author-information

CASES: International Conference on Compilers, Architectures, and Synthesis for Embedded Systems
CASES is a premier forum where researchers, developers and practitioners exchange information on the latest advances in compilers and architectures for high-performance, low-power embedded systems. The conference has a long tradition of showcasing leading edge research in embedded processor, memory, interconnect, storage architectures and related compiler techniques targeting performance, power, predictability, security, reliability issues for traditional and emerging applications. In addition, we invite innovative papers that address design, synthesis, and optimization in heterogeneous and accelerator-rich architectures.
https://esweek.org/sites/default/files/2019-CASES-cfp_0.pdf

CASES Program Chairs:
Akash Kumar, Technical University of Dresden, DE
Partha Pande, Washington State University, US

CODES+ISSS: International Conference on Hardware/Software Codesign and System Synthesis
The International Conference on Hardware/Software Codesign and System Synthesis is the premier event in system-level design, modeling, analysis, and implementation of modern embedded and cyber-physical systems, from system-level specification and optimization down to system synthesis of multi-processor hardware/software implementations. The conference is a forum bringing together academic research and industrial practice for all aspects related to system-level and hardware/software co-design. High-quality original papers will be accepted for oral presentation followed by interactive poster sessions. https://esweek.org/sites/default/files/CODES%2BISSS-2019-CFP.pdf

CODES+ISSS Program Chairs:
Sudeep Pasricha, Colorado State University, US
Roman Lysecky, Arizona State University, US

EMSOFT: International Conference on Embedded Software
The ACM SIGBED International Conference on Embedded Software (EMSOFT) brings together researchers and developers from academia, industry, and government to advance the science, engineering, and technology of embedded software development. Since 2001, EMSOFT has been the premier venue for cutting-edge research in the design and

analysis of software that interacts with physical processes, with a long-standing tradition for results on cyber-physical systems, which compose computation, networking, and physical dynamics.
https://esweek.org/sites/default/files/EMSOFT2019_CfP_0.pdf

EMSOFT Program Chairs:
Sriram Sankaranarayanan, University of Colorado Boulder, US
Timothy Bourke, Inria Paris, FR

IoMT: Internet of Medical Things
The Internet of Medical Things (IoMT) paves the foundations for intelligent and reliable personalized precision medicine. Grounded in the mathematical and physical modeling of human anatomy and physiology, it offers accurate multiscale medical monitoring through smart sensing, enabling continuous diagnosis via on-fly communication with medical experts. It provides hyperspectral and hyperdimensional processing and restores health through patient-specific actuation. The IoMT special day provides a forum for academic and industry representatives from areas such as medical and bio-engineering and embedded systems to discuss innovative ideas and solutions for precise personalized medicine. Sub-missions to the IoMT day are via the three conferences. https://esweek.org/iomt/about

IoMT Chairs:
Insup Lee, University of Pennsylvania, US
Paul Bogdan, University of Southern California, US

Call for Workshop Proposals
ESWEEK 2019 will host several workshops on Oct. 17/18th. ESWEEK workshops are excellent opportunities to bring together researchers and practitioners from different communities to share their experiences in an interactive atmosphere. We invite you to submit workshop proposals on any topic related to the broad set of research, education, and application areas in embedded systems before the deadline of April 18, 2019.
https://esweek.org/sites/default/files/ESWEEK2019_CfP_1.pdf

Workshop Chair:
Laura Pozzi, USI Lugano, CH

Call for Tutorial Proposals
ESWEEK 2019 is looking for high-quality tutorials that will take place on Oct. 13th. Tutorials offer a unique opportunity where presenters can interact with attendees and attendees can gain in-depth knowledge on specific topics. Tutorials on all topics related to embedded system design, analysis and development are welcome and can be either half or full day, lecture style or hands on. We invite you to submit tutorial proposals before the deadline of April 30, 2019.

Call for Special Session Proposals
ESWEEK 2019 will host several special sessions. They should cover hot, contemporary topics that are complementary to regular sessions and can constitute individual presentations, panels or other formats. Participants of each accepted special session will have the opportunity to co-author an overview paper (maximum 10 pages) of the session, published in the ESWEEK proceedings. We invite you to submit special session proposals on any topic related to the broad areas of interest of the conference or beyond before the deadline of April 30, 2019.
https://esweek.org/sites/default/files/ESWEEK2019_CfP_1.pdf

Tutorials and Special Sessions Chair:
Andreas Gerstlauer, University of Texas Austin, US

Organization
ESWEEK 2019 General Chairs:
Petru Eles, Linkˆping University, SE
Tulika Mitra, National University of Singapore, SG (Vice General Chair)
Soonhoi Ha, Seoul National University, KR (Past Chair)

ESWEEK Local Arrangement Chairs:
Ramesh Karri, New York University, US
Siddarth Garg, New York University, US

Notice to Authors

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership. Circulation: 2,700

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