Comments from the Editors

Dear ACM/SIGDA member,

We are excited to present to you the March newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from upcoming conference and funding deadlines, hot research topics to news from our community.
Get involved and contact us if you want to contribute an article or announcement.

Happy reading!

Aida Todri-Sanial
Yu Wang
Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit http://www.acm.org/renew or call
between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or
1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org

"SIGDA E-News Editorial Board:"

'"Aida Todri-Sanial"', E-Newsletter co Editor-in-Chief

'"Yu Wang"', E-Newsletter co Editor-in-Chief

'"Xiang Chen"', E-Newsletter Associate Editor for SIGDA News column

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'"Pingqiang Zhou"', E-Newsletter Associate Editor for SIGDA Awards column

'"Yuan-Hao Chang"', E-Newsletter Associate Editor for SIGDA What is column

'"Debjit Sinha"', E-Newsletter Associate Editor for for SIGDA Paper submission deadline column

'"Pingqiang Zhou"', E-Newsletter Associate Editor for SIGDA Awards column

'"Jayita Das"', E-Newsletter Associate Editor for SIGDA Funding opportunities column

'"Qinru Qiu"', E-Newsletter Associate Editor for SIGDA Live column

'"Yiyu Shi"', E-Newsletter Associate Editor for SIGDA Live column

'"Rajsaktish Sankaranarayanan"', E-Newsletter Associate Editor for SIGDA Researcher spotlight column

SIGDA News

(1) "Intel Says FinFET-Based Embedded MRAM is Production-Ready"
[https://www.eetimes.com/document.asp?doc_id=1334343]

Intel gave further details on its technique for embedding spin-transfer torque (STT)-MRAM into devices using its 22-nm FinFET process, pronouncing the technology ready for high-volume manufacturing. Embedded MRAM is considered a promising technology for applications such as the internet of things (IoT) devices.

(2) "ARM Adds Helium Extension for Intelligent Edge Capability"
[https://www.eetimes.com/document.asp?doc_id=1334384]

Arm has introduced its Armv8.1-M architecture with new vector extension called Helium, to bring signal processing and machine learning (ML) capability for local decision making in edge devices based on its Cortex-M series processors.

(3) "Toshiba Claims Highest-Capacity NAND"

Toshiba Memory laid claim to the highest-capacity flash memory device, describing a 96-layer, 1.33-Tb 3D NAND chip in a paper at the International Solid-State Circuits Conference (ISSCC) here Tuesday.

(4) "Bad Photoresist Costs TSMC $550 Million"

TSMC said it scrapped a batch of wafers after using substandard photoresist at one of its largest fabs in southern Taiwan.

(5) "Samsung Claims First 512GB Embedded UFS"

Samsung Electronics said it has begun mass production of the first 512GB embedded Universal Flash Storage (eUFS) device.

(6) "Samsung, Toshiba Detail AI Chips"

Samsung described a new neural-network accelerator for smartphones that match blocks from rivals such as Huawei. Toshiba detailed one for self-driving cars that pulls ahead of competitors such as Intel's Mobileye at the International Solid-State Circuits Conference here.

(7) "NVM ReRAM Memory Cell Targets Edge AI"

Researchers at CEA-Leti and Stanford University have demonstrated a chip that integrates multiple-bit non-volatile memory (NVM) resistive RAM (ReRAM) with silicon computing units and new memory resiliency features that provide 2.3× the capacity of existing ReRAM. Target applications include energy-efficient, smart-sensor nodes to support artificial intelligence on the internet of things or edge AI.

(8) "Would a Huawei Boycott Unravel the Supply Chain?"

Huawei Technologies Co. — the controversial Chinese vendor of networking gear and smartphones — faces the real possibility that its telecom equipment will be banned from U.S. and European markets. If Huawei's sales suffer, its supply chain will feel the pain. Huawei became the world's third-largest semiconductor buyer in 2018, according to Gartner, and almost half its $100 billion revenue is derived from foreign markets.

(9) "Timeline: History of Huawei's Legal Woes in the U.S."

Practically since the moment it first established operations in the U.S., Huawei has found itself accused of intellectual property theft. In 2003, Cisco sued Huawei — then an upstart rival that competed with Cisco at the low end — for allegedly stealing and copying the router source code. Cisco agreed to settle the suit the following year — apparently without financial compensation — when Huawei agreed to make changes to its products in question.

(10) "Qualcomm Offers Robotics Building Blocks"

In a bid to make development of consumer, enterprise and industrial robots easier for manufacturers and developers, Qualcomm has launched its first integrated, comprehensive offering designed specifically for robotics.

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SIGDA Award

Best Paper Awards at ACM/SIGDA Sponsored Events

FPGA 2019: 27th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays,
http://www.isfpga.org/index.html

1. "HeteroCL: A Multi-Paradigm Programming Infrastructure for Software-Defined Reconfigurable Computing", by Yi-

Hsiang Lai (Cornell University), Yuze Chi (University of California, Los Angeles), Yuwei Hu (Cornell University), Jie Wang (University of California, Los Angeles), Cody Hao Yu (University of California, Los Angeles, Falcon Computing Solutions, Inc.), Yuan Zhou (Cornell University), Jason Cong (University of California, Los Angeles), Zhiru Zhang (Cornell University).

"What is" Column

What is Heterogeneous Computing?

Chia-Heng Tu, National Cheng Kung University

Heterogeneous computing refers to computer systems that are equipped with different kinds of processing units, such as central processing units (CPUs), graphics processing units (GPUs), and specialized hardware accelerators. By integrating with different processor technologies, heterogeneous computing systems are able to achieve ideal balances of performance and power consumption for given workloads. The heterogeneity concept is commonly found in today's computer systems ranging from smartphones [1] to supercomputers [2].

In order to unleash the computing power of heterogeneous hardware, application software should be implemented carefully to accelerate the executions of the compute-intensive codes on the best processing units. Usually, the specialized programming languages, such as CUDA [3] and OpenCL [4], are used by application programmers to orchestrate the computation accelerations. The CUDA programming language has been widely used to accelerate various applications, such as cryptomining, molecular simulations, and machine learning and analytics. OpenCL is the open standard alternative to CUDA. Compared with CUDA, which is specifically designed for the systems with NVIDIA processors, OpenCL is able to accelerate the computations on various types of processing units via the specialized OpenCL runtime libraries offered by the hardware venders.

As the OpenCL standard allows the presence of heterogeneous processing units on a system, it offers more APIs (compared with the CUDA APIs) to manage the hardware platform on a system, e.g., various types of processors and their memories. It is the responsibility of application programmers to use the low-level APIs to manage the underlying hardware platform and data buffers in order to achieve high performance. To ease the programming efforts, several works have been done to abstract the low-level details while improving the application performance on heterogeneous systems. For example, this is often done by adding a virtualization layer [5] between the application software and the OpenCL runtime libraries provided by the hardware vendors. The thin software layer virtualizes the multiple processing units as a single processor and the programmers can perform the task offloading to the virtualized big processor as normally done in an OpenCL program. The virtualization software is responsible for discovering the available processing units on the system and dispatching the offloading tasks to the proper processors to boost application performance without the programmers' intervention. The advantage of the virtualization software layer is that it simplifies the programming and optimization efforts.

The research works can be classified into two main groups. The first group focuses on distributing of the computation jobs onto the heterogeneous processing units on a system. For example, FluidCL [6] determines a good mapping of the sub-tasks of a computation job onto a CPU and a GPU, so that the application execution time is reduced by the CPU-GPU collaborative execution. MultiCL [7] developed the task scheduling feature in the customized OpenCL runtime library, which provides the best scheduling of offloading tasks across various OpenCL processing units.

The second group puts the emphasis on expanding the OpenCL support from a single machine node to multiple nodes within the computer cluster. SnuCL [8] is a notable example among the works in this group. SnuCL makes multiple processing units across different machine nodes appear as if they were local. Internally, SnuCL uses the popular communication library, MPI, to exchange data among machine nodes that contain OpenCL-enabled processing units. In addition, a centralized controller is responsible for scheduling and dispatching the offloading tasks to the distributed processing units. SnuCL is an open-source software and can be used to study the virtualization technique of heterogeneous processing units.

Regarding the design of a system with heterogeneous processing units, while there have been various works attempt to improve the application performance with the heterogeneous computing hardware, simply applying the above OpenCL software might not exhibit the best performance of the underlying hardware platform as the delivered performance is often hardware-dependent. For example, the application that runs well on a heterogeneous hardware might perform poorly on another hardware platform. It requires extra efforts during the system design stage, such as profiling/analyzing the application performance and tweaking the task scheduling algorithm, in order to find a good system configuration that

meets the system constraints.

References

[1] DeviceSpecifications – Mobile device specifications. https://www.devicespecifications.com/en

[2] TOP500 Supercomputer Sites. https://www.top500.org/

[3] CUDA Zone | NVIDIA Developer. https://developer.nvidia.com/cuda-zone

[4] OpenCL Overview - The Khronos Group Inc. https://www.khronos.org/opencl/

[5] Y.P. You, H.J. Wu, Y.N. Tsai, and Y.T. Chao. 2015. VirtCL: A Framework for OpenCL Device Abstraction and Management. SIGPLAN Not. 50, 8 (August 2015), 161–172.

[6] P. Pandit and R. Govindarajan. 2014. Fluidic Kernels: Cooperative Execution of OpenCL Programs on Multiple Heterogeneous Devices. In CGO. Article 273, 11 pages.

[7] A. M. Aji, A. J. Peña, P. Balaji, and W. Feng. 2016. MultiCL: Enabling automatic scheduling for task-parallel workloads in OpenCL. Parallel Comput. 58, C (October 2016), 37–55.

[8] J. Kim, S. Seo, J. Lee, J. Nah, G. Jo, and J. Lee. 2012. SnuCL: An OpenCL Framework for Heterogeneous CPU/GPU Clusters. In ICS. 341–352.

Paper Submission Deadlines

IWLS 2019 - International Workshop on Logic & Synthesis
Paper abstract submission: March 3, 2019
Full paper submission: March 10, 2019
Notification of acceptance: April 14, 2019
Final version due: May 12, 2019

ISVLSI'19 – IEEE Computer Society Annual Symposium on VLSI
Miami, FL
Deadline: March 3, 2019
Jul 15-17, 2019
http://www.isvlsi.org

ISLPED'19 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
Lausanne, Switzerland
Deadline: Mar 4, 2019 (Abstracts due: Feb 25, 2019)
Jul 29-31, 2019
http://www.islped.org

NATW'19 – IEEE North Atlantic Test Workshop
Essex, Vermont
Deadline: Mar 8, 2019
May 13-15, 2019
http://natw.ieee.org

AHS'19 - NASA/ESA Conference on Adaptive Hardware and Systems
Colchester, UK
Deadline: Mar 29, 2019
Jul 22-24, 2019
http://www.ahs-conf.org

ICCAD'19 – IEEE/ACM Int'l Conference on Computer-Aided Design
Westminster, CO
Deadline: Apr 8, 2019 (Abstracts due: Apr 1, 2019)
Nov 4-7, 2019
http://www.iccad.com

ESWEEK'19 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)
New York, NY
Deadline: Apr 12, 2019 (Abstracts due: Apr 5, 2019)
Oct 13-18, 2019
http://www.esweek.org

BodyNets'19 – Int'l Conference on Body Area Networks
Florence, Italy
Deadline: Apr 15, 2019
Oct 2-3, 2019
http://www.bodynets.org

VLSI-SoC'19 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Cuzco, Peru
Deadline: Apr 25, 2019 (Abstracts due: Apr 18, 2019)
Oct 6-9, 2019
www.vlsi-soc.com

IWBDA'19 - Int'l Workshop on Bio-Design Automation
Cambridge, England
Deadline: May 2019 (expected)
Jul 9-12, 2019
http://www.iwbdaconf.org/2019

Upcoming Symposia, Conferences and Workshops

ISQED'19 - Int'l Symposium on Quality Electronic Design
Santa Clara, CA
Mar 6-7, 2019
http://www.isqed.org

BSN'19 – IEEE Int'l Conference on Wearable and Implantable Body Sensor Networks
Chicago, IL
Mar 19-22, 2019
https://www.bhi-bsn-2019.org/bsn-2019

BHI'19 – IEEE Int'l Conference on Biomedical and Health Informatics
Chicago, IL
Mar 19-22, 2019
https://www.bhi-bsn-2019.org/bhi

TAU'19 – ACM Int'l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems
Monterey, CA
Mar 21-22, 2019
http://www.tauworkshop.com

DATE'19 - Design Automation and Test in Europe
Florence, Italy
Mar 25-29, 2019
http://www.date-conference.com

Quo Vadis, Logic Synthesis? - A Workshop at DATE'19
Florence, Italy
March 29, 2019
https://www.date-conference.com/conference/workshop-w09

ISPD'19 – ACM Int'l Symposium on Physical Design
San Francisco, CA
Apr 14-17, 2019

http://www.ispd.cc

HOST'19 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
Tysons Corner, VA
May 6-10, 2019
http://www.hostsymposium.org

GLSVLSI'19 – ACM Great Lakes Symposium on VLSI
Washington D.C., USA
May 9-11, 2019
http://www.glsvlsi.org

ASYNC'19 – IEEE Int'l Symposium on Asynchronous Circuits and Systems
Hirosaki, Japan
May 12-15, 2019
http://asyncsymposium.org

ISCAS'19 – IEEE Int'l Symposium on Circuits and Systems
Sapporo, Japan
May 26-29, 2019
http://iscas2019.org

DAC'19 – Design Automation Conference
Las Vegas, NV
Jun 2-6, 2019
http://www.dac.com/

ISCA'19 – Int'l Symposium on Computer Architecture
Phoenix, AZ
Jun 22-26, 2019
https://iscaconf.org

Funding Opportunities

'''North America'''

Keck Foundation
Deadline: various
http://www.wmkeck.org/grant-programs/research/

USDA Foundational Program
Deadline: various
http://www.grants.gov/web/grants/view-opportunity.html?oppId=283836

NATO: Science for Peace and Security
Deadline: Proposals accepted anytime; reviews take place February 1 and May 15
http://www.nato.int/cps/en/natolive/87260.htm

Air Force Research Laboratory: Research Collaboration Program (BAA-RQKM-2013-0005)
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=212295

Federal Aviation Administration Grants for Aviation Research (FAA-12-01)
Deadline: open to December 2019
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=134953

AFRL RD/RV University Cooperative Agreement
Deadline: open to Nov 23, 2020
http://www.grants.gov/web/grants/view-opportunity.html?oppId=280237

NASA Fellowship Programs
Deadline: Various

http://science.nasa.gov/researchers/sara/fellowship-programs/

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Students-Etudiants/PG-CS/index_eng.asp

itacs Accelerate PhD Fellowship: Ontario Business Grants Program
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/...

Collaborative Research and Development Grants
(including DND/NSERC Research Partnership Grants)
http://www.nserc-crsng.gc.ca/Professors-Professeurs/RPP-PP/CRD-RDC_eng.asp

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Professors-Professeurs/CFS-PCP/index_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Engage-Mobiliser_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Collaborate-Collaborer_eng.asp
Research and Development Funding for Business Innovation (Multiple Organizations)
Deadline: Various
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/

'''Europe'''

Horizon 2020
Deadline: Various
http://goo.gl/geBouC

German Academic Exchange Service (DAAD)
Deadline: Various
https://www.daad.org/scholarship

German Research Foundation (DFG)
Deadline: Various
http://www.dfg.de/en

Helmholtz Association
Deadline: Various
https://www.helmholtz.de/en

Leibniz Association
Deadline: Various
http://www.leibniz-gemeinschaft.de/en/home

Leopoldina
Deadline: Various
https://www.leopoldina.org/en/about-us

ax Planck Society
Deadline: Various
https://www.mpg.de/en

Swiss National Science Foundation
Deadline: Various
http://www.snf.ch/en/

'''Asia'''

Korea:

National Research Foundation of Korea
Deadline: Various

http://www.nrf.re.kr/nrf_eng_cms/show.jsp?show_no=90&check_no=89&c_relation=0&c_...

China:

National Natural Science Foundation of China
Deadline: Various
http://www.nsfc.gov.cn/publish/portal1/

Singapore:

National Research Foundation (NRF) Singapore
http://www.nrf.gov.sg
RIE 2020 plan
Deadline: Various
http://www.nrf.gov.sg/rie2020

India:

Ministry of Electronics and Information Technology
Deadline: Various
http://meity.gov.in/content/research-development

Department of Science and Technology (Nano Mission)
Deadline: Various
http://nanomission.gov.in/

University Grants Commission
Deadline: Various
http://www.ugc.ac.in/

Ministry of Education Academic Research Fund
Deadline: Various
https://www.olga.moe.gov.sg/default.aspx

Agency for Science Technology and Research (A*STAR) Science and Engineering Research Council (SERC)
Deadline: Various
https://www.a-star.edu.sg/Research/Funding-Opportunities/Grants-Sponsorship.aspx

Multiple Funding
Deadline: Various
http://www.computerscienceonline.org/cs-scholarships/

'''Oceania/Polynesia'''

Polynesian Cultural Center (Hawaii) - International Student Scholarship Program
For studying in BYU Hawaii
http://www.polynesia.com/students.html

New Zealand:

inistry of Business, Innovation and Employment
Deadline: Various
http://www.mbie.govt.nz/

Australia:

Premier's Research and Industry Fund
Deadline: Various
http://www.statedevelopment.sa.gov.au/science/premiers-research-and-industry-fun...

Australian Research Council
Deadline: Various
http://www.arc.gov.au

'''South America'''

Brazil:

Coordination for the Improvement of Higher Education Personnel (CAPES)
Deadline: Various
http://www.iie.org/programs/capes#.WAu2kJMrJPM

Ministry of Science, Technology, Innovation and Communications (CNPq)
Deadline: Various
http://www.cnpq.br/

'''Africa'''

Other scholarships for African Students (list of over 30 different scholarships)
Deadline: Various
http://www.afterschoolafrica.com/12264/list-annual-engineering-scholarships-afri...

Nigeria:

Bilateral Education Agreement (BEA) Awards (both Undergraduate and Post Graduate)
Deadline: Nomination interview - March'17
http://www.fsb.gov.ng/index.php/scholarship/menu-styles/bilateral-agreement

Federal Scholarship Board
Deadline: Various
http://www.fsb.gov.ng/index.php

Call for Papers: ASAP 2019

The 30th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2019)
Cornell Tech, New York, USA, July 15-17, 2019
Website: asap2019.csl.cornell.edu

The 30th IEEE International Conference on Application-specific Systems, Architectures and Processors 2019 will take place in Cornell Tech, New York, United States.

The history of the event traces back to the International Workshop on Systolic Arrays, organized in 1986 in Oxford, UK. It later developed into the International Conference on Application Specific Array Processors. With its current title, it was organized for the first time in Chicago, USA in 1996. Since then it has alternated between Europe and North-America. The conference will cover the theory and practice of application-specific systems, architectures, and processors. The 2019 conference will build upon traditional strengths in areas such as computer arithmetic, cryptography, compression, signal and image processing, network processing, reconfigurable computing, application-specific instruction-set processors, and hardware accelerators.

TOPICS OF INTEREST (but not limited to)
Big data analytics
Cloud computing infrastructures and acceleration
Heterogeneous computing in data centers
Accelerating data center workloads
FPGA-based deep learning
Embedded systems and domain-specific solutions (digital media, gaming, automotive applications)
Accelerating genomic computations
Acceleration of data analytics
Reconfigurable computing in the IoT era
Applications in finance
Wireless and mobile systems
Application-aware controller synthesis
Emerging technologies (optical models, 3D Interconnects, devices)

Reconfigurable accelerators
Hardware and software architectures for cyber-physical systems
Distributed systems & networks
Critical issues (security, energy efficiency, fault-tolerance)
Autonomous and semi-autonomous large-scale CPS
Autonomic computing systems
High-level design methods (hardware/software co-design, compilers)
Simulations and prototyping (performance analysis, verification tools)
Socio-technical systems

IMPORTANT DATES
Submission deadline: April 8, 2019
Decision notification: May 6, 2019
Camera ready version: May 29, 2019

SUBMISSION OF PAPERS
All manuscripts will be reviewed by at least three members of the program committee. Submissions should be a complete manuscript or, in special cases, may be a summary of relevant work. Manuscript for full paper should not exceed 8 single-space, double-column pages using 10-point size font on 8.5x11 inch pages (IEEE conference style) including references, figures, and tables. Manuscript for short papers should not exceed 4 single-space, double-column pages. Manuscripts for posters should not exceed 2 single-spaced, double-column pages. Submitted papers should not have appeared in or be under submission for a different workshop, conference or journal. It is also expected that all accepted papers (full, short or poster) will be presented at ASAP by one of the authors. Accepted full and short papers will be included in the proceedings and published in IEEE Xplore. Failure to present will result in the removal of the submission from the proceedings before publication. All papers must be submitted electronically in PDF format.

Submission website: https://asap2019.csl.cornell.edu/submission/

Call for Participation: Quo Vadis, Logic Synthesis?

Call for Participation: Quo Vadis, Logic Synthesis? - A Workshop at DATE'19
Florence, Italy
Friday, March 29
https://www.date-conference.com/conference/workshop-w09

In 1984, the book on Espresso by R. Brayton, G. Hachtel, C. McMullen, A. Sangiovanni-Vincentelli contributed the foundations of modern logic synthesis. The work done in leading academic and industrial research institutions triggered the first wave of modern logic design tools like Espresso, MIS, SIS, which then became the backbone of the industrial design chains for digital systems provided by the newborn Electronic Design Automation industry. After many research breakthroughs and industrial successes, it is time for an assessment of the perspectives of logic synthesis, both as a core technology in digital system design and an enabling technology in other domains (biological synthesis, machine learning for data analysis, etc.). Towards this goal, this workshop brings together a heterogeneous mix of speakers, from both academia and industry, spanning 35 years of research and development in logic synthesis.

PROGRAM
7:30-8:30 Registration desk opens
8:30-8:40 Introduction by Luca Carloni and Tiziano Villa
8:40-9:00 Thirty-five years after the Espresso book: a retrospective on logic synthesis, Tiziano Villa
9:00-10:00 Algorithmic foundations of logic synthesis - Part 1
- Extracting functions from Boolean relations, Jordi Cortadella
- Expressing flexibility in logic synthesis by Boolean relations, Anna Bernasconi
10:00-10:15 Coffee break
10:15-11:15 Algorithmic foundations of logic synthesis - Part 2
- Craig interpolation in logic synthesis applications, Jie-Hong Jiang
- SAT in logic synthesis, Mathias Soeken
11:15-12:15 Synthesis for emerging technologies
- XOR gates in emerging technologies, Valentina Ciriani
- Majority Logic Synthesis, Luca Amaru'
12:15-13:15 Lunch

13:15-14:15 Approximate synthesis
- Approximate logic synthesis for area and delay optimization, Weikang Qian
- Systematic approaches to approximate logic synthesis, Sherief Reda
14:15-15:15 High-level synthesis
- High-level synthesis: status and future trends, Andres Takach
- How high-level synthesis enables design for reusability of hardware accelerators, Luca Carloni
15:15-15:30 Coffee break
15:30-16:30 Logic synthesis and machine learning
- Automated synthesis of distributed/parallel computing through templates and inductive reasoning, Masahiro Fujita
- On the minimization of variables to represent sparse multi-valued input decision diagrams, Tsutomu Sasao
16:30-17:30 Logic synthesis and biological models
- Synthetic biology: application of logic synthesis to biological models, Gabriella Trucco
- Stochastic logic applied to DNA computing, Marc Riedel

FOR MORE INFORMATION: https://www.date-conference.com/conference/workshop-w09

WORKSHOP ORGANIZERS Luca Carloni (Columbia University) and Tiziano Villa (Universita' di Verona)

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Call for Papers: ISVLSI 2019

ISVLSI 2019
July 15-17, 2019
Miami, Florida

The IEEE Symposium on VLSI (ISVLSI) 2019 explores emerging trends, novel ideas and basic concepts covering a broad range of VLSI-related topics: from VLSI systems, tools and design methods at different abstraction levels, to bringing VLSI design and methods into new technologies such as nano and molecular devices and burgeoning application areas, such as hardware security, and artificial intelligence. Future design methodologies are also one of the key topics at the symposium, as well as new EDA tools to support them. Over three decades ISVLSI has been a unique forum promoting multidisciplinary research and new visionary approaches in the area of VLSI, bringing together leading scientists and researchers from academia and industry. The ISVLSI proceedings will be published by IEEE Computer Society Press. Selected papers from past editions have been subsequently published in special issues of top archival journals. ISVLSI has a good reputation of bringing together well-known international scientists as invited speaks. ISVLSI 2019 will continue the momentum and carry forward these well-established trends for further growth of the symposium.

Contributions are sought in, but not limited to, the Following Tracks
1) Circuits, Reliability, and Fault-Tolerance (CRT)
2) Computer-Aided Design and Verification (CAD)
3) Digital Circuits and FPGA based Designs (DCF)
4) Emerging and Post-CMOS Technologies (EPT)
5) System Design and Security (SDS)
6) VLSI for Applied and Future Computing (AFC)

Paper Submission: Authors are invited to submit full-length (6 pages maximum), original, unpublished papers along with an abstract of at most 200 words. To enable blind review, the author list should be omitted from the main document. Papers violating length and blind-review criteria would be withdrawn from the review process. Previously published papers or papers currently under review for other conferences/journals should not be submitted and will not be considered for publication.

Paper Submission Site: https://easychair.org/conferences/?conf=isvlsi2019
Important Dates:
Paper Submission Deadline: March 3, 2019
Acceptance Notification: April 21, 2019
Submission of Final Version: May 12, 2019

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Call for Papers: NOCS 2019

13th IEEE/ACM International Symposium on Networks-on-Chip
October 17-18, 2019, New York, USA (Co-located with Embedded Systems Week 2019)
https://www.engr.colostate.edu/nocs2019/

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to interdisciplinary research on on-chip, package-scale, chip-to-chip, and datacenter rack-scale communication technology, architecture, design methods, applications and systems. NOCS brings together scientists and engineers working on network-on-chip (NoC) innovations and applications from inter-related research communities, including discrete optimization and algorithms, computer architecture, networking, circuits and systems, packaging, embedded systems, and design automation. Topics of interest include, but are not limited to:

NoC Architecture and Implementation
- Network architecture (topology, routing, arbitration)
- Timing, synchronous/asynchronous communication
- NoC reliability issues and solutions
- Security issues and solutions in NoC architectures
- Power/thermal issues at NoC un-core and system-level
- Network interface issues and solutions
- Signaling and circuit design for NoC links and routers

Communication Analysis, Optimization, & Verification
- NoC performance analysis and Quality of Service
- Modeling, simulation, and synthesis of NoC
- Verification, debug and test of NoC
- NoC design and simulation methodologies and tools
- Benchmarks, experiences on NoC-based hardware
- Communication-efficient algorithms
- Communication workload characterization & evaluation

Novel NoC Technologies
- Optical, wireless, CNT, and other emerging technologies
- NoC for 2.5D and 3D packages
- Package-specific NoC design
- Network coding and compression solutions
- Approximate computing for NoC and NoC-based systems

NoC for Intelligent Physical Systems
- NoC design for Deep Learning
- Mapping of existing and emerging applications onto NoC
- NoC case studies, application-specific NoC design
- NoC for FPGA, structured ASIC, CMP and MPSoC
- NoC designs for heterogeneous systems
- NoC for CPU-GPU and data-center-on-a-chip (DCoC)
- Scalable modeling of NoC
- Machine learning for NoC and NoC-based Systems

NoC at the Un-Core and System-level
- Design of memory subsystem (un-core) including memory controllers, caches, cache coherence protocols in NoC
- NoC for new memory/storage technologies
- NoC support for processing-in-memory
- OS support for NoC
- Programming models for NoCs
- Interactions between large-scale systems (datacenter, edge and fog computing) and NoC-based building blocks

Inter/Intra-Chip and Rack-Scale Network
- Unified inter/intra-chip networks
- Hybrid chip-scale and datacenter rack-scale networks
- All aspects of inter-chip and rack-scale network design

Electronic paper submission requires a full paper, up to 8 double-column ACM (sigconf) format pages, including figures and references. The program committee will use a double-blind review process to evaluate papers based on scientific merit, innovation, relevance, and presentation. Submitted papers must describe original work that has not been published before or is under review by another conference or journal at the same time. Each submission will be checked for any

significant similarity to previously published works or for simultaneous submission to other archival venues, and such papers will be rejected. Proposals for special sessions and demos are invited. Paper submissions and demo proposals by industry researchers or engineers to share their experiences and perspectives are also welcome. A percentage of accepted papers will be recommended for publication in an IEEE journal after revision according to the reviewersí comments. Please find the detailed submission instructions for paper submission, special session, and demo proposals at the submission webpage.

Important Dates (Anywhere on Earth)
Abstract registration: May 10, 2019
Full paper submission: May 17, 2019
Notification of acceptance: July 8, 2019
Final version due: July 22, 2019

General Chairs
Paul Bogdan (University of Southern California)
Cristina Silvano (Politecnico di Milano)

Technical Program Chairs
Sudeep Pasricha (Colorado State University)
Ajay Joshi (Boston University)

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2019 Low-Power Image Recognition Challenge

The 2019 Low-Power Image Recognition Challenge will be held in June, co-located with CVPR. The workshop will include invited speakers, announcements of the winners of the online competition, onsite competition, and presentations of "Grand Challenge in Low-Power Computer Vision". More details are available at
https://rebootingcomputing.ieee.org/lpirc

2019 Low-Power Imaging Recognition Challenge (LPIRC 2019) and Grand Challenge in Low-Power Computer Vision

This workshop will extend the past the success in the past four years identifying the best vision solutions that can simultaneously achieve high accuracy in computer vision and energy efficiency. Since the first competition held in 2015, the winners' solutions have improved 24 times in the ratio of accuracy divided by energy.

LPIRC 2019 will continue the online + onsite options for participants. One online track with pre-selected hardware allows participants to submit their solutions multiple times without the need of traveling. One onsite track allows participants to bring their systems to CVPR.

Online Track (objection detection): Tensorflow Model. Submission dates: 2019/05/15 - 2019/06/10
Onsite Track (objection detection): No restriction. Bring your system to CVPR.
For the onsite track, Xilinx Ultra96 + PYNQ framework http://www.pynq.io/community.html is an option available to participants. Xilinx will provide support and possible hardware donation. People interested in this opportunity may contact Naveen Purushotham (npurusho@xilinx.com) for more details.

All participants must register before 2019/05/15.

To win a prize in 2019 LPIRC, a solution must be better than the state of the art. Please notice that this is a new requirement in 2019. The requirement in each track is shown below. If a solution's score is below the number, it cannot win. If a solution's score is better, it still has to beat the other solutions submitted to 2019 LPIRC.

Call for Papers: Grand Challenge in Low-Power Computer Vision

Competitions are widely adopted in academia, industry, and government to propel technologies forward. Well-known competitions include the DARPA Autonomous Vehicle Challenge and the Space X prize. The competitions have been attributed as the accelerators of making significant progress in the technologies. This workshop solicits papers that describe future competition of low-power computer vision. Authors are encouraged to think boldly, imagining "Grand Challenge" or "X Prize" type of competitions. The paper should describe one (or several) competitions that are (1) easy to understand, (2) easy to evaluate success objectively, (3) possible but at least 5 years beyond today's technologies.

Authors are encouraged to discuss the following issues in their papers:

Description of the data (e.g., image, video, with or without caption)
Is any existing dataset used? If so, is the dataset sufficient or additional improvements are needed?
Methods to acquire the data
Description about copyright and privacy (if applicable)
Methods to annotate the data (if applicable, for getting the ground truth)
Methods for scoring
Infrastructure for scoring (if applicable, for example online grading server or harness)
Constraints of hardware (if applicable, for example weight, size)
Minimum or maximum requirements (e.g., accuracy, energy. execution time)
Differences from existing competitions
All submissions must be in PDF format. Submissions have no page limits. Please use the CVPR 2019 submission style. Several selected papers will be presented in the LPIRC workshop in CVPR 2019. The accepted papers will be posted on this website and will not be included in the CVPR proceeding.

Important Dates:

Paper submission: 2019/04/30 (This is a hard deadline and will not be extended). Submission will be open on 2019/04/15. Please check this page for additional information.
Acceptance notification: 2019/05/20
Presentation: LPIRC Workshop at CVPR

Call for Distinguished Lecturers

The IEEE Council on Electronic Design Automation (CEDA) invites nominations for CEDA Distinguished Lecturers (DLs). The DL Program is an outreach program of CEDA that brings distinguished speakers from academia and industry to give presentations to CEDA chapters, events, and industries in a variety of venues and formats. The DLs are selected and announced in April after approval by the CEDA EC. DEADLINE Mach 8, 2019

Nominees must meet the following criteria:
- The DL nominee must be nominated by a CEDA member who does not have conflict with the selection process. No self-nomination is allowed.
- If you are looking for a nominator we encourage you to contact the chair of your corresponding CEDA Local Chapter.
- The DL nominee must be a well-recognized expert in his/her field because of his/her research, teaching, service activities and an inspiring speaker.

Duties:
The Distinguished Lecturers will start their two-year term in April. Each Lecturer should submit up to three lecture topics in his/her field of expertise that will be posted on the CEDA Website. The Distinguished Lectures should be readily available to travel within his/her geographical area upon contact by the Chapters or appropriate organizations. Reasonable travel expenses will be paid by the Distinguished Lecturers Program, and it is encouraged the sharing of travel expenses with other Organizational Units (Societies, Councils, etc.) of IEEE for joint activities. In addition, the maximum expenses limit allowed for each for a DLP lecture include 1500 USD for intra-continental talks and a total of 2500 USD for inter-continental talks. Moreover, IEEE CEDA can only cover Economy Fare flights. Please return completed nomination form to the CEDA DLP Manager, Tsung-Yi Ho (tyho@cs.nthu.edu.tw).

Call for Papers: IWLS 2019

The International Workshop on Logic & Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits and systems. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop encourages early dissemination of ideas and results. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

Topics of interest include, but are not limited to hardware synthesis and optimization; software synthesis; hardware/software co-synthesis; power and timing analysis; testing, validation and verification; synthesis for reconfigurable architectures; hardware compilation for domain-specific languages; and design experiences. Submissions on modeling, analysis and synthesis for emerging technologies and platforms are particularly encouraged.

Important Dates
Paper abstract submission: March 3, 2019
Full paper submission: March 10, 2019
Notification of acceptance: April 14, 2019
Final version due: May 12, 2019

Paper submission
Only complete papers with original and previously unpublished material are permitted. Submissions must be no longer than 8 pages, double column, 10-point font. Accepted papers are distributed only to IWLS participants.

The submission system is available at http://www.iwls.org

Programming Contest
The IWLS 2019 edition will also have a programming contest. More information will be available at http://www.iwls.org.

Contact
General Chair
Soeken Mathias
École polytechnique fédérale de Lausanne, Switzerland
mathias.soeken@epfl.ch

Program chair & contest chair
Luca Amaru
Synopsys, USA
luca.amaru@synopsys.com

Special session chair
Jody Matos
Silvaco, USA
jody.matos@silvaco.com

Finance chair
Pierre-Emmanuel Gaillardon
University of Utah, USA
pierre-emmanuel.gaillardon@utah.edu

Proceedings Chair
Zhufei Chu
Ningbo University, China
chuzhufei@nbu.edu.cn

Publicity chair
Vinicius Callegaro
Mentor, a Siemens Business
vinicius_callegaro@mentor.com

Program Committee
L. Amaru Synopsys, USA

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Call for Nominations: JETC Editor-in-Chief

ACM Journal on Emerging Technologies in Computing (JETC)
The term of the current Editor-in-Chief (EiC) of the ACM Journal on Emerging Technologies in Computing (JETC) (JETC) is coming to an end, and the ACM Publications Board has set up a nominating committee to assist the Board in selecting the next EiC.
Nominations, including self-nominations, are invited for a three-year term as JETC EiC, beginning on June 15, 2019. The EiC appointment may be renewed at most one time. This is an entirely voluntary position, but ACM will provide appropriate administrative support.
The EiC is responsible for maintaining the highest editorial quality, for setting technical direction of the papers published in JETC, and for maintaining a reasonable pipeline of articles for publication. He/she has final say on acceptance of papers, size of the Editorial Board, and appointment of Associate Editors. The EiC is expected to adhere to the commitments expressed in the policy on Rights and Responsibilities in ACM Publishing. For more information about the role of the EiC, see ACM's Evaluation Criteria for Editors-in-Chief.
Nominations should include a vita along with a brief statement of why the nominee should be considered. Self-nominations are encouraged, and should include a statement of the candidate's vision for the future development of JETC. The deadline for submitting nominations is March 31, 2019, although nominations will continue to be accepted until the position is filled.
Please send all nominations to the nominating committee chair, Partha Pande (pande@wsu.edu).
The search committee members are:
• Partha Pande (Washington State University), Chair
• Krishnendu Chakrabarty (Duke University)
• Jörg Henkel (Karlsruhe Institute of Technology)
• Tsung-Yi Ho (National Tsing Hua University)
• Chaitali Chakrabarti (Arizona State University)
• Josh Tenenberg (University of Washington), A&S Committee Liaison

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Call for Papers: ICESS 2019

The 15th IEEE International Conference on Embedded Software and Systems (ICESS 2019)
Las Vegas Convention Center, Nevada, United States, June 2-3, 2019
Co-located with DAC 2019 (participants can access DAC Keynotes, Exhibits and Receptions)
http://lcs.ios.ac.cn/icess2019/

Overview: The advancement of embedded software and systems, such as intelligent vehicles, industrial robots, wearable devices, and Internet-of-Things, has great societal and economic impacts. It is of utmost importance to ensure the safety, efficiency, and security of their design and implementation. The IEEE International Conference on Embedded Software and Systems (ICESS) is a global forum for researchers and developers from academia, industry, and government to present and discuss emerging ideas and trends in embedded software and systems. The conference has a broad scope covering the design, implementation, optimization, and validation of embedded software and systems in various domains, with recent focus on cyber-physical systems, Internet-of-Things, embedded security, and autonomous software systems.

ICESS 2019 is the 15th IEEE International Conference on Embedded Software and Systems. The conference will be collocated with the Design Automation Conference (DAC) 2019 in Las Vegas, Nevada, USA. Participants can access DAC exhibits, keynotes, and receptions. It is the next event of a series of highly successful international conferences, held in recent years as ICESS 2017 (Sydney, Australia), ICESS 2016 (Sichuan, China), ICESS 2015 (New York, USA), ICESS 2014 (Paris, France), ICESS 2013 (Sydney, Australia), ICESS 2012 (Liverpool, UK), ICESS 2011 (Changsha, China), and ICESS 2010 (Bradford, UK).

All accepted papers are expected to be included in IEEE Xplore and indexed by EI. Selected papers, after further revisions, will be considered for publication in a special issue of the Elsevier Journal of Systems Architecture. ICESS 2019 will be sponsored by the IEEE, the IEEE Computer Society, the IEEE Technical Committee on Scalable Computing (TCSC), and the IEEE Technical Committee on Cyber-Physical Systems (TCCPS).

Important Dates
Paper Submission: March 12, 2019, 11:59 p.m. Anywhere on Earth
Notification: April 2, 2019
Camera-ready version: April 30, 2019
Conference: June 2-3, 2019

Notice to Authors

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership. Circulation: 2,700