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The resource for EDA Professionals

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Comments from the Editors

Dear ACM/SIGDA member,

We are excited to present to you the February newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from upcoming conference and funding deadlines, hot research topics to news from our community.
Get involved and contact us if you want to contribute an article or announcement.

Happy reading!

Aida Todri-Sanial
Yu Wang
Editors-in-Chief, SIGDA E-News

To renew your ACM SIGDA membership, please visit http://www.acm.org/renew or call between the hours of 8:30am to 4:30pm EST at +1-212-626-0500 (Global), or 1-800-342-6626 (US and Canada). For any questions, contact acmhelp@acm.org

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'"Rajsaktish Sankaranarayanan"', E-Newsletter Associate Editor for SIGDA Researcher spotlight column

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SIGDA News

(1) "U.S. Lawmakers Propose Ban on Chip Sales to Huawei, ZTE"
[https://www.eetimes.com/document.asp?doc_id=1334216]

A bipartisan group of U.S. lawmakers has introduced legislation which would ban the export of U.S. chips and other components to Chinese telecommunications companies Huawei and ZTE for violating U.S. export control laws.

(2) "Israel Approves $185 Million Grant for Intel Fab"
[https://www.eetimes.com/document.asp?doc_id=1334136]

The Israeli parliamentary finance committee approved a $185 million grant to Intel in return for meeting job creation targets and local contract guarantees.

(3) "IBM, Samsung Lead Patent Rankings"
[https://www.eetimes.com/document.asp?doc_id=1334151]

IBM led in U.S. utility patent awards again in 2018, a year that saw a dip in overall awards. But a new ranking of global patent holders showed that Samsung leads the pack by far.

(4) "Intel Tips 'Ice Lake' 10nm PC Processor"
[https://www.eetimes.com/document.asp?doc_id=1334158]

Intel uncorked a small geyser of news at the Consumer Electronics Show, including word of the company's first volume 10nm PC processor — which will be called Ice Lake — discussion of a new hybrid CPU architecture that combines different types of CPU cores in a single system on a chip (SOC) and the introduction of a new chip aimed at inference-based AI applications.

(5) "Nvidia Unveils Mid-Range Turing GPU"
[https://www.eetimes.com/document.asp?doc_id=1334150]

Nvidia rolled out its first mid-range GPU based on the company's Turing GPU architecture, promising to make available to more PC gamers real-time ray-tracing graphics capability in a card that retails for just $349.

(6) "Huawei Rolls 7-nm Arm Server CPU"
[https://www.eetimes.com/document.asp?doc_id=1334149]

Huawei announced a 7-nm Arm-based server CPU that it claims outperforms rivals and servers using it. The Kunpeng 920 shows the increasing sophistication of China's largest system vendor and chip designer at a time when it's at the center of heated trade tensions with the U.S.

(7) "AT&T Preps Edge Cloud Nets"
[https://www.eetimes.com/document.asp?doc_id=1334217]

An open-source group aims to release by April 30 code for carrier edge networks initially driven by AT&T and a team of its vendors. If successful, the Akraino Edge Stack software will someday power "cookie-cutter" deployments of "thousands and tens of thousands … of baby clouds," said an AT&T executive.

(8) "DRAM Prices Forecast to Crash in Q1"
[https://www.eetimes.com/document.asp?doc_id=1334222]

Contract prices for DRAM chips are projected to fall by nearly 20% in the first quarter, as high inventories and weak demand couple with a downbeat mid- to the long-term economic outlook, according to market research firm TrendForce's DRAMeXchange service.

(9) "'Excitons' Show Potential for Low-Power Quantum Computing"
[https://www.eetimes.com/document.asp?doc_id=1334205]

A laboratory in Switzerland has found a way of using a laser to change and regulate the polarization, wavelength and intensity of light in "excitons" in 2D materials, creating the potential for a new generation of transistors with less energy loss and heat dissipation, opening up the potential for low-power quantum computing.

(10) "Quantum Dots to Shrink MicroLED Display Pixels"
[https://www.eetimes.com/document.asp?doc_id=1334167]

Nanoco Technologies and Plessey Semiconductors have partnered to shrink the pixel size of monolithic microLED displays using Nanoco's cadmium-free quantum-dot (CFQD quantum dots) semiconductor nanoparticle technology.

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SIGDA Local Chapter News

The 3rd Future Chips Forum has been successfully held on December 10-11, 2018, in Reception Hall of the Main Building, Tsinghua University. The Future Chips forum is an annual event held by Beijing Innovation Center for Future Chips and the Institute of Microelectronics, Tsinghua University. The forum aims to provide an opportunity for experts from academia and industry to exchange new ideas and integrate expertise.

The Main Theme of this year's forum is "Reconfigurable Computing in a New Golden Age". This year, over 30 prominent scientists from all over the world joined the forum at Tsinghua University to share the latest trends and research development about reconfigurable computing. The forum committee includes Prof. Zheng You, Prof. Shaojun Wei, Prof. Sharon X. Hu, Prof. Yuan Xie, Prof. Yiran Chen, Prof. Huaqiang Wu, and Prof. Shouyi Yin. Please refer to the

following link for more details: http://www.icfc.tsinghua.edu.cn/futurechips2018/index.html

This Future Chips Forum is co-located with the Workshop on Device to Application Benchmarking, which is held on December 9, 2018 at Room 312, FIT Building, Tsinghua University. The workshop brings together industrial experts and academic researchers to explore future prospects particularly related to benchmarking for technology driven machine learning accelerators and compute-in-memory hardware infrastructure. It is co-sponsored by University of Notre Dame (U.S.) and Tsinghua University (China). Please refer to the following link for more details: http://www.icfc.tsinghua.edu.cn/futurechips2018/workshop.html

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SIGDA Award

Best Paper Awards at ACM/SIGDA Sponsored Events

ASP-DAC 2019: 24th Asia and South Pacific Design Automation Conference,
http://www.aspdac.com/aspdac2019/awards/

1. "GraphSAR: A Sparsity-Aware Processing-in-Memory Architecture for Large-Scale Graph Processing on ReRAMs", by Guohao Dai (Tsinghua Univ., China), Tianhao Huang (Massachusetts Inst. of Tech., U.S.A.), Yu Wang, Huazhong Yang (Tsinghua Univ., China) and John Wawrzynek (Univ. of California, Berkeley, U.S.A.).

2. "Energy-Efficient, Low-Latency Realization of Neural Networks through Boolean Logic Minimization", by Mahdi Nazemi, Ghasem Pasandi and Massoud Pedram (Univ. of Southern California, U.S.A.).

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Researcher Spotlight

Hello readers,

This edition of Researcher spotlight introduces Prof. Riadul Islam with the Department of Electrical and Computer Engineering at the University of Michigan-Dearborn (UMD). He received his Ph.D. in Computer Engineering from the University of California Santa Cruz. He leads the UMD VLSI-SoC group. He is a recipient of sponsored research grant from NASA and Michigan Space Grant Consortium (MSGC), Richard Newton Young Fellow awardee and a UC Santa Cruz Inventor Recognition Program (IRP) awardee. Some excerpts from a recent conversation.

'''1. Can you share with us some of the research areas you are interested in?'''

My primary research interests are low-power high-performance microprocessor design and IC synthesis tool development considering low-cost, robust, error-free hardware design. In addition, I have a deep interest in cosmic radiation-induced soft error-hardened circuits and system design.

'''2. Hybrid-mode Clock Distribution Network combining voltage-mode and current-mode clocking schemes offers power savings and reduces jitter-induced skew. What challenges did you face in this work and foresee in adoption using industry standard tool-flows?
'''

Clock skew and jitter are a primary hurdle for today's processor speed limits in conjunction with the total power budget and are our prime motivation for this work. The key challenges of this work were: (i) the conventional synthesis tools not supporting hybrid-mode clocking, (ii) designing low-power current-to-voltage converters, and (iii) identifying an optimal number of sinks/cluster and receiver placement locations.
In this work, we proposed the first hybrid-mode clock synthesis flow. We can easily apply this methodology in the existing industry standard tool-flow with slight modification. For example, the local clock network can still utilize the existing voltage-mode (VM) clock tree synthesis (CTS), while the global clock network can be current-mode to reduce jitter-induced delay variation.

'''3. Negative Capacitance Field Effect Transistors (NCFET) when deployed in Clock Distribution Network delivers

power savings and robustness to process variation. Based on your findings from this, if expanded to sequential and logic implementation (NCFET) too, do you expect similar savings or a change in CDN performance and power? Why?
'''

In our "Negative Capacitance Clock Distribution" work, we leverage the better current driving capability of the NCFET devices compared to the conventional bulk-CMOS devices. As a result, we use up to 20% fewer clock buffers compared to the existing synthesized clocking scheme, consequently saving up to 73% clock network power compared to the industry standard clocking schemes.
In this work, we identified that the direct use of NCFET devices in a conventional CTS tool can increase the crosstalk-induced delay. However, in the proposed buffer insertion method with increased wire segment (i.e., capacitance), the delay variation is 21% and 49% lower than the conventional CMOS- and NCFET-based designs.

'''4. Optimizing design effort and design implementation has a direct effect on product development costs in industry. Can you talk more on your Machine learning / Deep learning projects in this space?
'''

According to IRDS (successor to ITRS), human engineering cost is considered a major component of IC design cost. On the other hand, DARPA's Intelligent Design of Electronic Assets (IDEA) program is looking for a "no human in the loop," 24-hour design framework that would enable even non-experts to design complex ICs. My VLSI-SOC group at the University of Michigan-Dearborn is applying machine learning (ML) algorithms to reduce the existing tool noises. We are very excited to see our initial results. However, it very early to talk more about this project. In addition, we need national and industrial funding to make this project successful. We are planning to disseminate our results through upcoming conference and journal publications.

'''5. Can you help explain what is a double node upset in the context of memory systems and your research efforts in this space to help mitigate the impact?
'''

Sure, I will be happy to talk about the double node upset in the context of memory systems. A SET is a voltage transient caused by high-energy neutrons generated from cosmic radiation and by alpha particles from packaging materials, which interact with silicon and generate unwanted charge. If the amplitude and duration of the SET is large, it can be captured in a latch, resulting in a data upset, commonly known as an SEU or soft error. However, at today's leading process node, the charge produced by a particle strike can be collected by multiple nodes, resulting in multiple-node logic value corruption, also referred to as single event double-node upset (SEDU). In our recent journal article entitled "Low-Power Highly Reliable SET-Induced Dual-Node Upset Hardened Latch and Flip-Flop," we detailed a novel 16-transistor (16T) SEDU-hardened storage cell and the use of this cell in latch design. In addition, we proposed the first SEDU-hardened flip-flop. The proposed latch exhibits 25% lower power consumption, is 81% faster, and also shows 86% lower power-delay product compared to the existing SEDU-hardened latches. The proposed SEDU-hardened flip-flop is 29% faster, consumes 50% lower dynamic power and 25% lower static power, has 45% lower setup time, and uses 27% lower area compared to the existing partial SEDU-hardened flip-flop.

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"What is" Column

What is Ferroelectric FET?

by Xueqing Li, Tsinghua University

Ferroelectric Field-Effect Transistor (FeFET) is a kind of field-effect transistor (FET) that uses ferroelectric materials to enhance certain features, such as low-voltage operation and nonvolatile data storage capabilities [1]. From the perspective of device structure, an FeFET is essentially a metal-oxide-semiconductor FET (MOSFET) with an extra sandwiched ferroelectric gate insulator, such as hafnium dioxide doped with Zirconium which is extensively used today in high-$\varkappa$ dielectric transistor gate stacks, making it compatible with the commercial complementary metal-oxide-semiconductor (CMOS) process [2]. Between the internal MOSFET gate and the ferroelectric layer, an extra metal layer may be adopted. While FeFETs had been proposed decades ago [3], the proposal of highly-CMOS compatible FeFETs was experimentally reported recently. FeFETs are also reported to exhibit beyond-CMOS logic power efficiency and low-power nonvolatile memory (NVM) features [4][5].

One intriguing FeFET feature is the potential to make better switches in modern digital processors [4][5]. The

performance and energy efficiency of a transistor switch may lead to immediate and significant improvement at almost every level of electronics design. The story behind this fact is that, since the end of Dennard Scaling [6], the CMOS technology has been unable to continue with its supply voltage reduction, causing the bottleneck of further power consumption improvement at the device level. This is intrinsically due to the Boltzmann distribution of electrons in a MOSFET that limits the minimum switching slope to 60 mV per decade. Aggressive reduction of the supply voltage may lead to either unsatisfactory operating speed due to low ON-state current driving capability, or unwanted high leakage power consumption due to high OFF-state quiescent current.

FeFET devices, on the other hand, have been reported to exhibit an effect of negative capacitance, which consequently led to a type of FeFET known as NCFET. When the ferroelectric material is biased with negative capacitance and is connected in series with the positive MOSFET gate capacitance, a small voltage change at the external NCFET gate could be passively amplified at the internal MOSFET gate, leading to sub-60 mV per decade switching. Recently, there have been some debates over whether such voltage amplification could be caused by quasi-static negative capacitance in the famous S-shape polarization-electric field curves, and further, whether the power consumption could be reduced if only dynamic negative capacitance exists [7][8].

Another promising FeFET feature is the embedded NVM behavior [4][5]. The frequently mentioned story behind the importance of embedded NVM is the overwhelming concern of the “memory wall” between the computing unit and the memory storage of the von Neumann architecture. Embedding memory reduces the energy and latency of memory access. Making the memory nonvolatile also enables the mitigation of static standby leakage power. While there are quite a few emerging embedded NVM options such as STT-MRAM, PCRAM, RRAM, FeRAM, and possibly their 3D versions of a vertical-dimension stack, it is critical to have one with high density, logic compatibility, fast and low-power read and write access, and high-enough endurance [5].

The FeFET-based NVM solution becomes promising at the array level with a few features [5][9]: (i) high density with the one-transistor per cell configuration; (ii) intrinsic logic compatibility with the use of doped HfO2; (iii) ~10ns write speed with no static write current; (iv) similar read speed and power to SRAM; (v) medium endurance up to 1012. Efforts in using FeFETs for NVM and nonvolatile computing have been seen in both device and circuit architectures [4].

Another key concept of memory-centric computing approach to solving the “memory wall” problem calls for computing in-memory (CiM) or processing-in-memory (PIM). In this perspective, the intrinsic integration of both transistor and NVM in each single FeFET presents a new dimension of memory-logic synergy and may be exploited for further optimization in algorithms and circuit architectures. This approach has become promising and also reasonably practical with the emergence of neural networks, where a set of weighted states stored in a memory array accept input vectors and generate outputs through computing in the array and sensing interfaces. There has been early-stage research in using FeFET as the synapse for neural networks [9]. Design automation techniques to reduce the gap between the FeFET devices and the neural network hardware implementations could be of great significance.

References:

Salahuddin, S. & Datta, S. Use of negative capacitance to provide voltage amplification for low power nanoscale devices. Nano Lett. 8, 405–410 (2008).
Krivokapic, Z. et al. 14 nm ferroelectric FinFET technology with steep subthreshold slope for ultra-low power applications. 2017 IEEE Int. Electron Dev. Meet. (2017).
Wu, S.Y. et al. A new ferroelectric memory device, metal- ferroelectric-semiconductor transistor," IEEE Transactions on Electron Devices 8, 499-504 (1974).
Aziz, A. et al. Computing with ferroelectric FETs: Devices, Models, Systems, and Applications. 2018 Design Automation and Test in Europe.
Salahuddin, S. et al. The era of hyper-scaling in electronics. Nature Electronics. 8, 442-450 (2018)
https://en.wikipedia.org/wiki/Dennard_scaling
Liu, Z. et al. A critical examination of ‘quasi-static negative capacitance’ (QSNC) theory. 2018 IEEE Int. Electron Dev. Meet. (2018)
Yadav, A.K. et al. Spatially resolved steady-state negative capacitance. Nature 565, 468–471 (2019)
Ni, K. et al. SoC Logic Compatible Multi-Bit FeMFET Weight Cell for Neuromorphic Applications. 2018 IEEE Int. Electron Dev. Meet. (2018).

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Paper Submission Deadlines

ISVLSI’19 – IEEE Computer Society Annual Symposium on VLSI
Miami, FL
Deadline: Feb 17, 2019

Jul 15-17, 2019
http://www.isvlsi.org

BIOCAS'19 – Biomedical Circuits and Systems Conference
Nara, Japan
Deadline for abstract: Mar 1, 2019
Oct 17-19, 2019
http://www.biocas2018.org

LCTES'19 – Int'l Conference on Languages Compilers, Tools and Theory of Embedded Systems
Phoenix, AZ
Deadline: Mar 1, 2019 (Abstracts due: Feb 22, 2019)
Jun 22, 2019
https://conf.researchr.org/home/LCTES-2019

ISLPED'19 – ACM/IEEE Int'l Symposium on Low Power Electronics and Design
Lausanne, Switzerland
Deadline: Mar 4, 2019 (Abstracts due: Feb 25, 2019)
Jul 29-31, 2019
http://www.islped.org

NATW'19 – IEEE North Atlantic Test Workshop
Essex, Vermont
Deadline: Mar 8, 2019
May 13-15, 2019
http://natw.ieee.org

AHS'19 - NASA/ESA Conference on Adaptive Hardware and Systems
Colchester, UK
Deadline: Mar 29, 2019
Jul 22-24, 2019
http://www.ahs-conf.org

ICCAD'19 – IEEE/ACM Int'l Conference on Computer-Aided Design
Westminster, CO
Deadline: Apr 8, 2019 (Abstracts due: Apr 1, 2019)
Nov 4-7, 2019
http://www.iccad.com

ESWEEK'19 - Embedded Systems Week (CASES, CODES+ISSS, and EMSOFT)
New York, NY
Deadline: Apr 12, 2019 (Abstracts due: Apr 5, 2019)
Oct 13-18, 2019
http://www.esweek.org

BodyNets'19 – Int'l Conference on Body Area Networks
Florence, Italy
Deadline: Apr 15, 2019
Oct 2-3, 2019
http://www.bodynets.org

VLSI-SoC'19 – IFIP/IEEE Int'l Conference on Very Large Scale Integration
Cuzco, Peru
Deadline: Apr 25, 2019 (Abstracts due: Apr 18, 2019)
Oct 6-9, 2019
www.vlsi-soc.com

IWBDA'19 - Int'l Workshop on Bio-Design Automation
Cambridge, England
Deadline: May 2019 (expected)
Jul 9-12, 2019
http://www.iwbdaconf.org/2019

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Upcoming Symposia, Conferences and Workshops

ISSCC'19 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Feb 17-21, 2019
http://isscc.org

FPGA'19 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Seaside, CA
Feb 24-26, 2019
http://www.isfpga.org

ISQED'19 - Int'l Symposium on Quality Electronic Design
Santa Clara, CA
Mar 6-7, 2019
http://www.isqed.org

BSN'19 – IEEE Int'l Conference on Wearable and Implantable Body Sensor Networks
Chicago, IL
Mar 19-22, 2019
https://www.bhi-bsn-2019.org/bsn-2019

BHI'19 – IEEE Int'l Conference on Biomedical and Health Informatics
Chicago, IL
Mar 19-22, 2019
https://www.bhi-bsn-2019.org/bhi

TAU'19 – ACM Int'l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems
Monterey, CA
Mar 21-22, 2019
http://www.tauworkshop.com

DATE'19 - Design Automation and Test in Europe
Florence, Italy
Mar 25-29, 2019
http://www.date-conference.com

Quo Vadis, Logic Synthesis? - A Workshop at DATE'19
Florence, Italy
March 29, 2019
https://www.date-conference.com/conference/workshop-w09

ISPD'19 – ACM Int'l Symposium on Physical Design
San Francisco, CA
Apr 14-17, 2019
http://www.ispd.cc

HOST'19 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
Tysons Corner, VA
May 6-10, 2019
http://www.hostsymposium.org

GLSVLSI'19 – ACM Great Lakes Symposium on VLSI
Washington D.C., USA
May 9-11, 2019
http://www.glsvlsi.org

ASYNC'19 – IEEE Int'l Symposium on Asynchronous Circuits and Systems
Hirosaki, Japan
May 12-15, 2019
http://asyncsymposium.org

ISCAS'19 – IEEE Int'l Symposium on Circuits and Systems
Sapporo, Japan
May 26-29, 2019
http://iscas2019.org

DAC'19 – Design Automation Conference
Las Vegas, NV
Jun 2-6, 2019
http://www.dac.com/

ISCA'19 – Int'l Symposium on Computer Architecture
Phoenix, AZ
Jun 22-26, 2019
https://iscaconf.org

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Funding Opportunities

'"North America"'

Keck Foundation
Deadline: various
http://www.wmkeck.org/grant-programs/research/

USDA Foundational Program
Deadline: various
http://www.grants.gov/web/grants/view-opportunity.html?oppId=283836

NATO: Science for Peace and Security
Deadline: Proposals accepted anytime; reviews take place February 1 and May 15
http://www.nato.int/cps/en/natolive/87260.htm

Air Force Research Laboratory: Research Collaboration Program (BAA-RQKM-2013-0005)
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=212295

Federal Aviation Administration Grants for Aviation Research (FAA-12-01)
Deadline: open to December 2019
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=134953

AFRL RD/RV University Cooperative Agreement
Deadline: open to Nov 23, 2020
http://www.grants.gov/web/grants/view-opportunity.html?oppId=280237

NASA Fellowship Programs
Deadline: Various
http://science.nasa.gov/researchers/sara/fellowship-programs/

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Students-Etudiants/PG-CS/index_eng.asp

itacs Accelerate PhD Fellowship: Ontario Business Grants Program
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/...

Collaborative Research and Development Grants
(including DND/NSERC Research Partnership Grants)
http://www.nserc-crsng.gc.ca/Professors-Professeurs/RPP-PP/CRD-RDC_eng.asp

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Professors-Professeurs/CFS-PCP/index_eng.asp

http://www.nserc-crsng.gc.ca/Innovate-Innover/Engage-Mobiliser_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Collaborate-Collaborer_eng.asp
Research and Development Funding for Business Innovation (Multiple Organizations)
Deadline: Various
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/

'''Europe'''

Horizon 2020
Deadline: Various
http://goo.gl/geBouC

German Academic Exchange Service (DAAD)
Deadline: Various
https://www.daad.org/scholarship

German Research Foundation (DFG)
Deadline: Various
http://www.dfg.de/en

Helmholtz Association
Deadline: Various
https://www.helmholtz.de/en

Leibniz Association
Deadline: Various
http://www.leibniz-gemeinschaft.de/en/home

Leopoldina
Deadline: Various
https://www.leopoldina.org/en/about-us

ax Planck Society
Deadline: Various
https://www.mpg.de/en

Swiss National Science Foundation
Deadline: Various
http://www.snf.ch/en/

'''Asia'''

Korea:

National Research Foundation of Korea
Deadline: Various
http://www.nrf.re.kr/nrf_eng_cms/show.jsp?show_no=90&check_no=89&c_relation=0&c_...

China:

National Natural Science Foundation of China
Deadline: Various
http://www.nsfc.gov.cn/publish/portal1/

Singapore:

National Research Foundation (NRF) Singapore
http://www.nrf.gov.sg
RIE 2020 plan
Deadline: Various
http://www.nrf.gov.sg/rie2020

India:

Ministry of Electronics and Information Technology
Deadline: Various
http://meity.gov.in/content/research-development

Department of Science and Technology (Nano Mission)
Deadline: Various
http://nanomission.gov.in/

University Grants Commission
Deadline: Various
http://www.ugc.ac.in/

Ministry of Education Academic Research Fund
Deadline: Various
https://www.olga.moe.gov.sg/default.aspx

Agency for Science Technology and Research (A*STAR) Science and Engineering Research Council (SERC)
Deadline: Various
https://www.a-star.edu.sg/Research/Funding-Opportunities/Grants-Sponsorship.aspx

Multiple Funding
Deadline: Various
http://www.computerscienceonline.org/cs-scholarships/

'"Oceania/Polynesia"'

Polynesian Cultural Center (Hawaii) - International Student Scholarship Program
For studying in BYU Hawaii
http://www.polynesia.com/students.html

New Zealand:

inistry of Business, Innovation and Employment
Deadline: Various
http://www.mbie.govt.nz/

Australia:

Premier's Research and Industry Fund
Deadline: Various
http://www.statedevelopment.sa.gov.au/science/premiers-research-and-industry-fun...

Australian Research Council
Deadline: Various
http://www.arc.gov.au

'"South America"'

Brazil:

Coordination for the Improvement of Higher Education Personnel (CAPES)
Deadline: Various
http://www.iie.org/programs/capes#.WAu2kJMrJPM

Ministry of Science, Technology, Innovation and Communications (CNPq)
Deadline: Various
http://www.cnpq.br/

'"Africa"'

Other scholarships for African Students (list of over 30 different scholarships)

Deadline: Various
http://www.afterschoolafrica.com/12264/list-annual-engineering-scholarships-afri...

Nigeria:

Bilateral Education Agreement (BEA) Awards (both Undergraduate and Post Graduate)
Deadline: Nomination interview - March'17
http://www.fsb.gov.ng/index.php/scholarship/menu-styles/bilateral-agreement

Federal Scholarship Board
Deadline: Various
http://www.fsb.gov.ng/index.php

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Call for Papers: ASAP 2019

The 30th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2019)
Cornell Tech, New York, USA, July 15-17, 2019
Website: asap2019.csl.cornell.edu

The 30th IEEE International Conference on Application-specific Systems, Architectures and Processors 2019 will take place in Cornell Tech, New York, United States.

The history of the event traces back to the International Workshop on Systolic Arrays, organized in 1986 in Oxford, UK. It later developed into the International Conference on Application Specific Array Processors. With its current title, it was organized for the first time in Chicago, USA in 1996. Since then it has alternated between Europe and North-America. The conference will cover the theory and practice of application-specific systems, architectures, and processors. The 2019 conference will build upon traditional strengths in areas such as computer arithmetic, cryptography, compression, signal and image processing, network processing, reconfigurable computing, application-specific instruction-set processors, and hardware accelerators.

TOPICS OF INTEREST (but not limited to)
Big data analytics
Cloud computing infrastructures and acceleration
Heterogeneous computing in data centers
Accelerating data center workloads
FPGA-based deep learning
Embedded systems and domain-specific solutions (digital media, gaming, automotive applications)
Accelerating genomic computations
Acceleration of data analytics
Reconfigurable computing in the IoT era
Applications in finance
Wireless and mobile systems
Application-aware controller synthesis
Emerging technologies (optical models, 3D Interconnects, devices)
Reconfigurable accelerators
Hardware and software architectures for cyber-physical systems
Distributed systems & networks
Critical issues (security, energy efficiency, fault-tolerance)
Autonomous and semi-autonomous large-scale CPS
Autonomic computing systems
High-level design methods (hardware/software co-design, compilers)
Simulations and prototyping (performance analysis, verification tools)
Socio-technical systems

IMPORTANT DATES
Submission deadline: April 8, 2019
Decision notification: May 6, 2019
Camera ready version: May 29, 2019

SUBMISSION OF PAPERS

All manuscripts will be reviewed by at least three members of the program committee. Submissions should be a complete manuscript or, in special cases, may be a summary of relevant work. Manuscript for full paper should not exceed 8 single-space, double-column pages using 10-point size font on 8.5x11 inch pages (IEEE conference style) including references, figures, and tables. Manuscript for short papers should not exceed 4 single-space, double-column pages. Manuscripts for posters should not exceed 2 single-spaced, double-column pages. Submitted papers should not have appeared in or be under submission for a different workshop, conference or journal. It is also expected that all accepted papers (full, short or poster) will be presented at ASAP by one of the authors. Accepted full and short papers will be included in the proceedings and published in IEEE Xplore. Failure to present will result in the removal of the submission from the proceedings before publication. All papers must be submitted electronically in PDF format.

Submission website: https://asap2019.csl.cornell.edu/submission/
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Call for Papers: LCTES 2019

ACM LCTES 2019 International Conference on Languages
Compilers, Tools and Theory of Embedded Systems

co-located with PLDI 2019, June 22-28, 2019
Phoenix Convention Center, Phoenix, Arizona, United States
Website: https://conf.researchr.org/home/LCTES-2019

Embedded system design faces many challenges both with respect to functional requirements and nonfunctional requirements. The challenges are in the design process, developer productivity, verification, validation, maintainability, and meeting performance goals and resource constraints of the embedded system. Novel design-time and run-time approaches are needed to meet the demand of emerging applications and to exploit new hardware paradigms, including scaling up to multicores, in-memory computing, involving accelerators in the computing mix, and even distributed systems built using multi-cores.

LCTES 2019 solicits papers presenting original work on programming languages, compilers, tools, theory, and architectures that help in overcoming these challenges. Research papers on innovative techniques are welcome, as well as experience papers on insights obtained by experimenting with real-world systems and applications.

TOPICS OF INTEREST
Original contributions are solicited on the topics of interest including, but not limited to:
Programming languages
Compilers
Tools for analysis, specification, design, and implementation
Theory and foundations of embedded systems
Novel embedded architectures
Mobile systems and IoT
Industrial case studies

PAPER CATEGORIES
Full paper: 10 pages presenting original work.
Work-In-Progress (WIP) paper: 2-4 page papers presenting original ideas that are likely to trigger interesting discussions.
Accepted papers inboth categories will appear in the proceedings published by ACM.

INVITATION TO SUBMIT IN ACM TECS
This year, the top full papers from LCTES 2019 be invited to be published in a special issue of ACM Transactions on Embedded Computing Systems (TECS).

ARTIFACT EVALUATION
Authors of accepted full papers will be invited to formally submit their supporting materials to the Artifact Evaluation process. The Artifact Evaluation process is run by a separate committee whose task is to reproduce (at least some) experiments and asses how the artifacts support

the work described in the papers. This submission is voluntary and will not influence the final decision regarding the papers.

WHERE/HOW/WHAT TO SUBMIT
Submissions due on February 22, 2019.

Submissions must be in ACM proceedings format, double-column, 10-point type, and may not exceed 10 pages for full papers and 4 pages for work-in-progress papers. These page limits do not include the references. There is no page limit for references for both categories of papers.

Where to submit: https://lctes2019.hotcrp.com/

Details of submission: https://conf.researchr.org/home/LCTES-2019#Submission-Instructions

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Special Issue CFP: IEEE Design and Test

Special Issue Call for Papers from IEEE Design & Test: Machine Intelligence at the Edge

Aim and Scope

Recent years have seen widespread application of machine learning (ML) to a diverse range of industries and problem domains. By taking advantage of the availability of massive amounts of data and scalable compute resources, ML methods -- including linear models (e.g., SVMs, logistic regression), decision trees (e.g., XGBoost, lightGBM), and deep neural networks (e.g., CNNs and RNNs) -- are able to outperform traditional hand-tuned models on today's large-scale AI tasks. Due to their compute-intensive nature, machine learning systems are typically deployed on clusters of CPUs/GPUs in public or private clouds. However, the success of ML in sensing applications such as object detection and speech recognition has also driven a demand for such technology (both training and inference) in edge settings, for applications such as autonomous vehicles, mobile devices, and embedded/IoT systems. Unfortunately, most existing ML models, hardware, and frameworks are tailored towards a server environment and are ill-equipped for edge computing.

Bringing ML to today's emerging edge applications involves tackling a diverse set of challenges. To give just a few examples: power and energy requirements for mobile, strict latency constraints for autonomous vehicles, security concerns of model/data transmission for IoT, and intermittent operation for embedded sensors. State-of-the-art ML systems in industry today already use custom frameworks, algorithms, and hardware built for a server infrastructure.

Addressing the unique challenges of ML at the edge will similarly require specialization, co-design, and integration of domain knowledge for the edge across the computing stack.

Topics of Interest:

This special issue of IEEE Design and Test calls for novel research on machine learning models, hardware architectures, programming tools, and design methodologies for ML at the Edge. Topics of interest include but not limited to:

- Novel ML algorithms co-designed for computing and/or learning at the edge
- Techniques to compress and/or exploit redundancy in existing ML models
- Methodologies to design and test intelligent edge systems, with emphasis on power, latency, and security requirements
- Constraint aware compilers and tools for mapping ML applications to edge devices
- Efficient hardware architectures for ML algorithms
- Benchmarking ML workloads and/or frameworks on the edge, including accuracy, performance, power and energy etc.
- Comparison studies of different devices (GPUs, ASICs, FPGAs, etc) and architectures (systolic arrays, sparse vs. dense, etc) for the edge
- Hierarchical and distributed approaches to enable edge ML

The special issue particularly welcomes and encourages the submissions from industry or collaborative works between industry and academia for this fast growing area.

Submission Guidelines:

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted

electronically to IEEE Manuscript Central at https://mc.manuscriptcentral.com/dandt. Indicate that you are submitting your article to the special issue on Machine Intelligence at the Edge. All articles will undergo the standard IEEE Design & Test review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere.

Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Resources at http://ieee-ceda.org/publication/ieee-design-test-dt/paper-submission-instructio... to view links in Submission Guidelines Basics and Electronic Submission Guidelines and requirements.

Schedule:

Submission Deadline: March. 1st, 2019
Notification First Round: May 1st, 2019
Submission of Revision: June 16th, 2019
Final Notification: August 1st, 2019
Final Papers Due: September 1st, 2019

Guest Editors:
(Please direct any questions regarding this special issue to one of the following.)

Luca Benini <lbenini@iis.ee.ethz.ch>, ETH Zurich, Switzerland
Deming Chen <dchen@illinois.edu>, University of Illinois at Urbana-Champaign, USA
Jinjun Xiong <jinjun@us.ibm.com>, IBM, USA
Zhiru Zhang <zhiruz@cornell.edu>, Cornell University, USA
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Call for Participation: Quo Vadis, Logic Synthesis?

Call for Participation: Quo Vadis, Logic Synthesis? - A Workshop at DATE'19
Florence, Italy
Friday, March 29
https://www.date-conference.com/conference/workshop-w09

In 1984, the book on Espresso by R. Brayton, G. Hachtel, C. McMullen, A. Sangiovanni-Vincentelli contributed the foundations of modern logic synthesis. The work done in leading academic and industrial research institutions triggered the first wave of modern logic design tools like Espresso, MIS, SIS, which then became the backbone of the industrial design chains for digital systems provided by the newborn Electronic Design Automation industry. After many research breakthroughs and industrial successes, it is time for an assessment of the perspectives of logic synthesis, both as a core technology in digital system design and an enabling technology in other domains (biological synthesis, machine learning for data analysis, etc.). Towards this goal, this workshop brings together a heterogeneous mix of speakers, from both academia and industry, spanning 35 years of research and development in logic synthesis.

PROGRAM
7:30-8:30 Registration desk opens
8:30-8:40 Introduction by Luca Carloni and Tiziano Villa
8:40-9:00 Thirty-five years after the Espresso book: a retrospective on logic synthesis, Tiziano Villa
9:00-10:00 Algorithmic foundations of logic synthesis - Part 1
- Extracting functions from Boolean relations, Jordi Cortadella
- Expressing flexibility in logic synthesis by Boolean relations, Anna Bernasconi
10:00-10:15 Coffee break
10:15-11:15 Algorithmic foundations of logic synthesis - Part 2
- Craig interpolation in logic synthesis applications, Jie-Hong Jiang
- SAT in logic synthesis, Mathias Soeken
11:15-12:15 Synthesis for emerging technologies
- XOR gates in emerging technologies, Valentina Ciriani
- Majority Logic Synthesis, Luca Amaru'
12:15-13:15 Lunch

13:15-14:15 Approximate synthesis
- Approximate logic synthesis for area and delay optimization, Weikang Qian
- Systematic approaches to approximate logic synthesis, Sherief Reda
14:15-15:15 High-level synthesis
- High-level synthesis: status and future trends, Andres Takach
- How high-level synthesis enables design for reusability of hardware accelerators, Luca Carloni
15:15-15:30 Coffee break
15:30-16:30 Logic synthesis and machine learning
- Automated synthesis of distributed/parallel computing through templates and inductive reasoning, Masahiro Fujita
- On the minimization of variables to represent sparse multi-valued input decision diagrams, Tsutomu Sasao
16:30-17:30 Logic synthesis and biological models
- Synthetic biology: application of logic synthesis to biological models, Gabriella Trucco
- Stochastic logic applied to DNA computing, Marc Riedel

FOR MORE INFORMATION: https://www.date-conference.com/conference/workshop-w09

WORKSHOP ORGANIZERS Luca Carloni (Columbia University) and Tiziano Villa (Universita' di Verona)

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Call for Papers: ISVLSI 2019

ISVLSI 2019
July 15-17, 2019
Miami, Florida

The IEEE Symposium on VLSI (ISVLSI) 2019 explores emerging trends, novel ideas and basic concepts covering a broad range of VLSI-related topics: from VLSI systems, tools and design methods at different abstraction levels, to bringing VLSI design and methods into new technologies such as nano and molecular devices and burgeoning application areas, such as hardware security, and artificial intelligence. Future design methodologies are also one of the key topics at the symposium, as well as new EDA tools to support them. Over three decades ISVLSI has been a unique forum promoting multidisciplinary research and new visionary approaches in the area of VLSI, bringing together leading scientists and researchers from academia and industry. The ISVLSI proceedings will be published by IEEE Computer Society Press. Selected papers from past editions have been subsequently published in special issues of top archival journals. ISVLSI has a good reputation of bringing together well-known international scientists as invited speaks. ISVLSI 2019 will continue the momentum and carry forward these well-established trends for further growth of the symposium.

Contributions are sought in, but not limited to, the Following Tracks
1) Circuits, Reliability, and Fault-Tolerance (CRT)
2) Computer-Aided Design and Verification (CAD)
3) Digital Circuits and FPGA based Designs (DCF)
4) Emerging and Post-CMOS Technologies (EPT)
5) System Design and Security (SDS)
6) VLSI for Applied and Future Computing (AFC)

Paper Submission: Authors are invited to submit full-length (6 pages maximum), original, unpublished papers along with an abstract of at most 200 words. To enable blind review, the author list should be omitted from the main document. Papers violating length and blind-review criteria would be withdrawn from the review process. Previously published papers or papers currently under review for other conferences/journals should not be submitted and will not be considered for publication.

Paper Submission Site: https://easychair.org/conferences/?conf=isvlsi2019
Important Dates:
Paper Submission Deadline: February 17, 2019
Acceptance Notification: April 21, 2019
Submission of Final Version: May 12, 2019

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Call for Papers: NOCS 2019

13th IEEE/ACM International Symposium on Networks-on-Chip
October 17 ñ 18, 2019, New York, USA (Co-located with Embedded Systems Week 2019)
https://www.engr.colostate.edu/nocs2019/

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to interdisciplinary research on on-chip, package-scale, chip-to-chip, and datacenter rack-scale communication technology, architecture, design methods, applications and systems. NOCS brings together scientists and engineers working on network-on-chip (NoC) innovations and applications from inter-related research communities, including discrete optimization and algorithms, computer architecture, networking, circuits and systems, packaging, embedded systems, and design automation. Topics of interest include, but are not limited to:

NoC Architecture and Implementation
- Network architecture (topology, routing, arbitration)
- Timing, synchronous/asynchronous communication
- NoC reliability issues and solutions
- Security issues and solutions in NoC architectures
- Power/thermal issues at NoC un-core and system-level
- Network interface issues and solutions
- Signaling and circuit design for NoC links and routers

Communication Analysis, Optimization, & Verification
- NoC performance analysis and Quality of Service
- Modeling, simulation, and synthesis of NoC
- Verification, debug and test of NoC
- NoC design and simulation methodologies and tools
- Benchmarks, experiences on NoC-based hardware
- Communication-efficient algorithms
- Communication workload characterization & evaluation

Novel NoC Technologies
- Optical, wireless, CNT, and other emerging technologies
- NoC for 2.5D and 3D packages
- Package-specific NoC design
- Network coding and compression solutions
- Approximate computing for NoC and NoC-based systems

NoC for Intelligent Physical Systems
- NoC design for Deep Learning
- Mapping of existing and emerging applications onto NoC
- NoC case studies, application-specific NoC design
- NoC for FPGA, structured ASIC, CMP and MPSoC
- NoC designs for heterogeneous systems
- NoC for CPU-GPU and data-center-on-a-chip (DCoC)
- Scalable modeling of NoC
- Machine learning for NoC and NoC-based Systems

NoC at the Un-Core and System-level
- Design of memory subsystem (un-core) including memory controllers, caches, cache coherence protocols in NoC
- NoC for new memory/storage technologies
- NoC support for processing-in-memory
- OS support for NoC
- Programming models for NoCs
- Interactions between large-scale systems (datacenter, edge and fog computing) and NoC-based building blocks

Inter/Intra-Chip and Rack-Scale Network
- Unified inter/intra-chip networks
- Hybrid chip-scale and datacenter rack-scale networks
- All aspects of inter-chip and rack-scale network design

Electronic paper submission requires a full paper, up to 8 double-column ACM (sigconf) format pages, including figures and references. The program committee will use a double-blind review process to evaluate papers based on scientific merit, innovation, relevance, and presentation. Submitted papers must describe original work that has not been published before or is under review by another conference or journal at the same time. Each submission will be checked for any

significant similarity to previously published works or for simultaneous submission to other archival venues, and such papers will be rejected. Proposals for special sessions and demos are invited. Paper submissions and demo proposals by industry researchers or engineers to share their experiences and perspectives are also welcome. A percentage of accepted papers will be recommended for publication in an IEEE journal after revision according to the reviewersí comments. Please find the detailed submission instructions for paper submission, special session, and demo proposals at the submission webpage.

Important Dates (Anywhere on Earth)
Abstract registration: May 10, 2019
Full paper submission: May 17, 2019
Notification of acceptance: July 8, 2019
Final version due: July 22, 2019

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Notice to Authors

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
Circulation: 2,700