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The resource for EDA Professionals

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Comments from the Editors

Dear ACM/SIGDA member,

We are excited to present to you the January newsletter. We encourage you to invite your students and colleagues to be a part of the SIGDA newsletter. The newsletter covers a wide range of information from upcoming conference and funding deadlines, hot research topics to news from our community.
Get involved and contact us if you want to contribute an article or announcement.

Happy reading!

Aida Todri-Sanial
Yu Wang
Editors-in-Chief, SIGDA E-News

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"SIGDA E-News Editorial Board:"

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"'Yiyu Shi'", E-Newsletter Associate Editor for SIGDA Live column

"'Rajsaktish Sankaranarayanan'", E-Newsletter Associate Editor for SIGDA Researcher spotlight column

Back to Contents

SIGDA News

(1) "Researchers Explore Emerging Memories for AI"
[https://www.eetimes.com/document.asp?doc_id=1334122]

Resistive random access memory (ReRAM) and other emerging memory technologies have been getting a lot of attention in the past year as semiconductor companies look for ways to more efficiently deal with the requirements of artificial intelligence and neuromorphic computing.

(2) "Intel Steps Toward Heterogeneous Integration"
[https://www.eetimes.com/document.asp?doc_id=1334073]

Intel demonstrated a new 3D packaging technology for face-to-face stacking of logic, scheduled to be available in the second half of next year. The company also tipped a new processor microarchitecture and a new graphics architecture on a day when its chief architect laid out the company's vision for future computing architectures.

(3) "Foxconn Reportedly Readies Chip Fab in China"
[https://www.eetimes.com/document.asp?doc_id=1334120]

Taiwan's Hon Hai Precision is set to break ground in 2020 on a $9 billion 300mm chip fab in the city of Zhuhai in southern China, according to a report by the Nikkei news service.

(4) "MIPS Goes Open Source"
[https://www.eetimes.com/document.asp?doc_id=1334087]

Without question, 2018 was the year RISC-V genuinely began to build momentum among chip architects hungry for open-source instruction sets. That was then.

(5) "5G Networks Under Construction"
[https://www.eetimes.com/document.asp?doc_id=1334092]

Carriers are racing to turn on their first 5G services, but the underlying upgrade that they are working on will take years, according to a handful of engineering managers helping build the networks.

(6) "Eval Kit Enables 3D Radar Imaging SoC Development"

[https://www.eetimes.com/document.asp?doc_id=1334081]

Vayyar Imaging has introduced a new mmWave evaluation kit giving engineers and software developers access to its 3D radio-wave–based imaging sensor technology.

(7) "Smartphone Shipments Expected to Rebound in 2019"
[https://www.eetimes.com/document.asp?doc_id=1334076]

Shipments of smartphones, the mainstay of the electronics industry, are expected to rebound, returning to low-single-digit growth in 2019, according to market research firm International Data Corp. (IDC).

(8) "BMW, Microsoft Join $200 Million Graphcore Funding"
[https://www.eetimes.com/document.asp?doc_id=1334106]

UK-based developer of machine intelligence processors Graphcore announced a new round of $200 million in funding, including investment from BMW and Microsoft. The deal — which brings Graphcore's total funding to $300 million — values the company at $1.7 billion.

(9) "Fab Tool Billings Fall for First Time in 2 Years"
[https://www.eetimes.com/document.asp?doc_id=1334097]

Billings among North American manufacturers of semiconductor production equipment posted a year-over-year decline last month for the first time in two years as the fab tool market continues to cool after two years of white-hot growth.

(10) "Robocar's 2018 Reverse Puts ADAS in Drive"
[https://www.eetimes.com/document.asp?doc_id=1334100]

From Uber's first fatality accident in March to Waymo's substantially scaled-back commercial self-driving service launch earlier this month, 2018 offered a clear reminder that "autonomy" remains a goal not easily reached, whether by emerging tech startups, leading automotive OEMs/Tier Ones, or even well-funded self-driving pioneers like Waymo.

Back to Contents

SIGDA Local Chapter News

The 3rd Future Chips Forum has been successfully held on December 10-11, 2018, in Reception Hall of the Main Building, Tsinghua University. The Future Chips forum is an annual event held by Beijing Innovation Center for Future Chips and the Institute of Microelectronics, Tsinghua University. The forum aims to provide an opportunity for experts from academia and industry to exchange new ideas and integrate expertise.

The Main Theme of this year's forum is "Reconfigurable Computing in a New Golden Age". This year, over 30 prominent scientists from all over the world joined the forum at Tsinghua University to share the latest trends and research development about reconfigurable computing. The forum committee includes Prof. Zheng You, Prof. Shaojun Wei, Prof. Sharon X. Hu, Prof. Yuan Xie, Prof. Yiran Chen, Prof. Huaqiang Wu, and Prof. Shouyi Yin. Please refer to the following link for more details: http://www.icfc.tsinghua.edu.cn/futurechips2018/index.html

This Future Chips Forum is co-located with the Workshop on Device to Application Benchmarking, which is held on December 9, 2018 at Room 312, FIT Building, Tsinghua University. The workshop brings together industrial experts and academic researchers to explore future prospects particularly related to benchmarking for technology driven machine learning accelerators and compute-in-memory hardware infrastructure. It is co-sponsored by University of Notre Dame (U.S.) and Tsinghua University (China). Please refer to the following link for more details:
http://www.icfc.tsinghua.edu.cn/futurechips2018/workshop.html

Back to Contents

SIGDA Award

Best Paper Awards at ACM/SIGDA Sponsored Events

ICCAD 2018: International Conference On Computer Aided Design, http://www.iccad.com/

1. Front-End Best Paper Award: "DNN Builder: An Automated Tool for Building High-Performance DNN Hardware Accelerators for FPGAs", by Xiaofan Zhang (Univ. of Illinois at Urbana-Champaign), Junsong Wang (IBM Research - China), Chao Zhu (IBM Research - China), Yonghua Lin (IBM Research - China), JinJun Xiong (IBM T.J. Watson Research Center), Wen-Mei Hwu (Univ. of Illinois at Urbana-Champaign) and Deming Chen (Univ. of Illinois at Urbana-Champaign).

2. Back-End Best Paper Award: "PolyCleaner: Clean Your Polynomials Before Backward Rewriting to Verify Million-Gate Multipliers", by Alireza Mahzoon (Universität Bremen), Daniel Grosse (Universität Bremen/DFKI) and Rolf Drechsler (Universität Bremen/DFKI).

3. Ten Year Retrospective Most Influential Paper Award: "A Low-Overhead Fault Tolerance Scheme for TSV-Based 3D Network on Chip", by Igor Loi (University of Bologna), Subhasish Mitra (Stanford University), Thomas H. Lee (Stanford University), Shinobu Fujita (Toshiba) and Luca Benini (University of Bologna), 2008.

Back to Contents

Researcher Spotlight

Hello readers,

This edition of Researcher spotlight introduces [https://www.cse.iitm.ac.in/profile.php?arg=MTg= Prof. Veezhinathan Kamakoti] with the Department of Computer Science and Engineering at the Indian Institute of Technology, Chennai, India. He leads the Reconfigurable and Intelligent Systems Engineering (RISE) lab focusing on Information Security, Computer Architecture and VLSI Design. He completed B.E. in Computer Science and Engineering from University of Madras followed by M.S. (By research) and Ph.D. at Department of Computer Science and Engineering, Indian Institute of Technology Madras. His post-doctoral assignments were at Supercomputer Education and Research Center, Indian Institute of Science, Bengaluru and Institute of Mathematical Sciences, Chennai. He leads the Shakti open-source initiative at IIT-Madras, which is building open source, production-grade processors, and associated components like interconnect fabrics, verification tools, storage controllers, peripheral IPs and SoC tools. Some excerpts from a recent conversation.

'''1.Choice of RISC-V ISA seems well suited to the Base-class of processors. What challenges do you foresee in scaling up towards enterprise-grade performance? How do you plan to address them?'''

RISC-V ISA is suited even for high-performance processors including out-of-order execution ones. Given the Instruction encoding, I do not see any major issues in realization of out of order superscalar cores at high frequencies. Looking at server grade chips the challenge is integration of Peripheral IPs including high-speed ones like PCIX, 10G Ethernet, DDR4 etc. Many of the IPs have foundry specific PHYs. How this will go together with an open source initiative is to be seen. The integration of peripheral IPs is going to be the challenge. In addition, prototyping simple cores can be done on commercially of the shelf FPGA boards. Prototyping large-scale multicore designs is also a challenge both from complexity and cost perspectives.

'''2.High-level synthesis (HLS) is gaining traction again, in the context of RTL generation for silicon. Can you share the reasons behind choosing Blue-spec System Verilog (BSV), as opposed to Chisel, considering say multi-core processors?'''

BSV was used in our Curriculum for more than a decade. In addition, Chisel could not be used in live mission-mode projects as we do not have timeline assured commercial support. Chisel is promising but need many more features and assured support for adoption into a National programme like SHAKTI.

'''3.Can you talk a bit about the physical implementation and challenges, including synthesizability, silicon implementation and design bring-up? Was it a custom methodology or an ASIC-like methodology?'''

For both the 22nm tape out at Intel, Oregon, USA fab and 180nm tape out at SCL, Chandigarh, India fab the ASIC-like methodology was followed for the backend. Commercial VLSI CAD tool flow was used. The synthesizability is ensured by the BSV compiler. In addition, there was a multifactor boost in productivity in both design and verification efforts because of the use of Blue spec. The language by itself took care of major issues that could not have been addressed by Verilog/VHDL in such an efficient manner.

'''4.Taping-out silicon from academia poses unique challenges including project-modularization, funding, flowing student population, diverse interests & skills, for instance. How were these (and more?) addressed? Can you share your

insights?"'

As academicians we run a company with 100% attrition in the month of May and 100% fresh recruitment in the month of June. There was a core team of research scholars who took care of this transitions over the last few years and that is one of major reason for success. We received our first funding from Government in the month of November 2017. Till then, SHAKTI was run with zero funding. However, we had learnt lots during this "non-funded" times which helped us quickly ramp-up and deliver GDSII of two chips by February 2018. The "Make-in-India" pitch of Government of India and specifically by the Prime Minister of India helped us get more community participation in this effort. Many companies including Intel, HCL, Synopsys, Cadence, Mentor and Xilinx helped us with the tool flows, prototyping and tapeout. Many of our alumnus volunteered to help us on their own during the tapeout time. We really felt proud and united, working on an important project for our Nation.

"'5.Sometimes commercial companies and Government agencies may lean towards sourcing chips from vendors who are available to offer support. Do you foresee similar challenges towards broader adoption? If so, can you talk about potential solutions to work around this?"'

We are very clear in this point. We do not want anyone to adopt SHAKTI just because it is Made-in-India but that it is globally competitive, matching or exceeding contemporary processors. Once we establish this, I think we will have a fair chance in the market. The success crucially depends upon making software development and debugging environments available. In this digital world, there are varieties of problems that are moving towards electronics-based solutions and each of them would require a processor core. The crucial point here is customization. The basic cores will be made available open source along with a set of peripheral IPs at our website Shakti.org.in
This will enable more exploration by prospective users and quick customization.

"'6.How can someone get involved in this project?"'

Our contact details are available at [http://shakti.org.in/ Shakti]

Back to Contents

"What is" Column

"'What is Multi-version Index Scheme?"'

"'Tseng-Yi Chen, Department of Computer Science and Engineering, Yuan Ze University. <tychen@saturn.yzu.edu.tw>"'

As cyber-physical systems (CPS) and internet-of-things (IoT) applications have been rapidly developed and widely applied in recent years, multi-version data management gradually becomes a critical issue in the design of multi-version database/file systems. Traditionally, database systems usually adopt an index structure, e.g., B+-tree-like structure, to provide efficient access to data items so as to increase the performance of read and write operations in database systems. Nevertheless, according to the prior research work [1], a B+-tree-like index scheme is not appropriate for maintaining the same data item with multiple versions. For efficient multi-version data management, many multi-version indexing schemes [2, 3, 4] have been presented and applied to multi-version database systems. Among them, multi-version B+-tree (MVBT) is the most efficient indexing scheme. As MVBT follows the spirit of the convention B+-tree design, it is a directed acyclic tree graph. Similarly, an MVBT index structure is composed of multiple B+-tree nodes, each of which can maintain different data items with its version information from the first version to the current version. More specifically, a multi-version B+-tree node represents for a range of data versions.

By inheriting the legacy of the B+-tree design, an MVBT node is composed of multiple entries, each of which contains the information of key, insertion version, deletion version, and pointer. For simplicity's sake, the information of an version entry could be denoted as . The lifetime information of a data item will be from its insertion version in_version to its deletion version del_version, i.e., [in_version, del_version). Since a leaf entry within an MVBT leaf node needs to address its corresponding data location, a leaf entry include the ptr field to record its data address. Instead, an inner entry within an MVBT node utilizes ptr field to point its child with the separator value as key. While a new data item is added to an MVBT scheme at time tc, a new version entry with in_version = tc and del_version = "∗" will be generated in an MVBT node. In the entry, tc represents the current version and ∗ denotes that this entry is a live entry. Conversely, while a data item is removed from a database/file system at time td, del_version information within its version entry will be

replaced by td. Therefore, if a data item currently exist in the databased system, its in_version and del_version are tc and ∗, respectively. Otherwise, a deleted data item will have tc and td in its version entry. If a version entry include td information in its del_version field, this version entry is called a dead entry.

For increase its query performance, the MVBT sets overflow condition and underflow condition. The overflow condition (also known as strong version overflow) will be triggered while the number of entries in an MVBT node reaches the maximum capacity. In other words, if an MVBT node does not have enough space to accommodate new version entry, the overflow condition will be triggered and the MVBT structure splits the overflow node into multiple MVBT nodes by version split and key split operations. A version split operation will copy current entries from the overflow node to a new node space and a key split will evenly separate current entries within the overflow block into two node spaces. On the other hand, if the number of current entries in an MVBT node is smaller than the predefined threshold (MINWT), the underflow condition will be satisfied and the current entries within the underflow MVBT node will be merged to its sibling node. In the original MVBT work [3], MINWT equals to b/a where b is the capacity of an MVBT node and a is non-zero positive value. Because the underflow situation will be resulted from version split operations and entry deletions, the MVBT categorized the underflow condition into the strong version underflow (resulted from version split operations) and the weak version underflow (resulted from entry deletions). No matter strong or weak version underflow, the MVBT will merge the copied current entries to another sibling node.

[1]. Tuukka Haapasalo, Ibrahim Jaluta, Bernhard Seeger, Seppo Sippu, and Eljas Soisalon-Soininen. “Transactions on the Multiversion B+-Tree.” In EDBT, 2009.

[2]. D. Zeinalipour-Yazti, S. Lin, V. Kalogeraki, D. Gunopulos, and W.A. Najjar. Microhash, “An Efficient Index Structure for Flash-based Sensor Devices.” In USENIX FAST. 31–44. 2005

[3]. Bruno Becker, Stephan Gschwind, Thomas Ohler, Bernhard Seeger, and Peter Widmayer. “An asymptotically optimal multiversion B-tree.” The VLDB Journal vol. 5, issue. 4, pp. 264-275, December 1996.

[4]. Yuan-Hung Kuan, Yuan-Hao Chang, Tseng-Yi Chen, Po-Chun Huang, and Kam-Yiu Lam. “Space-Efficient Index Scheme for PCM-Based Multiversion Databases in Cyber-Physical Systems.” ACM Trans. Embed. Comput. Syst. Vol. 16, issue 1, Article 21, 26 pages, October 2016.

Back to Contents

Paper Submission Deadlines

TAU’19 – ACM Int’l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems
onterey, CA
Deadline: Dec 1, 2018
Mar 21-22, 2019
http://www.tauworkshop.com

ISCA’19 – Int’l Symposium on Computer Architecture
Phoenix, AZ
Deadline: Dec 7, 2018 (Abstracts due: Dec 3, 2018)
Jun 22-26, 2019
https://iscaconf.org

ASYNC'19 – IEEE Int’l Symposium on Asynchronous Circuits and Systems
Hirosaki, Japan
Deadline: Dec 14, 2018 (Abstracts due: Dec 7, 2018)
May 12-15, 2019
http://asyncsymposium.org

GLSVLSI’19 – ACM Great Lakes Symposium on VLSI
Washington D.C., USA
Deadline: Dec 17, 2018
May 9-11, 2019
http://www.glsvlsi.org

Back to Contents

Upcoming Conferences and Symposia

ICPADS'18 – IEEE Int'l Conference on Parallel and Distributed Systems
Sentosa, Singapore
Dec 11-13, 2018
http://icpads.sg

FPT'18 - Int'l Conference on Field-Programmable Technology
Okinawa, Japan
Dec 11-15, 2018
http://icfpt.org

ISED'18 – Int'l Symposium on Electronic System Design
Kochi, India
Dec 13-15, 2018
http://ised2018.org

iSES'18 – IEEE Int'l Symposium on Smart Electronic Systems
Hyderabad, India
Dec 17-19, 2018
http://www.ieee-ises.org

HiPC'18 – IEEE Int'l Conference on High Performance Computing
Bengaluru, India
Dec 17-20, 2018
http://www.hipc.org

VLSID'19 – Embedded and VLSI Design Conference
Delhi (NCR), India
Jan 5-9, 2019
http://www.vlsidesignconference.org

HiPEAC'19: Int'l Conference on High Performance Embedded Architectures & Compilers
Valencia, Spain
Jan 21-23, 2019
https://www.hipeac.net/2019/valencia

ASP -DAC'19 - Asia and South Pacific Design Automation Conference
Tokyo, Japan
Jan 21-24, 2019
www.aspdac.com

ISSCC'19 – IEEE Int'l Solid-State Circuits Conference
San Francisco, CA
Feb 17-21, 2019
http://isscc.org

FPGA'19 – ACM/SIGDA Int'l Symposium on Field-Programmable Gate Arrays
Seaside, CA
Feb 24-26, 2019
http://www.isfpga.org

ISQED'19 - Int'l Symposium on Quality Electronic Design
Santa Clara, CA
Mar 6-7, 2019
http://www.isqed.org

DATE'19 - Design Automation and Test in Europe
Florence, Italy
Mar 25-29, 2019
http://www.date-conference.com

ISPD'19 – ACM Int'l Symposium on Physical Design
Bay area, CA
Apr 14-17, 2019
http://www.ispd.cc

HOST'19 – IEEE Int'l Symposium on Hardware-Oriented Security and Trust
Tysons Corner, VA
May 6-10, 2019
http://www.hostsymposium.org

ISCAS'19 – IEEE Int'l Symposium on Circuits and Systems
Sapporo, Japan
May 26-29, 2019
http://iscas2019.org

Back to Contents

Funding Opportunities

'"North America"'

Keck Foundation
Deadline: various
http://www.wmkeck.org/grant-programs/research/

USDA Foundational Program
Deadline: various
http://www.grants.gov/web/grants/view-opportunity.html?oppId=283836

NATO: Science for Peace and Security
Deadline: Proposals accepted anytime; reviews take place February 1 and May 15
http://www.nato.int/cps/en/natolive/87260.htm

Air Force Research Laboratory: Research Collaboration Program (BAA-RQKM-2013-0005)
Deadline: open to December 20, 2017
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=212295

Federal Aviation Administration Grants for Aviation Research (FAA-12-01)
Deadline: open to December 2019
http://www07.grants.gov/search/search.do?&mode=VIEW&oppId=134953

AFRL RD/RV University Cooperative Agreement
Deadline: open to Nov 23, 2020
http://www.grants.gov/web/grants/view-opportunity.html?oppId=280237

NASA Fellowship Programs
Deadline: Various
http://science.nasa.gov/researchers/sara/fellowship-programs/

Natural Sciences and Engineering Research Council of Canada
Deadline: Various
http://www.nserc-crsng.gc.ca/Students-Etudiants/PG-CS/index_eng.asp

itacs Accelerate PhD Fellowship: Ontario Business Grants Program
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/...

Collaborative Research and Development Grants
(including DND/NSERC Research Partnership Grants)
http://www.nserc-crsng.gc.ca/Professors-Professeurs/RPP-PP/CRD-RDC_eng.asp

Natural Sciences and Engineering Research Council of Canada
Deadline: Various

http://www.nserc-crsng.gc.ca/Professors-Professeurs/CFS-PCP/index_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Engage-Mobiliser_eng.asp
http://www.nserc-crsng.gc.ca/Innovate-Innover/Collaborate-Collaborer_eng.asp
Research and Development Funding for Business Innovation (Multiple Organizations)
Deadline: Various
http://www.mentorworks.ca/what-we-offer/government-funding/research-development/

'''Europe'''

Horizon 2020
Deadline: Various
http://goo.gl/geBouC

German Academic Exchange Service (DAAD)
Deadline: Various
https://www.daad.org/scholarship

German Research Foundation (DFG)
Deadline: Various
http://www.dfg.de/en

Helmholtz Association
Deadline: Various
https://www.helmholtz.de/en

Leibniz Association
Deadline: Various
http://www.leibniz-gemeinschaft.de/en/home

Leopoldina
Deadline: Various
https://www.leopoldina.org/en/about-us

ax Planck Society
Deadline: Various
https://www.mpg.de/en

Swiss National Science Foundation
Deadline: Various
http://www.snf.ch/en/

'''Asia'''

Korea:

National Research Foundation of Korea
Deadline: Various
http://www.nrf.re.kr/nrf_eng_cms/show.jsp?show_no=90&check_no=89&c_relation=0&c_...

China:

National Natural Science Foundation of China
Deadline: Various
http://www.nsfc.gov.cn/publish/portal1/

Singapore:

National Research Foundation (NRF) Singapore
http://www.nrf.gov.sg
RIE 2020 plan
Deadline: Various
http://www.nrf.gov.sg/rie2020

India:

inistry of Electronics and Information Technology
Deadline: Various
http://meity.gov.in/content/research-development

Department of Science and Technology (Nano Mission)
Deadline: Various
http://nanomission.gov.in/

University Grants Commission
Deadline: Various
http://www.ugc.ac.in/

inistry of Education Academic Research Fund
Deadline: Various
https://www.olga.moe.gov.sg/default.aspx

Agency for Science Technology and Research (A*STAR) Science and Engineering Research Council (SERC)
Deadline: Various
https://www.a-star.edu.sg/Research/Funding-Opportunities/Grants-Sponsorship.aspx

ultiple Funding
Deadline: Various
http://www.computerscienceonline.org/cs-scholarships/

'"Oceania/Polynesia"'

Polynesian Cultural Center (Hawaii) - International Student Scholarship Program
For studying in BYU Hawaii
http://www.polynesia.com/students.html

New Zealand:

inistry of Business, Innovation and Employment
Deadline: Various
http://www.mbie.govt.nz/

Australia:

Premier's Research and Industry Fund
Deadline: Various
http://www.statedevelopment.sa.gov.au/science/premiers-research-and-industry-fun...

Australian Research Council
Deadline: Various
http://www.arc.gov.au

'"South America"'

Brazil:

Coordination for the Improvement of Higher Education Personnel (CAPES)
Deadline: Various
http://www.iie.org/programs/capes#.WAu2kJMrJPM

inistry of Science, Technology, Innovation and Communications (CNPq)
Deadline: Various
http://www.cnpq.br/

'"Africa"'

Other scholarships for African Students (list of over 30 different scholarships)
Deadline: Various
http://www.afterschoolafrica.com/12264/list-annual-engineering-scholarships-afri...

Nigeria:

Bilateral Education Agreement (BEA) Awards (both Undergraduate and Post Graduate)
Deadline: Nomination interview - March'17
http://www.fsb.gov.ng/index.php/scholarship/menu-styles/bilateral-agreement

Federal Scholarship Board
Deadline: Various
http://www.fsb.gov.ng/index.php

Back to Contents

ACM TODAES: A New Page Limit Policy

ACM TODAES new page limit policy update: now 35 pages.

ACM TODAES has been updated the page limit policy to 35 pages, which was previously 25 pages. The new page limit policy is to help authors submit extended versions of 6 to 10 page conference papers and also include more experimental results and more comprehensive reference lists. Papers longer than 35 pages can be published when the Editorial Board approves. In addition, ACM TODAES Editorial Board also accepts survey papers and keynote papers longer than 35 pages.

For your information, ACM TODAES became a bimonthly journal (6 issues in a year) from January 2018. ACM TODAES welcomes your timely special issue (section) proposals.

We look forward to having your quality submissions to ACM TODAES.
Back to Contents

Notice to Authors

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
Circulation: 2,700