



The University Booth

The University Booth features state-of-the-art demonstrations of projects by university researchers and DAC authors. Both EDA, as well as design and instructional demonstrations are featured. At the Vendor Corner DAC exhibitors provide information on their discounted university hardware and software programs.

Booth Activities

- **SVC** - The Stanford Validity Checker presented in Paper 32.1 "A Decision Procedure for Bit-Vector Arithmetic" will be demonstrated. Tuesday 11:00 to 12:00.
- **UCLA** - Paper 43.2 "Delay-Optimal Technology Mapping for FPGAs with Heterogeneous LUTs" will be demonstrated using a JAVA based interface to a C language implementation for delay and area minimization. Monday to Wednesday 10:00 to 11:00.
- **University of Pittsburgh** - A CAD tool to model and simulate free space opto-electronic systems will be presented. Monday, Tuesday 10:00 to 11:00. Wednesday 2:00 to 3:00.
- **University of Pittsburgh** - Model abstraction techniques to improve the performance of formal verification tools based on the behavioral semantics of VHDL models will be presented. Daily 11:00 to 12:00.
- **UMBC** - Defect detection and failure analysis in digital devices by transient signal analysis is presented. Daily 1:00 to 2:00.
- **Chinook** - A development environment for distributed embedded systems from the University of Washington will be presented.
- **SiMPA** - DAC paper 7.2 and the UCLA developed SiMPA DSM Design Flow will be presented. Tuesday 11:00 to 12:00, Wednesday 3:00 to 4:00.
- **JavaTime** - High-level design of heterogeneous systems using the Java language. Daily 12:00 to 2:00.
- **Video Signal Processor AxPe1280V** - The University of Hannover Germany will demonstrate the AxPe1280V and its software development toolkit. University Design Contest entry and DAC paper 3.2. Daily 4:00 to 5:00.
- **HiPAR-DSP Video Signal Processor** - The University of Hannover Germany will demonstrate the HiPAR-DSP video signal processor and its software toolkit. University Design Contest entry and DAC paper 3.3. Daily 4:00 to 5:00.
- **Case Western** - A high level test synthesis system will be demonstrated. Monday 4:00 to 5:00.
- **MEMS Synthesis and Extraction** - Prototype tools that translate engineering design specifications into a MEMS layout and that extract a lumped parameter schematic and SPICE level view from the traditional layout and finite element view will be demonstrated by CMU. Monday, Tuesday 11:00 to 12:00.
- **RF floorplanning** - CMU will demonstrate a geometric algorithm based tool capable of solving early RF floorplanning problems. Monday, Tuesday 1:00 to 2:00.
- **University of North Texas** - The author of paper 13.1 "A Fast Hierarchical Algorithm for 3-D Capacitance Extraction" will be available for discussion. Wednesday 11:00 to 12:00.
- **University of Cincinnati** - The VHDL-AMS (VHDL 1076.1) simulator will be demonstrated. Daily 2:00 to 3:00.
- **University of Toronto** - An 8-processor version of the NUMA-machine Multiprocessor will be demonstrated. The NUMAchine is a University Design Contest entry and DAC paper 3.6S. Daily 4:00 to 5:00.
- **Vela (the sail of 'Argo Navis')** - A collaborating team constellation in a globally distributed microsystem design project will be demonstrated. Daily 11:00-1:00.
- **JavaCADD** - A Java-based server and client developed by Mississippi State University for distributed ECAD services. Daily 11:00 to 1:00.
- **Tufts University** - A Xilinx based FPGA microprocessor including ALU, RAM, ROM, and registers implemented using Viewlogic Workview Office and Xilinx Alliance will be presented. Daily 10:00 to 11:00 and 3:00 to 4:00.
- **UC Irvine** - Presentation of behavioral timed decision tables for the pre-synthesis optimizations of HDL code. Monday 11:00 to 12:00, Tuesday and Wednesday 3:00 to 4:00.
- **UCLA** - University Design Contest winner and DAC paper 3.1 on "Design Methodology Underlying a Single-Chip CMOS 900 MHz Spread-Spectrum Wireless Transceiver" will be presented. Tuesday 5:00 to 6:00, Wednesday 11:00 to 12:00.
- **BISRAMGEN** - A generator for embedded SRAMs with SEU-hard and stable cell design, built-in self-test and self-repair, and other advanced features suitable for submicron and deep-submicron applications will be demonstrated. Daily 3:00 to 4:00.
- **QSPICE** - A version of SPICE containing models of nonlinear quantum electronic devices and improved convergence routines for efficient DC and transient simulation will be demonstrated. Daily 3:00 to 4:00.
- **MINIMALIST** - An environment developed at Columbia University for the synthesis and verification of burst-mode asynchronous machines will be demonstrated. Times TBA.
- **Georgia Tech** - Demonstrations of video games, state machines, and simple computers containing a logic analyzer and CPLD generated VGA video graphics and keyboard input on an Altera UP1 board will be presented. Daily at 11:00 and 2:00.
- **Vendor Corner** - EDA companies at the Vendor Corner include ALDEC, ACELL Technologies, Altera, Cadence, Cypress Semiconductor, Mentor Graphics, Model Technology, Synopsys, Tanner Research, and Xilinx. Daily 10:00 to 6:00.
- **Cadence** - A representative will be at the vendor corner to discuss their university program. Monday 10:00 to 11:00 and 1:00 to 2:00, Tuesday 1:00 to 2:00.
- **Synopsys** - A representative will be at the vendor corner to discuss their university program. Daily from 2:00 to 3:00, and Monday 11:00 to 12:00, Tuesday and Wednesday 10:00 to 11:00.

