

Call for Papers

The 18th International Workshop on Logic & Synthesis (IWLS)

July 31 – August 2, 2009

Cadence Research Laboratories
Berkeley, CA

www.iwls.org

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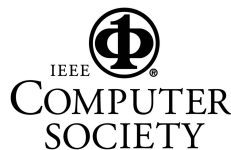
The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop accepts complete papers as well as abstracts, highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

Topics of interest include (but are not limited to): synthesis and optimization; power and timing analysis; testing and verification; architectures and compilation; and design experiences. Submissions on modeling, analysis and synthesis for emerging technologies and platforms are particularly encouraged.

Both complete papers as well as extended abstracts highlighting new problems and new topics of research are welcomed. (Only original and previously unpublished material is permitted.) Submissions must be no longer than 8 pages, double column, 10-point font. Accepted papers are distributed only to IWLS participants. The workshop format includes paper presentations, posters, invited talks, social lunch and dinner gatherings, and recreational activities.

Submissions are made electronically through the EDAS system. Please see the website for instructions: <http://www.iwls.org>

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Submission deadline (extended)	May 15, 2009 (<i>Midnight EST</i>)
Notification of acceptance	May 29, 2009
Final version due	June 19, 2009

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