

FINAL PROGRAM

15th International Workshop on Logic & Synthesis IWLS 2006

**Vail Cascade Resort & Spa
Vail, Colorado, USA**

June 7-9, 2006

Wednesday, June 7

12:00-5:00	REGISTRATION (Cascade Ballroom Foyer)
12:00-1:00	LUNCH (Mountain View Room)
1:00 - 3:00 Synthesis Chair: Michel Berkelaar	Factor Cuts <i>S. Chatterjee, A. Mishchenko, R. Brayton</i>
	Integrated Logic Synthesis Using Simulated Annealing <i>P. Farm, E. Dubrova, A. Kuehlmann</i>
	Scalable Logic Synthesis using a Simple Circuit Structure <i>A. Mishchenko, R. Brayton</i>
	Generalized Buffering of PTL Logic Stages using Boolean Division and Don't Cares <i>R. Garg, S. Khatri</i>
3:00-3:15	Two-Minute Poster Presentations
3:15 - 4:00 Coffee Break & Poster Session 1 (Cascade Ballroom Foyer)	Efficient Techniques for Large BDDs <i>K. Shinozuka</i>
	Boolean Function Minimization: The Information Theoretic Approach <i>J. Safaei, H. Beigy</i>
	Stochastic Programming Based Optimization Framework in Presence of Variability <i>V. Khandelwal, A. Srivastava</i>
	Performance Analysis of the Asynchronous Nonlinear Pipeline using the Max-Plus Algebra <i>J. Ruan, L. Wang, Z. Wang, K. Dai</i>
	An Approximate Method by Queuing Network Modeling for Performance Evaluation of Asynchronous Pipeline Rings <i>L. Wang, Z-Y. Wang, K. Dai</i>
	A Low Power Overhead Bus Coding Technique for Minimizing Inductive Crosstalk in VLSI Interconnects <i>K. S. Sainarayanan, J. V. R. Ravindra, M. B. Srinivas</i>
4:00 - 5:30 Physical Issues Chair: Christoph Albrecht	Design and Analysis of "Tree + Local Meshes" Clock Architecture <i>G. Wilke, R. Murgai</i>
	An Improved Sliding Window Scheme for Clock Mesh Analysis <i>S. Reddy, R. Murgai</i>
	Keeping Physical Synthesis Safe and Sound <i>K.-H. Chang, I. Markov, V. Bertacco</i>
5:30 - 7:00 IWLS Programming Challenge Chairs: Christoph Albrecht, Florian Krohm, Robert Brayton, Valavan Manohararajah	Introduction to the OA Gear Func and Aig package <i>A. Hurst</i>
	State-dependent Leakage Minimization in OpenAccess <i>D. Chai</i>
	Fast Simulation and Equivalence Checking Using OAGear <i>K.-H. Chang, D. Papa, I. Markov, V. Bertacco</i>
	Graph Optimization by Simulated Annealing <i>P. Farm</i>
	SAT Sweeping with Local Observability Don't-Cares <i>Q. Zhu, N. Kitchen</i>
7:00-9:00	DINNER (Creekside Deck)

Thursday, June 8

8:00-5:00	REGISTRATION (<i>Cascade Ballroom Foyer</i>)
7:30-8:30	BREAKFAST (<i>Creekside Deck</i>)
8:30 - 10:00 High-Level Synthesis Chair: Marc Riedel	A Design Method of Address Generators Using Hash Memories <i>T. Sasao</i>
	Optimizing Fixed-Size Bit-Vector Arithmetic using Finite Ring Algebra <i>S. Gopalakrishnan, P. Kalla, F. Enescu</i>
	Protocol Wrapper Generation from Statement Based Specification <i>Y. Ishikawa, S. Watanabe, K. Seto, M. Fujita</i>
10:00-10:15	Two-Minute Poster Presentations
10:15 - 11:00 Coffee Break & Poster Session 2 (<i>Cascade Ballroom Foyer</i>)	A Fully Multiplexer-based Implementation of Redundant Number System <i>S. Veeramachaneni, P. Yarlagadda, M. Srinivas</i>
	Fast CMOS Logic Style Using Minimum Transistor Stack for Pull-up and Pull-down Networks <i>F. Schneider, R. Ribas, A. Reis</i>
	BDDs and transistor networks with minimum pull-up/pull-down chains <i>L. da Rosa Jr., F. Marques, T. Cardoso, R. Ribas, A. Reis</i>
	On prefix graph generation algorithm for binary addition under area-delay trade-off <i>T. Matsunaga, Y. Matsunaga</i>
	Analysis of Maximum Switching Activities in Sequential Circuits for Power Supply Integrity Validation <i>H. Higuchi</i>
	Automatic Protocol Transducer Synthesis aiming at facilitating IP-Reuse <i>S. Watanabe, K. Seto, Y. Ishikawa, S. Komatsu, M. Fujita</i>
11:00 - 1:00 Invited Session: New Directions for Logic Synthesis Chair: Marc Riedel	Engineering New Molecules for Programming Complex Cellular Systems <i>Prof. Christina Smolke, Caltech</i>
	Frequent Subgraph Mining Across Massive Biological Networks for Functional Discovery <i>Prof. Jasmine Zhou, USC</i>
	Synthetically Modified Structural Proteins: Self-Assembling Building Blocks for Nanoscale Materials <i>Prof. Matthew Francis, U. C. Berkeley</i>
1:00-2:00	LUNCH & Planning for IWLS2007 (<i>Creekside Deck</i>)
2:00-2:30	Refreshments to go
2:30-5:30	Social Activity: Hiking Trip
5:30-8:00	DINNER (<i>TBA</i>)

Friday, June 9

7:30-8:30	BREAKFAST (Creekside Room)
8:30 - 10:00 Verification 1 Chair: Mukul Prasad	Inductively Finding a Reachable State Space Over-Approximation <i>M. Case, A. Mishchenko, R. Brayton</i>
	Improvements to Combinational Equivalence Checking <i>A. Mishchenko, S. Chatterjee, R. Brayton, N. Een</i>
	Advances and Insights into Parallel SAT Solving <i>S. Plaza, I. Kountanis, Z. Andraus, V. Bertacco, T. Mudge</i>
10:00-10:15	Two-Minute Poster Presentations
10:15 - 11:00 Coffee Break & Poster Session 3 (Cascade Ballroom Foyer)	Design of a Reversible PLD Architecture <i>J.-J. Lee and G.-Y. Song</i>
	Reversible Logic Implementation of BCD Subtractor in IEEE 754r Format <i>H. Thapliyal, M. Srinivas</i>
	Synthesis of a Reversible Bit-Serial GF (2m) Systolic multiplier using a Novel Reversible Gate <i>R. Kamala, M. Srinivas</i>
	Design of Asynchronous Circuits on Top of Synchronous FPGAs <i>R. Mocho, G. Sartori, R. Ribas, A. Reis</i>
	On Automatic Synthesis of Data Dependent Micropipelines <i>A. Smirnov, M. Karpovsky, A. Taubin</i>
	A Compositional Approach to Symmetry Detection in Circuits <i>D. Chai, A. Kuehlmann</i>
11:00 - 12:30 Variability Chair: Andreas Kuehlmann	Variability Driven Gate Sizing for Binning Yield Optimization <i>A. Davoodi, A. Srivastava</i>
	Latch-Based Design under Process Variation <i>A. Hurst, R. Brayton</i>
	Efficient and Accurate Statistical Timing Analysis for Non-Linear, Non-Gaussian Variability With Incremental Attributes <i>A. Dobhal, V. Khandelwal, A. Srivastava</i>
12:30-1:30	LUNCH (Rocky Mountain Garden)
1:30 - 3:00 Verification 2 Chair: Michael Theobald	Design Error Detection in System-Level Designs by Dependence Analysis and Formal Checker <i>D. Ando, T. Nishihara, S. Sasaki, T. Matsumoto, M. Fujita</i>
	Verification after Synthesis <i>A. Mishchenko, R. Brayton</i>
	Improved Threshold Voltage Assignment via Combinatorial Implementation Selection <i>S. Ghiasi</i>