

Final Call for Papers

The 15th International Workshop on Logic & Synthesis (IWLS)

June 7 – 9, 2006

Vail Cascade Resort, Vail, Colorado
(Just before the ICCAD TPC Meeting)

www.iwls.org

General Chair
Victor Kravets
IBM T. J. Watson

Program Chair
Stephen A. Edwards
Columbia University

Panel Chair
Marc Riedel
University of Minnesota

Special Activities Chair
Alan Mishchenko
U. C. Berkeley

Publicity Chair
Mukul R. Prasad
Fujitsu Labs. of America

Programming Challenge
Christoph Albrecht
Cadence Berkeley Labs
Florian Krohm
IBM

The International Workshop on Logic and Synthesis provides an international forum for promoting research and exchanging ideas about all aspects of integrated circuit and system synthesis, optimization, and verification. The workshop encourages early dissemination of ideas and results. Accepted papers are distributed only to IWLS participants. *Note, that due to the delayed schedule of DAC this year, papers submitted to DAC 2006 are also eligible for submission as regular papers.*

Topics of interest include architectures and compilation, synthesis and optimization, power and timing analysis, design validation and verification, and design experiences, all applied at system description levels ranging from transistors to hardware-software interfaces. Implementation might be in synchronous or asynchronous CMOS, or any emerging technology. Submissions on modeling, analysis and tools targeting emerging technologies and platforms are particularly encouraged.

Authors may submit complete papers for their proposed presentation. These must be no longer than 8 pages, double column, and in a 10-point font. We also encourage submissions of extended abstracts in the early stages of research that highlight important new problems, perhaps without providing complete solutions. Only electronic submissions will be accepted: submit at <http://www.iwls.org>. For questions, contact IWLS_pchair@sigda.org. For travel grants, apply to ACM/SIGDA's travel grant program at <http://www.sigda.org/travelgrants.html>.

The workshop format includes paper presentations, posters, invited talks, social lunch and dinner gatherings, and recreational activities to further stimulate interaction among participants.

For the first time, the workshop includes a programming challenge sponsored by IEEE CEDA for students. The challenge is to implement one or more logic optimization algorithms on the industrial EDA database OpenAccess and to use the OA Gear infrastructure. A jury will select significant contributions which are awarded with travel grants and one cash prize. For more information, see <http://www.iwls.org/challenge/>

Sponsored by
ACM/SIGDA and the
IEEE Council on Electronic
Design Automation

Submission deadline for papers (<i>final</i>)	March 17, 2006 (Midnight EST)
Notification of acceptance	April 13, 2006
Final version due	April 27, 2006

Technical Program Committee

C. Albrecht, Cadence Berkeley Labs	A. Kuehlmann, Cadence Berkeley Labs
F. Aloul, American University in Sharjah	Y. Kukimoto, Extreme DA
M. Berkelaar, Magma Design Automation	D. Marculescu, Carnegie Mellon University
R. Brayton, University of California, Berkeley	I. Markov, University of Michigan
E. Dubrova, KTH, Sweden	A. Mishchenko, University of California, Berkeley
S. Edwards, Columbia University	S. Nowick, Columbia University
T. Givargis, University of California, Irvine	M. Prasad, Fujitsu Labs of America
M. Hutton, Altera	M. Riedel, University of Minnesota
E. Jacobs, Magma Design Automation	H. Savoj
T. Kam, Intel	S. Sinha, Synopsys
S. Khatri, Texas A&M University	C. Stangier, Magma Design Automation
J. Kim, Intel	M. Theobald, Carnegie Mellon University
V. Kravets, IBM T. J. Watson	T. Villa, Universita di Udine/PARADES, Italy
P. Kudva, IBM T. J. Watson	H. Zhou, Northwestern University

