

2005 International Symposium on Physical Design



Marines' Memorial Club & Hotel, San Francisco, CA
April 3-6, 2005
www.ispd.cc



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PROGRAM

The International Symposium on Physical Design provides a high-quality forum for the exchange of ideas on the physical layout design of VLSI systems. The scope of this symposium includes all aspects of physical design, from high-level interactions with logic synthesis, down to back-end performance analysis and verification.

Long presentations (marked L) run 25 minutes. Short presentations are 20 minutes.

SUNDAY, APRIL 3

5:30 – 7:00 pm Evening Reception

MONDAY, APRIL 4

8:30 – 9:40 am Welcome and Keynote Address

Host: Patrick Groeneveld / Eindhoven University

The Death of Logic Synthesis

Rajeev Madhavan / Chairman and CEO, Magma Design Automation

9:40 – 10:00 am Morning break

10:00 - 12:00 am Session 1: Routing Techniques

Chair: Raymond Nijssen / Magma

A Diagnostic Method for Detecting and Assessing the Impact of Physical Design Optimizations on Routing

Robert Lembach, Rafael A. Arce-Nazario, Donald Eisenmenger, Cory Wood/IBM

An Efficient Tile-Based ECO Router with Routing Graph Reduction and Enhanced Global Routing Flow

Jian-Yin Li, Yih-Lang Li/National Chiao Tung University

Routing of Analog Busses with Parasitic Symmetry

Lars Schreiner, Markus Olbrich / Hannover, Erich Barke, Volker Meyer-zu-Bexten / ATMEL

Coupling Aware Timing Optimization and Antenna Avoidance in Layer Assignment (L)

Di Wu, Jiang Hu and Rabi Mahapatra/Texas A&M

Fast and Accurate Rectilinear Steiner Minimal Tree Algorithm for VLSI Design

Chris Chu / Iowa State University, Yiu-Chung Wong / Rio Design Automation

A Global Routing Method for 2-Layer Ball Grid Array Packages
Yukiko Kubo/Kitakyushu and Atsushi Takahashi/Tokyo Institute of Technology

12:05 – 1:30 pm Lunch

1:30 – 3:15 pm Session 2: Geometric Programming and Clocks

Chair: Andrew B. Kahng / UCSD

Tutorial: "Geometric Programming" (Invited)

Stephen Boyd / Stanford

Delay Insertion Method in Clock Skew Scheduling (L)

Baris Taskin and Ivan Kourtev/Univ. of Pittsburgh

Improved Algorithms for Link Based Nontree Clock Networks for Skew Variability Reduction

Anand Rajaram, David Z. Pan/UT Austin, Jiang Hu/Texas A&M

3:15 – 3:45 pm Afternoon break

3:45 – 5:30 pm: Session 3: Power, Buffering and Open Source

Chair: Charlie Chen / National Taiwan University

Effects of On-Chip Inductance on Power Distribution Grid

Atsushi Muramatsu, Masanori Hashimoto and Hidetoshi Onodera / Kyoto Univ.

A Fast Algorithm for Power Grid Design

Jaskirat Singh, Sachin S. Sapatnekar / Minnesota

Simultaneous Buffer Insertion and Wire Sizing Considering Systematic CMP Variation and Random Leff Variation (L)

Lei He / UCLA, Andrew B. Kahng / UCSD, Kingho Tam, Jinjun Xiong

An Efficient Surface-Based Low-Power Buffer Insertion Algorithm (L)

Rajeev R. Rao, David Blaauw, Dennis Sylvester / Michigan, Chuck Alpert, Sani Nassif / IBM Austin

Early Research Experience With OpenAccess Gear: an Open Source Development Environment for Physical Design

Zhong Xiu/CMU, David A. Papa/Michigan, Philip Chong, Christoph Albrecht, Andreas Kuehlmann

/Cadence, Rob A. Rutenbar/CMU, Igor Markov/Michigan (15 minutes)

6:30 – 9:30 pm: Dinner Banquet
Dinner Speaker: Gary Smith / Dataquest

TUESDAY, APRIL 5

8:30 – 10:00 am Session 4: Keynote and Tutorial on the History and Future of Physical Design (Invited)
Chair: Desmond Kirkpatrick / Intel

Challenges of Analog/Mixed-Signal SoC Design and Verification
Jue-Hsien Chern / VP and General Manager of Deep Submicron Division, Mentor Graphics

Tutorial on DFM for physical design
Andrzej Strojwas / CMU & PDF Solutions

10:05 – 10:35 pm Morning break

10:35 – 12:00 am Session 5: Floorplanning
Chair: Jason Cong / UCLA

Modern Floorplanning Based on Fast Simulated Annealing
Tung-Chieh Chen and Yao-Wen Chang / Nat. Taiwan University

Multi-Bend Bus Driven Floorplanning
Jill H.Y.Law, Evangeline F.Y.Young / CU HongKong

Floorplan Assisted Data Rate Enhancement through Wire Pipelining: A Real Assessment
Mario R. Casu / Politecnico di Torino, Italy Luca Macchiarulo / University of Hawaii at Manoa

Are Floorplan Representations Important for Digital Design? (I)
Hayward H. Chan, Saurabh N. Adya and Igor L. Markov / Michigan

12:00 pm – 1:30 pm Lunch

1:30 – 2:35 pm Session 6: Technology Mapping
Chair: Xiaojian Yang / Synplicity

An Efficient Technology Mapping Algorithm Targeting Routing Congestion under Delay Constraints (I)
Rupesh S. Shelar, Prashant Saxena /Intel, Xinning Wang, Sachin S. Sapatnekar / Minnesota

Wire Length Prediction-Based Technology Mapping and Fanout Optimization
Qinghua Liu, Malgorzata Marek-Sadowska / UCSB

Mapping Algorithm for Large-Scale Field Programmable Analog Array
I. Faik Baskaya, Sasank Reddy, Sung Kyu Lim, Tyson Hall and David Anderson/Georgia Tech

2:35 – 2:50 pm Afternoon break 1

2:50 – 3:55 pm Session 7: Advanced Techniques & Technologies
Chair: Margaret Marek-Sadowska /UCSB

Fast Interval-Valued Statistical Interconnect Modeling and Reduction (L)
James D. Ma, Rob A. Rutenbar / CMU

Thermal Via Placement in 3-D ICs
Brent Goplen, Sachin S. Sapatnekar / Minnesota

Technology Migration Technique for Designs with Strong Ret-Driven Layout Restrictions
Xin Yuan, Kevin W. McCullen, Fook-Luen Heng, Robert F. Walker, Jason Hibbeler, Robert J. Allen, Rani R. Narayan / IBM

3:55 – 4:15 pm Afternoon break 2

4:15 – 5:30 pm Session 8: Physical Synthesis (invited)
Chair: Patrick H. Madden / Binghamton & Kitakyushu

Insights and Perspectives on Physical Synthesis
Shankar Krishnamoorthy / Sierra Design Automation

Physical Design Tools for Hierarchy
Paul Villarrubia / IBM

WEDNESDAY, APRIL 6

8:30 – 10:00 am Session 9: Placement
Chair: Igor Markov / Michigan

Multilevel Generalized Force-Directed Method for Circuit Placement (L)
Tony Chan, Jason Cong, Kenton Sze / UCLA

Unified Quadratic Programming Approach for Mixed Mode Placement (L)
Bo Yao, Chung-Kuan Cheng, Lung-Tien Liu, Nan-Chi Chou/UCSD

A Semi-Persistent Clustering Technique For Vlsi Circuit Placement
Charles Alpert, Andrew B. Kahng / UCSD, Gi-Joon Nam, Sherief Reda, Paul Villarrubia / IBM

Evaluation of Placer Suboptimality via Zero-Change Netlist Transformations
Andrew B. Kahng and Sherief Reda /UCSD

10:00 – 10:30 am break

10:30 – 12:20 am Session 10: 2005 ISPD Placement Contest
Organizer and chair: Gi-Joon Nam/IBM

ISPD05 Placement Contest and Benchmark Suite
Gi-Joon Nam, IBM

Individual placer presentations:

1. **FastPlace**, Chris Chu, Natarajan Viswanathan, Min Pan / Iowa State University
2. **Capo**, Jarrod Roy, David Papa, Saurabh Adya, Hayward Chan, Aaron Ng, James Lu, Igor Markov / University of Michigan
3. **mPL**, Tony Chan, Jason Cong, Michalis Romesis, Joseph Shinnerl, Kenton Sze and Min Xie / UCLA
4. **Feng Shui**, Ameya R. Agnihotri, Satoshi Ono, Patrick H. Madden / Binghamton
5. **Aplace**, Qinke Wang, Andrew B. Kahng, Sherief Reda / UCSD
6. **NTUPlace**, Tung-Chieh Chen, Tien-Chang Hsu, Zhe-Wei Jiang, Yao-Wen Chang / National Taiwan University
7. **mFar**, Bo Hu, Yue Zeng, Margaret Marek-Sadowska / UCSB
8. **KraftWerk**, Bernd Obermeier, Hans Ranke, Frank M. Johannes / Technical University of Munich
9. **Dragon2005**, Taraneh Taghavi, Xiaojian Yang, Bo-Kyung Choi / UCLA

Announcement of Results, Gi-Joon Nam

12:20 – 12:30 pm Closing Remarks

SYMPOSIUM REGISTRATION

Please register on-line at <http://www.ispd.cc> by **March 16th, 2005** for the early registration discount rates.

HOTEL ACCOMODATIONS AND TRAVEL

ISPD 2005 is being held at the Marines' Memorial Club & Hotel in downtown San Francisco, located at:

609 Sutter Street,
San Francisco, CA 94102,
USA
Tel: +1 415-673-6672 or 800-562-7463
Fax: +1 415-441-3649
Email: reservations@marineclub.com
Http://www.marineclub.com

Please use phone, fax or email to make a reservation. Ask for the special ISPD room rate in order to book in our room block. The room rate for a Standard room is: \$139 per night; the room rate for a Deluxe room is: \$154 per night (+applicable taxes). To get the special rate you must book by Wednesday, March 2, 2005.

San Francisco International Airport (SFO) is near. We advise the use of shuttle buses (approx. \$14) for ground transportation instead of a rental car.

Tip: Reserve early to give yourself the best chance of getting a room

Symposium Organization

General Chair	Patrick Groeneveld / Eindhoven University	
Past Chair	Charles J. Alpert/ IBM	
Steering Committee	Charles J. Alpert/ IBM (chair), David Blaauw / Michigan, Jason Cong / UCLA, Desmond Kirkpatrick / Intel, Martin Wong / UIUC	
Technical Program Chair	Lou Scheffer / Cadence	
Technical Program Committee		
Charlie Chen/NTU	Jiang Hu/Texas A&M	Andrew B. Kahng /UCSD
Patrick H. Madden/Binghamton	Margaret Marek-Sadowska/UCSB	Igor Markov / Michigan
Gi-Joon Nam/IBM	Raymond Nijssen/Magma	David Z. Pan / UT Austin
Prashant Saxena/Synopsys	Narendra Shenoy/Synopsys	Janet M. L. Wang /Arizona
Xiaojian Yang/Synplicity	Hai Zhou/Northwestern	
Publication Chair	Patrick H. Madden/ Binghamton & Kitakyushu	
Publicity Chair/Webmaster	David Z. Pan/ UT Austin	
Arrangements & support	Stephanie Shaffer / Shaffer & Associates Event Management	