

ON-CHIP CROSSTALK EVALUATION BETWEEN ADJACENT INTERCONNECTIONS

G. SERVEL, D. DESCHACHT

Laboratoire d'Informatique, de Robotique et de Microélectronique,
U.M.R. C.N.R.S. 5506
161, rue ADA, 34392 Montpellier Cedex 5, France.
e-mail : servel@lirmm.fr

ABSTRACT

With the reduction of distances between wires in deep sub-micron technologies, coupling capacitances are becoming significant. These increasing of capacities cause noises capable of propagating a logical fault. A bad evaluation of the crosstalk could be at the origin of a malfunction of the circuit. In this paper we propose a new closer form expression for the crosstalk between two, three and five lines. Results given by our expression will be compared to simulations with SPICE in technology 0.25 μm .

1. INTRODUCTION

The passage to sub-micron technologies increases effects of coupling in interconnections [1]. Indeed, in technologies greatly sub-micron, capacities of coupling between lines reach values so that we can't be indifferent to the amplexness of the noise due to this coupling [2].

Several factors bound to the technology contribute to the increase of crosstalk problems: the increase of the number of metal layers [3], the increase of the line thickness, the density of integration and the reduction of the spacing between lines.

Effects of the crosstalk can provoke a dysfunction of an embedded circuit therefore very well to the temporal level while increasing the delay of the line that commutes, either to the logical level while provoking a commutation owed to a too important crosstalk.

Especially for an on-chip bus crosstalk noise is a serious problem for VLSI design. In bus structure, crosstalk immunity is more important because long interconnect wires often run together and in parallel.

Recent models as [4], [5] propose some complex models of prediction of crosstalk requiring some complex calculations, then important calculation time. Other model [6], don't take in account the equivalent driver resistance. At last, some more ancient models [7] don't correspond to requirements of sub-micron technologies.

In this paper we will first determine the worst-case, that is to say the input transition leading to the most important crosstalk voltage. Then, we will propose a formulation of this voltage for one, two and four adjacent lines. This formulation takes interconnect

capacitances, line resistance and their distributed nature, driver resistance and the variable strengths of the drivers driving coupled lines, into account. An analytical expression for two and four adjacent lines are given for the first time in our knowledge. Based on a simplified one cell modeling, a corrective term must be added to take the distributed RC model into account. In the last part, we will compare the influence of adjacent lines number on crosstalk amplitude.

2. DETERMINATION OF THE WORST CASE

In the case of two lines with inverters as drivers and loads (Fig. 1), the line 1 being the aggressor (the line who commutes) and the line 2 the victim (the line with potential stationary), the input V_{in1} can be either an positive pulse or a negative pulse. In the same way, the line victim can be at the potential V_{DD} or Gnd.

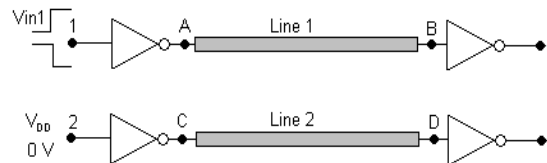


Fig. 1 : Case of one adjacent line

The results of HSPICE simulations are presented in the Table 1 for two lines of 2 mm. The driver and loading inverters are respectively the same in the four cases of commutation. ΔV_C , and ΔV_D are the noise voltage induced by the coupling at the beginning and end of the line (points C and D of Fig. 1).

	Case 1	Case 2	Case 3	Case 4
V_{in1}	0 to V_{DD}	0 to V_{DD}	V_{DD} to 0	V_{DD} to 0
V_{in2}	0	V_{DD}	0	V_{DD}
ΔV_C (mV)	-430	-190	300	130
ΔV_D (mV)	-920	-700	610	490

Table 1 : Crosstalk for one adjacent line

Simulations with SPICE show that when V_{in1} changes from 0 to V_{DD} and V_{in2} is at V_{DD} , the noise voltage induced on the victim line is more important than in the other cases.

3. DETERMINATION OF CROSSTALK FOR TWO LINES

We consider two parallel coupled interconnects with drivers and loads attached (Fig. 1). We apply the L model for the interconnect and compute both the peak noise voltage as shown in Fig. 2.

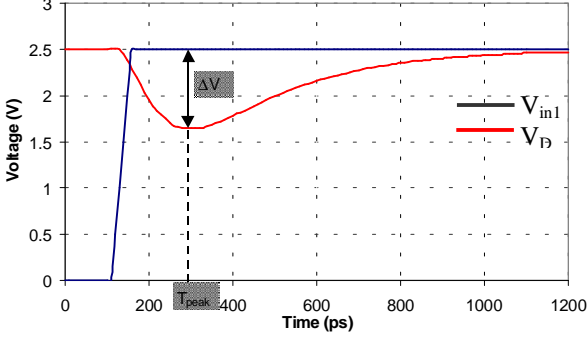


Fig. 2 : Dynamic noise voltage characteristic

We use Fig. 3 as the equivalent circuit for analysis purposes. R_{L1} and R_{L2} are total resistance of aggressor and victim lines. R_{inv1} and R_{inv2} are driver on-resistance of aggressor and victim lines. C_{10} and C_{20} are ground capacitances between aggressor and victim lines, and C_{12} is coupling capacitance between aggressor and victim lines. C_{L1} and C_{L2} are the equivalent load capacitances of the loading inverters. In this section, we are interested in studying the variation of victim wire crosstalk as a function of aggressor and victim line, and drivers of lines.

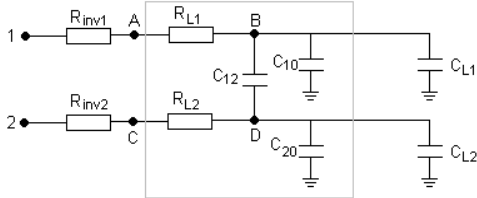


Fig. 3 : L Model for lines

We are interested in studying the variation of victim wire crosstalk at the beginning and the end of the line, and the variation of the time where the peak noise appeared. We are in the worst case, the node 1 commutes from V_{DD} to 0 and the node 2 is at V_{DD} . For solve the equations, we use Laplace transforms. Then, following expressions for voltages at node C and D are:

$$\frac{V_c(s)}{V_1(s)} = \frac{R_{inv2}}{R_2} \cdot \frac{s}{a_1 \cdot s^2 + b_1 \cdot s + c_1}$$

$$\frac{V_D(s)}{V_1(s)} = \frac{s}{a_1 \cdot s^2 + b_1 \cdot s + c_1}$$

where :

$$a_1 = \frac{R_1 \cdot C_{10} \cdot C_{20}}{C_{12}} + R_1 \cdot C_{10} + R_1 \cdot C_{20},$$

$$b_1 = \frac{C_{20}}{C_{12}} + 1 + \frac{R_1 \cdot C_{10}}{R_2 \cdot C_{12}} + \frac{R_1}{R_2}, \quad c_1 = \frac{1}{R_2 \cdot C_{20}},$$

$$R_1 = R_{inv1} + R_{L1}, \quad R_2 = R_{inv2} + R_{L2}.$$

The input signal at aggressor wire can be expressed as

$$V_1(s) = V_{DD} \cdot \left(\frac{1}{s} - \frac{1}{s} \cdot e^{-t_0 \cdot s} \right)$$

and the node at the input of victim line is to V_{DD} .

We obtain after inverse Laplace transforms the voltage at the begin and the of the victim line in time-domain.

$$V_c(t) = \frac{R_{inv2}}{R_2} \cdot \frac{V_{DD}}{\sqrt{\Delta}} \cdot \left\{ e^{s' \cdot t} - e^{s'' \cdot t} \right\} - \left[e^{s' \cdot (t-t_0)} - e^{s'' \cdot (t-t_0)} \right] + V_{DD}$$

$$V_D(t) = \frac{V_{DD}}{\sqrt{\Delta}} \cdot \left\{ e^{s' \cdot t} - e^{s'' \cdot t} \right\} - \left[e^{s' \cdot (t-t_0)} - e^{s'' \cdot (t-t_0)} \right] + V_{DD}$$

with :

$$\Delta = b_1^2 - 4 \cdot a_1 \cdot c_1, \quad s' = \frac{-b_1 + \sqrt{\Delta}}{2 \cdot a_1}, \quad \text{and} \quad s'' = \frac{-b_1 - \sqrt{\Delta}}{2 \cdot a_1}.$$

To find the peak noise we differentiate equation of $V_D(t)$ with respect to t and set the derivative to zero. The time at which peak noise is reached is :

$$t_{peak} = - \frac{\ln \left(\frac{s'' - \frac{s''}{e^{s'' \cdot t_0}}}{s' - \frac{s'}{e^{s' \cdot t_0}}} \right)}{s' - s''}$$

and the corresponding peaks noise at the begin of the line $V_c(t)$, and at the end of the line $V_D(t)$ are expressed as :

$$V_c(t_{peak}) = \frac{R_{inv2}}{R_2} \cdot \frac{V_{DD}}{\sqrt{\Delta}} \cdot \left\{ e^{s' \cdot t_{peak}} - e^{s'' \cdot t_{peak}} \right\} - \left[e^{s' \cdot (t_{peak}-t_0)} - e^{s'' \cdot (t_{peak}-t_0)} \right] + V_{DD}$$

$$V_D(t_{peak}) = \frac{V_{DD}}{\sqrt{\Delta}} \cdot \left\{ e^{s' \cdot t_{peak}} - e^{s'' \cdot t_{peak}} \right\} - \left[e^{s' \cdot (t_{peak}-t_0)} - e^{s'' \cdot (t_{peak}-t_0)} \right] + V_{DD}$$

$$\Delta V_c = V_{DD} - V_c(t_{peak}) \quad \Delta V_D = V_{DD} - V_D(t_{peak})$$

Table 2 presents the different configurations used for HSPICE simulations. W is the width of the wire, T the thickness, S the spacing between the two lines, H the oxide height and L is the length of the lines. W_{inv1} is the width of the inverter of the aggressor wire, and W_{inv2} the width of the inverter of the victim wire.

Cases	W (μm)	T (μm)	S (μm)	H (μm)	L (mm)	W _{inv1} (μm)	W _{inv2} (μm)
1	1	1	1	7.3	1	3	3
2	0.4	0.6	0.4	2.8	0.5	3	3
3	1	1	1	7.3	5	10	10
4	0.4	0.6	0.4	2.8	1	15	15
5	1	1	1	7.3	10	25	5
6	0.4	0.6	0.4	2.8	2	25	5
7	1	1	1	7.3	20	30	30

Table 2 : Configuration used for HSPICE simulations

To calculate the capacitance values, C_{10} , C_{20} and C_{12} , we use capacitance analytic formulas of Delorme [8]. The lines are in Al-Cu with $\rho=3.03^{E-08} \Omega.m$.

Table 3 shows the comparison of the simulated and calculated crosstalk. The simulations have been done with a sufficiently important number cell to reach a constant value. We can notice that in the cases 5, 6 and 7 (where $\frac{R_{inv1}}{R_{inv2} + R_L}$ is inferior to 0.3) the mistake

between calculated and simulated evaluation is important. Therefore in these cases where

$$\frac{R_{inv1}}{R_{inv2} + R_L} < 0.3, \text{ we must bring a correction.}$$

Cases	CALCULATED		HSPICE		$\epsilon V_D/V_{DD}$ (%)
	ΔV_C (mV)	ΔV_D (mV)	ΔV_C (mV)	ΔV_D (mV)	
1	-800	-820	-760	-770	2 %
2	-780	-810	-720	-740	2.8 %
3	-600	-810	-700	-870	-2.4 %
4	-560	-790	-530	-720	2.8 %
5	-750	-1000	-1000	-1250	-10 %
6	-830	-1070	-1050	-1250	-7.2 %
7	-130	-640	-280	-870	-9.2%

Table 3 : Comparison between HSPICE and calculated

Then, we add the corrective term in crosstalk evaluation at the calculation with one single cell :

$$\Delta V_{C2} = \Delta V_C \cdot (1 + \alpha_1) \quad \Delta V_{D2} = \Delta V_{D2} \cdot (1 + \beta_1)$$

$$\alpha_1 = \frac{-r_1 + 7}{12 \cdot r_1 + 2} \quad \beta_1 = \frac{0.28 \cdot r_2 - 1}{1.06 \cdot r_2 + 1}$$

$$r_1 = \frac{R_{inv1} + R_{inv2}}{R_L} \quad r_2 = \frac{R_{inv1} + R_{inv2} + R_L}{R_{inv1}}$$

Coefficients have been determined for the 0.25 μm technology. For the passage to a new technology, correction terms have the same form but it will be necessary to fit the coefficients.

Table 3 shows comparison between the new calculated and simulated crosstalk in the case where

$$\frac{R_{inv1}}{R_{inv2} + R_L} < 0.3 \cdot$$

Cases	CALCULATED		HSPICE		$\epsilon V_D/V_{DD}$ (%)
	ΔV_C (mV)	ΔV_D (mV)	ΔV_C (mV)	ΔV_D (mV)	
5	-830	-1210	-1000	-1250	-1.6 %
6	-890	-1270	-1050	-1250	0.8 %
7	-270	-770	-280	-870	-4 %

Table 4 : Comparison between HSPICE and calculated with correction

To validate this expression, we have simulated more than a hundred of different configurations, with a range

of wire length between 0.5 mm to 20 mm, and size of drivers between 3 μm and 30 μm for Metal 2 (cross section 0.24 μm^2) and Metal 5 (cross section 1 μm^2) geometry in technology 0.25 μm . Fig. 4 presents the difference between the amplitude of the peak noise with regard to V_{DD} simulated and calculated. In any case the error is less than 5%.

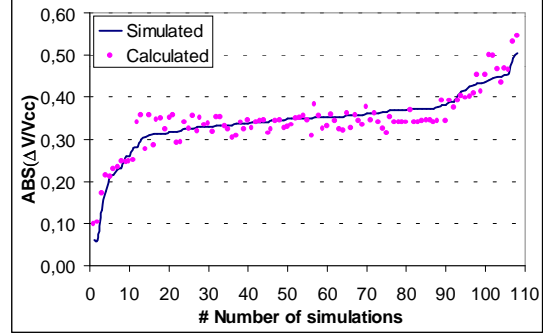


Fig . 4 : Crosstalk calculated and simulated

4. DETERMINATION OF CROSSTALK FOR THREE LINES

The determination of the crosstalk with a cell for three lines by an analytic method being too complex, we use an other corrective term. Again, we are in the worst case, the case where the aggressive lines commute from V_{DD} to 0 V and the line victim is to V_{DD} (Fig 5).

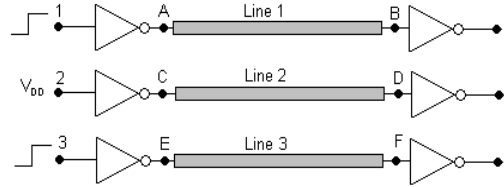


Fig . 5 : Case of two adjacent lines

Table 5 presents the differents configurations used for HSPICE simulations. W, T, S, H have the same values that in the case of two lines. W_{inv1} , W_{inv2} and W_{inv3} are the inverter's width of the victim wire.

Cases	W_{inv1} (μm)	W_{inv2} (μm)	W_{inv3} (μm)
1	3	3	3
2	3	3	2
3	10	10	10
4	15	15	15
5	25	5	5
6	25	5	25
7	30	30	30

Table 5 : Configuration used for HSPICE simulations

Therefore, we calculate the peak of crosstalk with a cell for two lines using the capacitance values of three lines. Next we apply the first corrective term (α_1 , β_1), then the second (α_2 , β_2).

$$\Delta V_{C3} = \Delta V_{C2} \cdot (1 + \alpha_2) \quad \Delta V_{D3} = \Delta V_{D2} \cdot (1 + \beta_2)$$

$$\alpha_2 = \left(\frac{1.8 \cdot r_3 - 70}{1.03 \cdot r_3} \right) \cdot (5.10^{-4} \cdot r_4 + 1) - 1$$

$$\beta_2 = \left(\frac{1.65 \cdot r_5 - 7.5}{0.95 \cdot r_5 + 10} \right) \cdot (-0.25 \cdot \ln r_6 + 1) - 1$$

$$r_3 = R_{inv2} \quad r_4 = R_{inv1} - R_{inv3}$$

$$r_5 = \frac{R_L \cdot R_{inv1}}{(R_{inv1} + R_{inv2})} \quad r_6 = \frac{R_L + R_{inv3}}{(R_L + R_{inv1})}$$

Table 6 shows comparison between the peak of crosstalk calculated and simulated.

Cases	CALCULATED		HSPICE		$\epsilon V_D/V_{DD}$ (%)
	ΔV_C (mV)	ΔV_D (mV)	ΔV_C (mV)	ΔV_D (mV)	
1	-1580	-1280	-1360	-1380	-4 %
2	-1140	-1120	-1180	-1200	-3.2 %
3	-1170	-1480	-1260	-1490	-0.4 %
4	-1010	-1380	-940	-1230	6 %
5	-1340	-1730	-1430	-1660	2.8 %
6	-1690	-2030	-1620	-1900	5.2 %
7	-400	-1460	-530	-1440	0.8 %

Table 6 : Comparison between HSPICE and calculated for 3 lines

As in the case of two lines, the error made on the evaluation of the crosstalk at the beginning and the end of line is less than 10%.

5. DETERMINATION OF CROSSTALK FOR FIVE LINES

To evaluate the peak of crosstalk in the case of five lines, we use the three lines method. We apply the capacitance values with five lines to calculation with three lines. Then, no one else correction is necessary. For simulations and calculations we calculated the capacitance values with ATLAS of SILCACO. Tables 7 shows the comparison between HSPICE and our calculation.

Cases	CALCULATED		HSPICE		$\epsilon V_D/V_{DD}$ (%)
	ΔV_C (mV)	ΔV_D (mV)	ΔV_C (mV)	ΔV_D (mV)	
1	-1790	-1400	-1560	-1570	-6.8 %
2	-1460	-1440	-1370	-1390	2 %
3	-1320	-1670	-1500	-1730	-2.4 %
4	-1080	-1470	-1100	-1370	4 %
5	-1510	-1950	-1730	-2010	-2.4 %
6	-1790	-2160	-1740	-1990	6.8 %
7	-430	-1620	-660	-1680	-2.4 %

Table 7 : Comparison between HSPICE and calculated We can see that the error is again less than 10%. Then, we notice that the crosstalk amplitude increases with the number of adjacent lines. In fact, for the same configuration the crosstalk increase of about 60% with

two adjacent lines and about 80% with four adjacent lines with regard to one adjacent line as shown in Fig. 6.

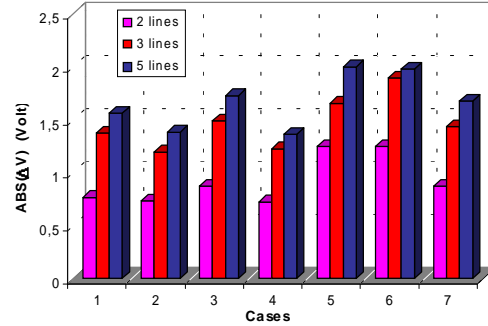


Fig . 6 : Crosstalk versus aggressors number

6. CONCLUSION

In this paper, we have presented a new simple closer form expression for the crosstalk amplitude between two, three and five lines. By comparing the results of our evaluations and SPICE simulations, we have demonstrated the excellent accuracy of the proposed model. Besides, our approach take into account of the variable strengths of the drivers driving coupled lines. Finally, we have verified and evaluated the increase of the crosstalk amplitude versus the number of adjacent lines. These analytical equations provide an estimate of the noise with an error less than 10% at the both lines extremities.

7. REFERENCES

- [1] L. Gal, "On-chip crosstalk-the new signal integrity challenge", IEEE Custom Integrated Circuits Conference, pp. 251-254, 1995.
- [2] Semiconductor Industry Association, "National Technology Roadmap for semiconductors", 1997.
- [3] S. Delmas-Bendhia, F. Caignet, E. Sicard, "On Chip Crosstalk Characterization on Deep Submicron Buses", IEEE International Caracas Conference on Devices, Circuits and Systems, 2000.
- [4] M. Kuhlmann, S.S. Sapatnekar, K.K. Parhi, "Efficient Crosstalk Estimation", IEEE Int. Conf. On Computer Design : VLSI in Computer & Processors, pp. 266-272, 1999.
- [5] A. B. Kahng, S. Muddu, D. Vidhani, "Noise and Delay Uncertainty Studies for Coupled RC Interconnects", IEEE Int. ASIC/SOC Conference, pp. 3-8, 1999.
- [6] A. Vittal, M. Marek-Sadowska, "Crosstalk Reduction for VLSI", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, NO. 3, pp. 290-298, March 1997.
- [7] T. Sakurai, "Closed-Form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSI's", IEEE Transactions on Electron Devices, Vol. 40, NO. 1, pp. 118-124, January 1993.
- [8] N. Delorme, M. Belleville, J. Chilo, "Inductance and capacitance analytic formulas for VLSI interconnects", IEEE Electronics Letters, Vol. 32, NO. 11, pp. 996-997, 23rd May 1996.