IN PROC. OF INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (ISCAS 2001)

# A LOW POWER SINUSOIDAL CLOCK

*Burkart Voss and Manfred Glesner*

Darmstadt University of Technology
Institute of Microelectronic Systems
D-64283 Darmstadt, Germany
*voss@mes.tu-darmstadt.de*

## ABSTRACT

This paper describes a low power clock distribution that utilizes sinusoidal clock waveforms and proposes registers that are able to cope with the overlapping clock edges. We can report power savings of 30% to 70% compared with conventional clocking schemes while maintaining traditional static CMOS design styles and logic levels.

## 1. INTRODUCTION

In today's large synchronous electronic systems, one major difficulty is the distribution of the clock signal, which can consume a major portion of the overall dissipated power (up to 50% in a microprocessor, see e.g. [Fre98]). Thus it is desirable for low power designs to reduce the power dissipation that is due to the clocking of the system. For the distribution of the clocks, two main techniques can be distinguished [WE93]:

- A single large buffer followed by the clocking network. It is used mainly to drive a global clock that feeds all modules.
- A distributed-clock-tree which is a tree of clock buffers with some suitable geometry. That approach is suitable for regular structures like data paths.

Considering a single large buffer followed by the clocking network as the clock distribution method, a large capacitance $C_L$ is seen by a large clock buffer. One way to reduce the power consumed in this buffer is to charge / discharge this large capacitance relatively slowly. When charging a capacitance with a constant current I (with a voltage ramp of length T), the dissipation through the channel resistance R is then [SFM$^+$85]:

$$\begin{aligned} E_{diss} &= P \cdot T = I^2 RT = \left(\frac{C_L V_{DD}}{T}\right)^2 RT \\ &= \left(\frac{RC_L}{T}\right) C_L V_{DD}^2 \qquad (1) \end{aligned}$$

If the energy that is stored on a capacitance is reused, systems are possible that consume considerably less energy for a charging/discharging cycle than the limit imposed by static CMOS ($\frac{1}{2}CV_{DD}^2$).

This is refered to as the principle of adiabatic charging. The term adiabatic is used to indicate that all charge transfer is done without generating heat. Different adiabatic logic styles have been developed until now (e.g. [ASK$^+$94, YK94, MONC97]). Those logic styles try to charge/discharge all capacitive nodes of a circuit and imply thus a relatively large overhead in terms of time and area. In this paper we propose to charge only the clocking network with its high capacitance adiabatically, thus making the overhead relatively small.

The constant current charging needed can be approximated using a sinusoidal power supply. To account for the then non-constant charge current, the dissipation of (1) must be multiplied by a constant shape factor $\xi$ (which takes the value $\frac{\pi^2}{8}$ for a sine-shaped current). Substituting $V_{DD}$ with the peak voltage of the power clock $\hat{V}_{pck}$ (1) becomes:

$$\begin{aligned} E_{diss} &= 2\xi \left(\frac{RC_L}{\frac{1}{2}T}\right) C_L \hat{V}_{pck}^2 \\ &= 4\xi \left(RC_L f\right) C_L \hat{V}_{pck}^2 \qquad (2) \end{aligned}$$

Since we consider a complete charging / discharging process, $\xi$ has to be multiplied by 2. T is the period of the sinusoidal power supply with frequency $f = \frac{1}{T}$. The sinusoidal power supply can be realized using an external inductor. Thus an LC resonant circuit with a resonance frequency of approximately $\frac{1}{\sqrt{LC}}$ is created and the energy is oscillated between the external inductor and the capacitances to be switched.

We considered the first clock distribution technique mentioned above, because it enables a low resistance path between the inductor and the capacitor resulting in a high-Q resonant circuit.

## 2. FIRST PROPOSED REGISTER

Sinusoidal clocks result in wide overlapping clock edges, preventing the correct functionality of the traditional registers. That implies the need for new register types. We

---

THIS WORK IS SUPPORTED BY THE GERMAN RESEARCH FOUNDATION (DFG) UNDER GRAND GL 144/18-1

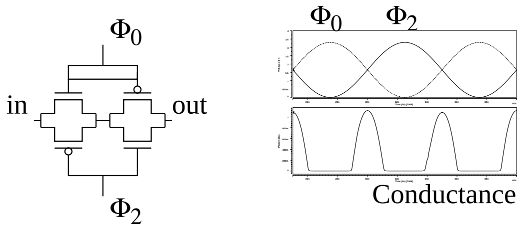

Figure 1: Pass-gate and SPICE simulation of conductance

suggest registers that use a 4-phase sinusoidal clock and take advantage of the overlapping clock edges. We use a pass-gate as shown in fig. 1. In this figure the result of a SPICE simulation of the conductance between the ports *in* and *out* is shown on the right hand side. There is a conducting phase and a long non-conducting phase. The conducting phases occur with twice the frequency of the sinusoidal clock, hereafter termed *effective clock frequency*.

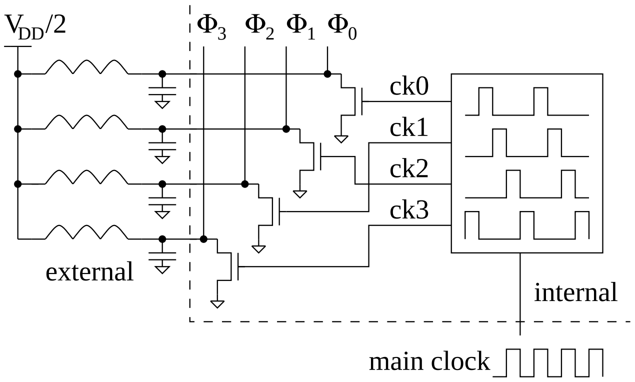

Figure 2: Generation of 4 phase clock

Using a four phase clock one can create two non overlapping conducting phases. The necessary 4 phase clock can be built with the circuit shown in fig. 2. The auxiliary clocks $ck0...ck3$ can be generated by a circuit similar to a Johnson counter using two D-latches and four NAND gates. The resonance frequency and phase of the oscillators can be tuned to $ck0 - ck3$ by putting extra capacitors in parallel with the load capacitance.

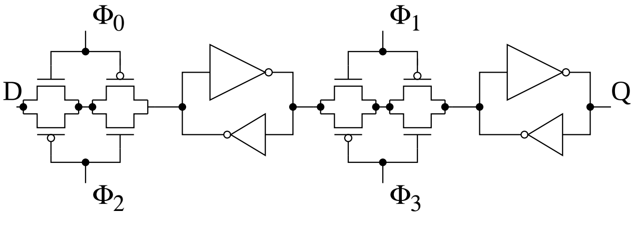

Figure 3: Proposed register

The two non-overlapping conducting phases can be used in a master-slave register. A schematic of the first register we propose is shown in fig. 3.

Of crucial interest for the correct functionality of the register is the duration of the conducting phases which depends on the frequency of the clock and on the deviation from the desired phase shift. Considering the pass-gate shown in fig. 1 with

$$\Phi_0 = \tfrac{1}{2}\hat{V} sin(\omega t) + \tfrac{1}{2}\hat{V} \tag{3}$$

and

$$\Phi_2 = \tfrac{1}{2}\hat{V} sin(\omega t + \phi) + \tfrac{1}{2}\hat{V}, \tag{4}$$

the conducting phase $T_{cond}$ can be defined as the minimum of the two periods of time in that both clock phases $\Phi_0$ and $\Phi_2$ are either above $V_{TN}$ or below $\hat{V} - |V_{TP}|$.

Assuming that the phase shift $\phi$ is approximately $\pi$, the point of intersection of the two curves can be calculated to

$$t_{intersect} = \frac{\phi - \pi}{2\omega}. \tag{5}$$

The point of intersection of $\Phi_0$ with the line $V = \hat{V} - |V_{TP}|$ in the interesting section of $\Phi_0$ is

$$t_{V_{TP}} = \frac{1}{\omega} \arcsin\left(1 - \frac{2|V_{TP}|}{\hat{V}}\right) \tag{6}$$

and the point of intersection with the line $V = V_{TN}$ is

$$t_{V_{TN}} = \frac{1}{\omega} \arcsin\left(\frac{2V_{TN}}{\hat{V}} - 1\right). \tag{7}$$

The conducting phase can now be calculated.

$$\begin{aligned} T_{cond} = min \quad ( \quad & 2(t_{V_{TP}} - t_{intersect}), \\ & 2(t_{intersect} - t_{V_{TN}})) \end{aligned} \tag{8}$$

Thus $T_{cond}$ is influenced linearly by the frequency and by the phase deviation from the desired phase shift $\pi$. Because the conduction phase has to have a certain duration, the frequency and allowed phase shift is limited.

Below this frequency limit, the energy dissipation depends only slightly on the frequency, as can be seen in fig. 4. That shows that it is possible to save energy with our approach over a wide range of frequencies.

Due to the structure of this register the clock-to-Q delay is slightly less than $\frac{1}{2}$ of the effective clock cycle time. The timing diagram shown in fig. 5 illustrates this.

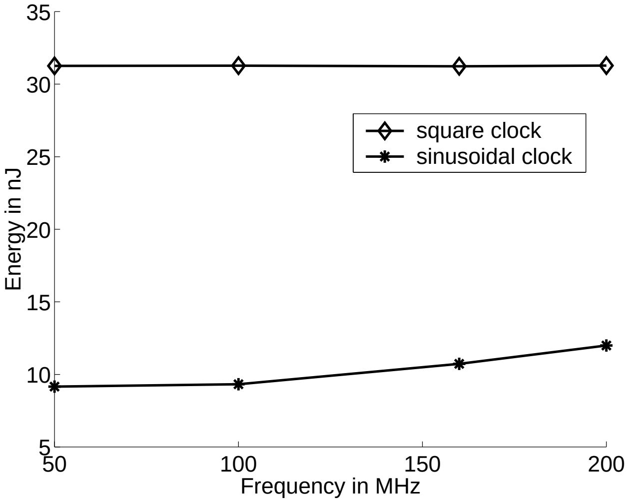

Figure 4: Consumed energy of 1000 registers during 10 effective clock cycles in dependence of the clock frequency with an input activity of 20%

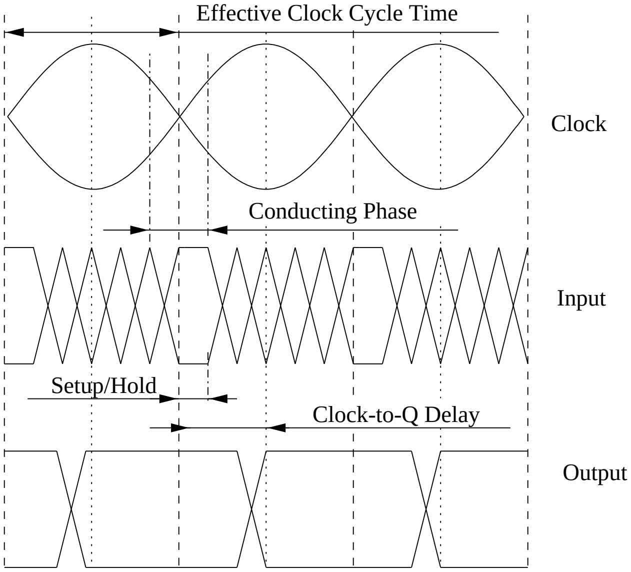

Figure 5: Timing diagram of first proposed register

## 3. SECOND PROPOSED REGISTER

The large clock-to-Q delay is one drawback of this approach because it nearly halves the time for computations. Thus we propose a second register that generates a local square wave clock out of the sinusoidal clock as depicted in fig. 6.

Here the respective conducting phases are used to pull the clock signal to $V_{DD}$ or $GND$ resulting in a clock frequency equal to the effective clock frequency. Thus we can still efficiently charge/discharge the global clock lines, while the local capacitances of the flipflop are charged/discharged in a static CMOS like manner.

## 4. EXPERIMENTAL RESULTS

We performed HSPICE simulations using the models of a $0.35\mu$ process made available to us via EUROPRACTICE to evaluate the functionality of the suggested registers and to determine the power consumption of our clocking approach. As a reference we used a conventional clocking scheme with static D flipflops and a single square wave clock.

To verify the functionality we simulated a 10-register-ring-buffer. The buffer functions correctly up to an effective clock frequency of 250MHz with the first register proposed and up to 300MHz with the second.

One problem that could occur with our approach is an unwanted phase shift of the clock phases, which would result in shorter conducting periods and in the worst case in an elimination of some of these periods.

In a period of 1.5ns before the end of the conducting phase the input into the first proposed register has to be stable. This time is necessary to change the state of the cross coupled inverters and determines the maximum frequency of this approach since a conducting phase has to be at least 1.5ns wide for the register to function correctly. Theoretical considerations and simulations showed that a phase shift of 5% is tolerable with an effective clock cycle time of 20ns. If there is no phase shift, the maximum obtainable clock frequency is theoretically 300MHz and with our non-ideal clock waveforms approximately 250MHz.

For the second proposed register a conducting period of 1.2ns is needed to change the state of the inverter preceding the CMOS flip-flop, which enables higher clock frequencies compared to the first approach.

We simulated the power needed by 1000 registers. Since the resistance of the charging/discharging path influences the power consumption when using a resonant clock, we included in our simulation a lumped resistance/capacitance of the interconnect to each register. The results are shown in fig. 7. The dissipated power at 0% input activity corresponds to the power consumption due to the charging/discharging of the clock lines and input capacitances of the flipflops and to the generation of the 4 phase clock. Because of the relatively high resistance of the pass-gate in fig. 1 during the conducting phase, the input to the cross coupled inverters of the first proposed register changes slowly and there are higher short-cut currents compared to the case with square wave clocks. That results in a steeper increase of the dissipated power when the input activity increases. Thus this register consumes more power when the state of the flipflop changes in each cycle which corresponds to an input activity of 100%. More realistic values for the input activity show relatively large power savings of the first proposed register over a wide range of frequencies. For a realistic input activity of 25% there is a power dissipation advantage of 70% of our approach compared to the conventional scheme. If there is no input activity, our approach needs less than 3% of the power needed by the conventional scheme.

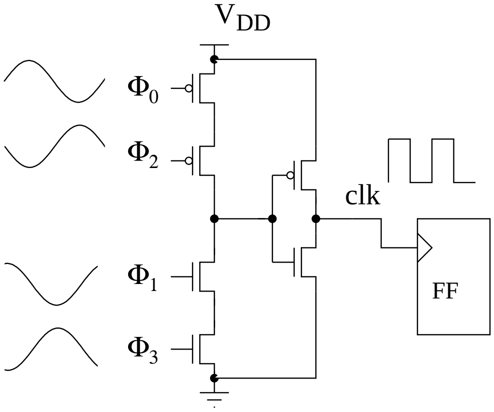

Figure 6: Circuit for the local generation of a square wave clock signal

The second proposed register charges/discharges the clock lines with an resonant clock, dissipating energy following equation 2, whereas the input capacitances of the register after the square wave clock generator are charged and discharged conventionally. Thus the activity dependence of the power dissipation is similar to the conventional register.

Additionally, it can be observed that our approach reduces the noise because there are no high-frequency components in a sinusoidal clock.

## 5. CONCLUSION

In this paper we propose to use a sinusoidal clock which allows us to save 30% to 70% in terms of power dissipation. Because classical registers need steep clock edges, we propose two registers that can cope with sinusoidal clock waveforms. The problems that can occur with non ideal phase shifts of the needed 4 phase clock are analyzed and limits for the allowed deviation in dependence of the clock frequency are derived.

## 6. REFERENCES

[ASK$^{+}$94] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzanis, and E. Y.-C. Chou. Low-Power Digital Systems Based on Adiabatic-Switching Principles. *IEEE Transactions on Very Large Scale Integration*, 2(4):398 – 407, October 1994.

[Fre98] Jerry Frenkil. A multi-level approach to low-power ic design. *IEEE Spectrum*, pages 54 – 60, feb 1998.

[MONC97] Dragan Maksimovic, Vojin G. Oklobdzija, Borivoje Nikolic, and K. Wayne Current. Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply: Experimental Results. In *International Symposium on Low Power Electronics and Design*, Monterey, CA, August 1997.

[SFM$^{+}$85] C. L. Seitz, A. H. Frey, S. Mattisson, S. D. Rabin, D. A. Speck, and J. L. A. van de Snepscheut. Hot-clock NMOS. In *Proc. 1985 Chapel Hill Conf. VLSI*, pages 1–17, 1985.

[WE93] Neil H. E. Weste and Kamran Eshraghian. *Principles of CMOS VLSI Design - A System Perspective*. Addison-Wesley Publishing Company, 1993.

[YK94] S. G. Younis and T. F. Knight. Asymptotically zero energy split-level charge recovery logic. In *Int. Workshop Low Power Design*, pages 177 – 182, 1994.

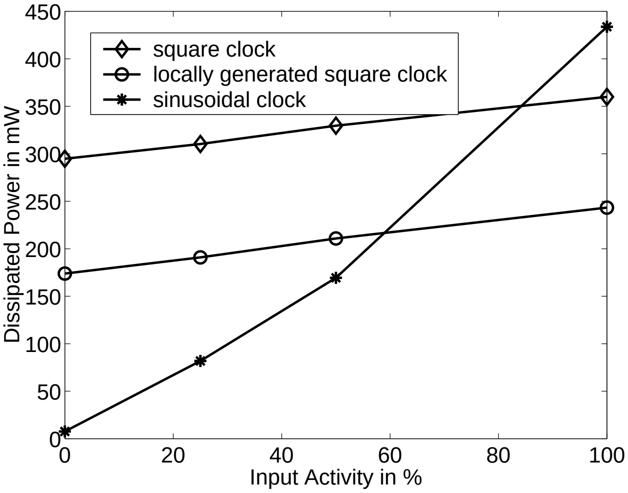

Figure 7: Dissipated power in dependence of the input activity with 100MHz effective clock frequency